SGM852
Dual Adjustable Voltage Detector with Reset and Gate Driver Outputs

GENERAL DESCRIPTION

The SGM852 is a dual adjustable voltage detector with reset and gate driver outputs. Two adjustable sense inputs can monitor a wide voltage range through external resistor dividers. The device has internal sequence timing. The delay time of two outputs can be programmed by their respective external capacitors. The gate driver output is implemented for external N-MOSFET by a charge pump circuit.

Two options are available. When both VSEN1 and VSEN2 voltages exceed the internal fixed rising threshold voltage in SGM852A, or VSEN1 voltage exceeds the internal fixed rising threshold and VSEN2 voltage falls below the internal fixed falling threshold in SGM852B, both internal comparators output high, the reset output (nRESET) asserts high after a propagation delay and a capacitor charge set-time delay. And if either of the comparators outputs low, nRESET asserts low.

The SGM852 is available in a Green TDFN-3×3-10L package. It operates over a junction temperature range of -40℃ to +125℃.

FEATURES

- **Operating Voltage Range: 3V to 16V**
- **Low Dual Adjustable Threshold:**
  - **Rising Threshold: 0.6V (TYP)**
  - **Falling Threshold: 0.55V (TYP)**
- **High Threshold Accuracy:**
  - **Rising Threshold Accuracy: ±1.5%**
  - **Falling Threshold Accuracy: ±2%**
- **Push-Pull Reset Output**
- **Gate Driver Output**
- **Capacitor-Adjustable Delay Time**
- **Available in a Green TDFN-3×3-10L Package**

APPLICATIONS

Power Sequencing and Reset Sequencing
Power Switching
Portable Equipment
Computers/Servers

TYPICAL APPLICATION

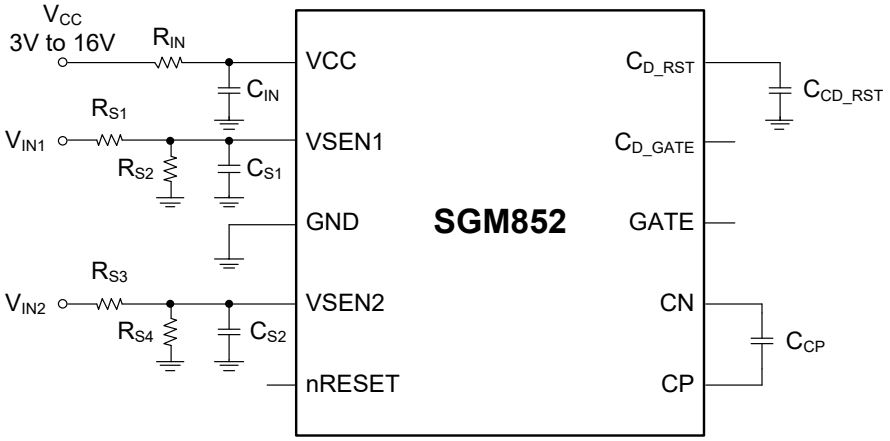


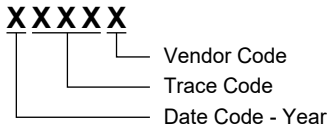
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM852A	TDFN-3×3-10L	-40℃ to +125℃	SGM852AXTD10G/TR	SGM 852AD XXXXX	Tape and Reel, 4000
SGM852B	TDFN-3×3-10L	-40℃ to +125℃	SGM852BXTD10G/TR	SGM 852BD XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VCC ..... -0.3V to 24V
VSEN1, VSEN2 ..... -0.3V to 3.5V
CP, GATE ..... -0.3V to 12.6V
All Other Pins ..... -0.3V to 6V
Package Thermal Resistance
TDFN-3×3-10L, θ_{JA} ..... 51℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 3000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

VSEN1, VSEN2 ..... 0V to 3V
Operating Supply Range, V_{CC} ..... 3V to 16V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

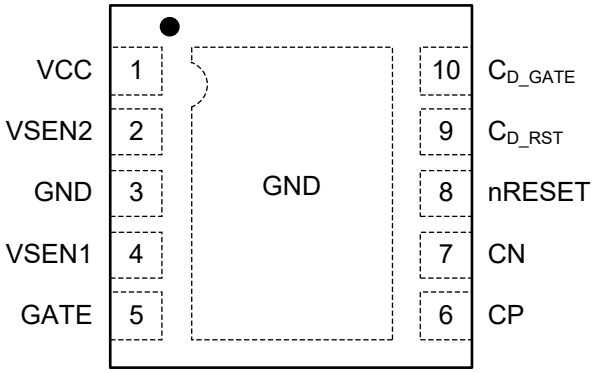
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-3×3-10L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VCC	Supply Voltage.
2	VSEN2	Input Sense Voltage Pin 2.
3	GND	Ground Pin. GND is connected to the exposed pad and soldered to a large PCB for maximum power dissipation.
4	VSEN1	Input Sense Voltage Pin 1.
5	GATE	N-MOSFET Gate Driver Output.
6	CP	Charge Pump Capacitor Pin. Positive Node.
7	CN	Charge Pump Capacitor Pin. Negative Node.
8	nRESET	Active-Low Push-Pull Reset Output Pin. For SGM852A, it goes high when both VSEN1 and VSEN2 exceed the rising threshold voltage. For SGM852B, it goes high when VSEN1 exceeds the rising threshold voltage and VSEN2 falls below the falling threshold voltage.
9	C_{D_RST}	Capacitor to Set Delay Time for nRESET Pin. Connect this pin to GND through an external capacitor to set the reset delay time. Leave this pin open to set faster delay time.
10	C_{D_GATE}	Capacitor to Set Delay Time for Gate Pin. Connect this pin to GND through an external capacitor to set the GATE delay time. Leave this pin open to set faster delay time.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 16V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

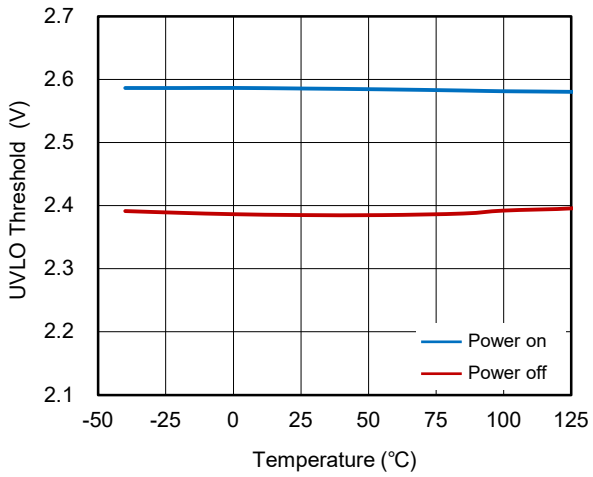
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCC						
Operating Voltage	V_{CC}		3		16	V
Supply Current	I_{CC}	Charge pump off		39	66	μA
POR Threshold	V_{POR}		2.5	2.6	2.7	V
POR Hysteresis	ΔV_{PHYS}			200		mV
SENSE1/SENSE2						
Rising Threshold	V_{RTH}		0.591	0.6	0.609	V
Falling Threshold	V_{FTH}		0.539	0.55	0.561	V
Hysteresis	ΔV_{RHYS}			50		mV
Input Current	I_{SENSE}	V_{SENx} < 1V	-100		100	nA
nRESET						
nRESET Output Voltage	V_{OH}	Logic-High, V_{CC} = 3V, I_R = -2mA	2.6	2.87	3	V
		Logic-High, V_{CC} = 4V I_R = -2mA	3.6	3.88	4	
		Logic-High, V_{CC} = 5V, I_R = -2mA	3.9	4.68	5	
		Logic-High, V_{CC} > 5.5V, I_R = -2mA	3.9	4.54	5.5	
	V_{OL}	Logic-Low, I_R = 2mA	0		0.4	
Timing						
C_{D_RST} Source Current	I_{CD_RST}	V_{SEN1} > 0.6V, V_{SEN2} > 0.6V for SGM852A V_{SEN1} > 0.6V, V_{SEN2} < 0.55V for SGM852B	0.925	1	1.075	μA
C_{D_GATE} Source Current	I_{CD_GATE}	V_{SEN1} > 0.6V, V_{SEN2} > 0.6V for SGM852A V_{SEN1} > 0.6V, V_{SEN2} < 0.55V for SGM852B	0.925	1	1.075	μA
GATE Output Voltage (1)	V_{GATE}	V_{CC} ≤ 5V	-10%	2 × V_{CC}	+10%	V
		V_{CC} > 5V	9.0	10.0	11.0	
C_{D_RST} Trip Rising Threshold	V_{RTH_RST}		1.191	1.234	1.277	V
C_{D_RST} Hysteresis	V_{HYS_RST}			50		mV
C_{D_GATE} Trip Rising Threshold	V_{RTH_GATE}		1.191	1.234	1.277	V
C_{D_GATE} Hysteresis	V_{HYS_GATE}			50		mV
C_{D_RST} Discharging Resistor		I_{CD_RST} = 10mA		7	12	Ω
C_{D_GATE} Discharging Resistor		I_{CD_GATE} = 10mA		7	12	Ω
Over-Temperature Protection						
Thermal Shutdown	T_{SD}			155		℃
Thermal Shutdown Hysteresis	ΔT_{SD}			20		℃

NOTE:

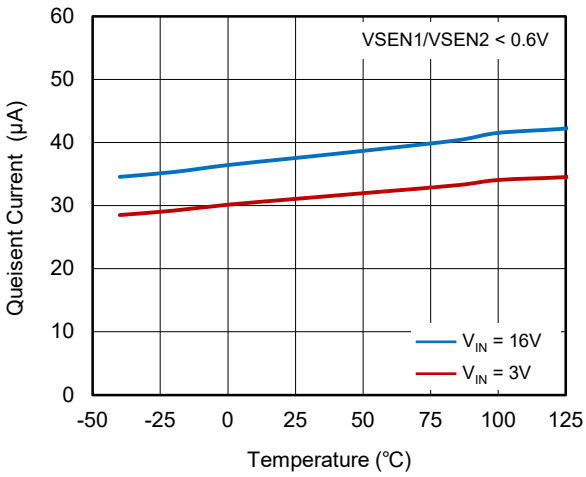
1. Note that when V_{GATE} is from 0V to 2 × V_{CC} (or from 0V to 10V), it needs to go through several cycles, during which a large current will flow from the GATE pin.

TYPICAL PERFORMANCE CHARACTERISTICS

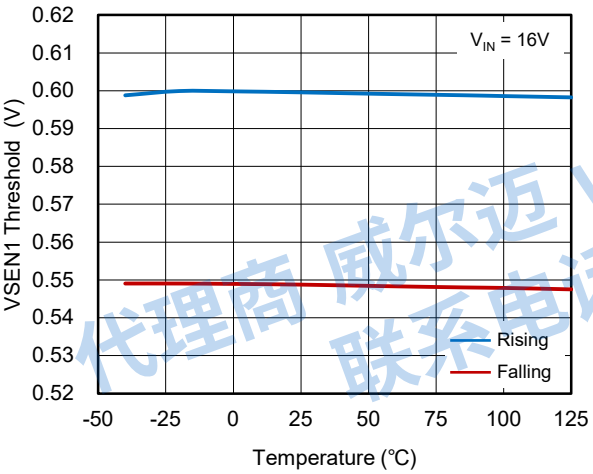
UVLO Threshold vs. Temperature



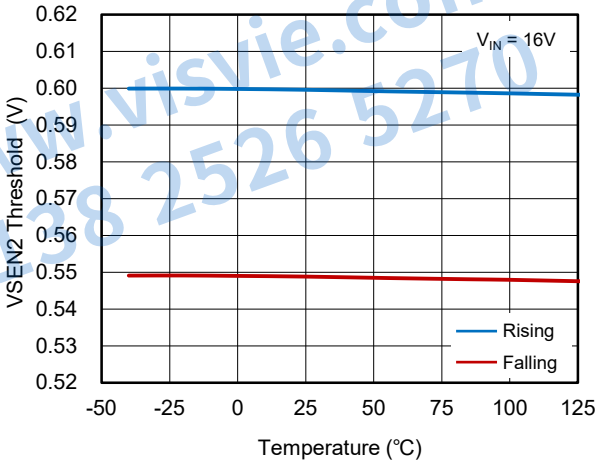
Quiescent Current vs. Temperature



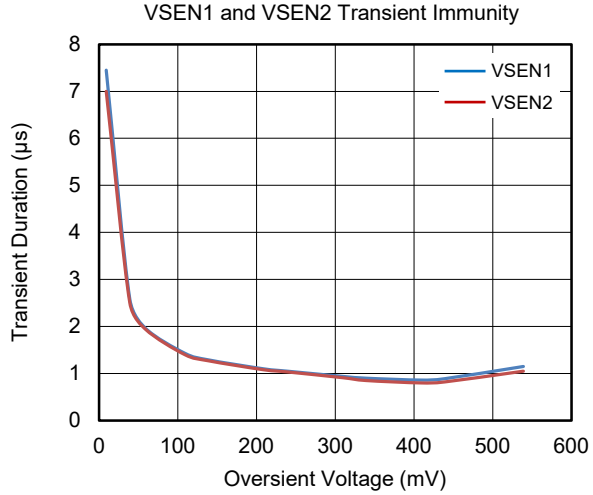
VSEN1 Threshold vs. Temperature



VSEN2 Threshold vs. Temperature



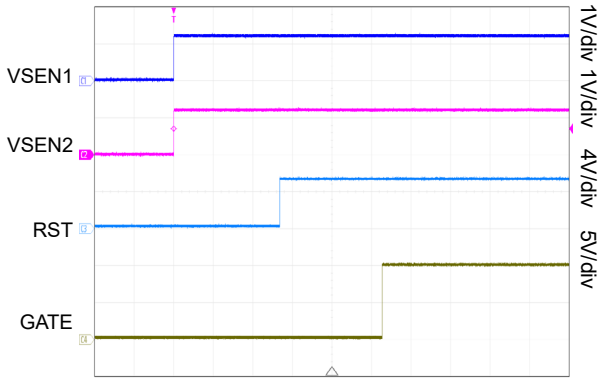
VSEN1 and VSEN2 Transient Immunity



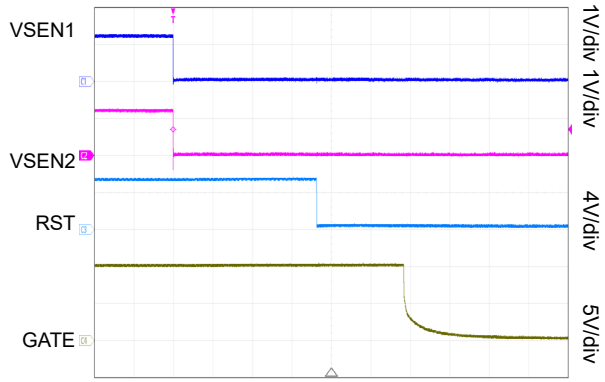
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 16V, C_{IN} = 100nF, C_{CP} = 47nF, C_{CD_RST} = 1μF, C_{CD_GATE} = 1μF, C_{GATE} = 1nF, VSEN1 = VSEN2 = 0V to 1.2V.

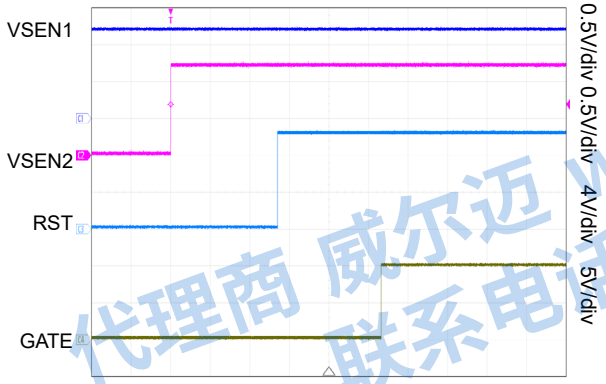
VSEN1 and VSEN2 Power on



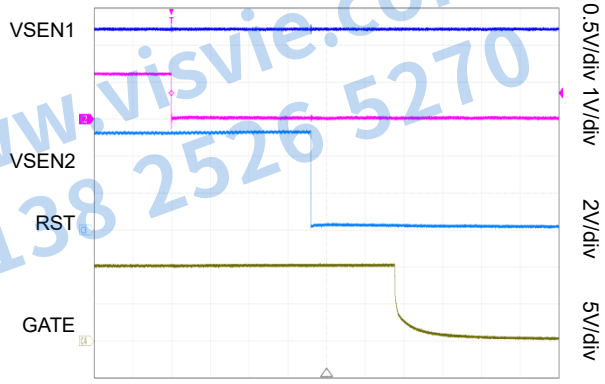
VSEN1 and VSEN2 Power off



VSEN2 Power on



VSEN2 Power off



FUNCTIONAL BLOCK DIAGRAM

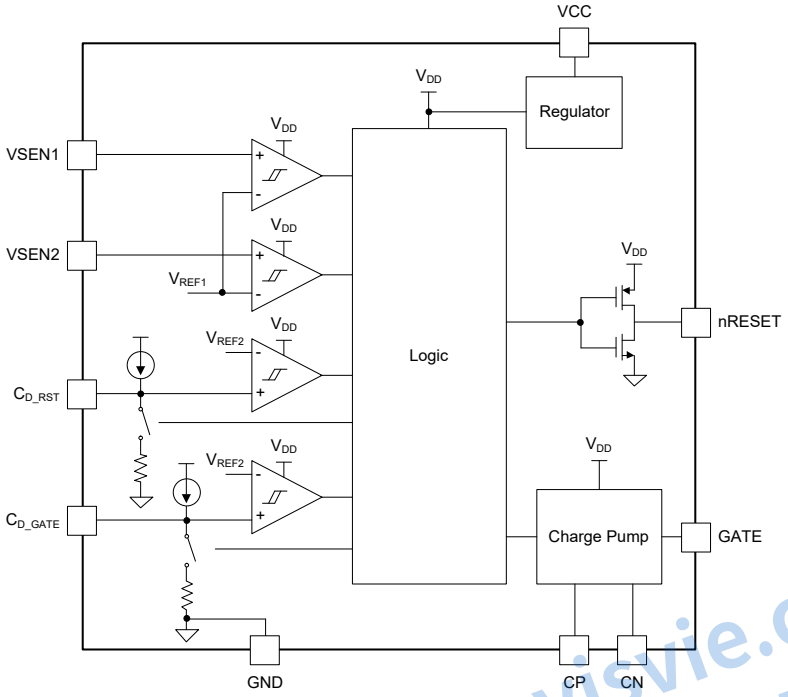


Figure 2. SGM852A Block Diagram

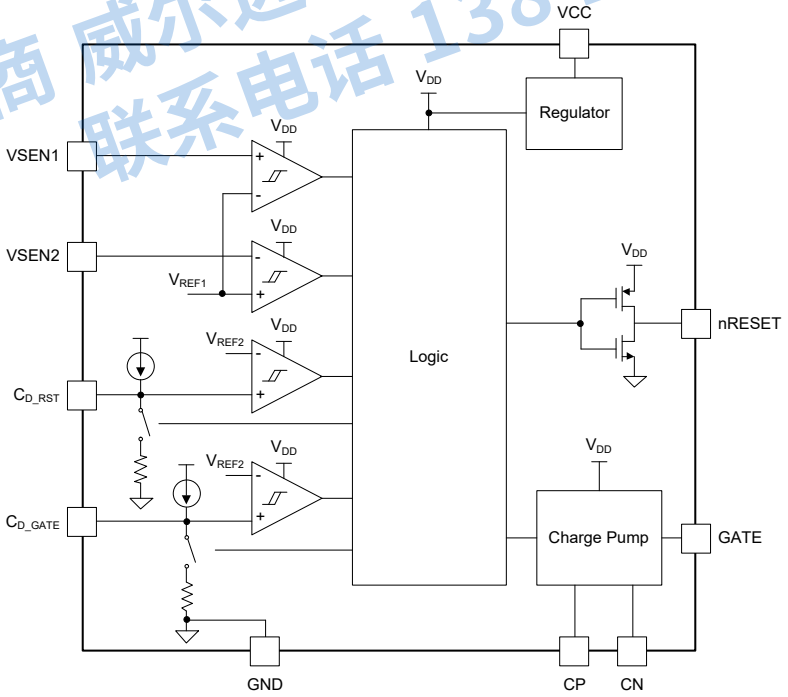


Figure 3. SGM852B Block Diagram

DETAILED DESCRIPTION

The SGM852 is used to monitor dual-voltage systems and provides sequential control with two outputs. When the power input voltage (V_{CC}) exceeds the POR threshold voltage, V_{POR} (2.6V, TYP), dual voltages are monitored through the respective external resistor dividers into VSEN1 and VSEN2 pin. Once both VSENx voltages exceed the internal fixed rising threshold, V_{RTH} (0.6V, TYP), in SGM852A or once VSEN1 exceeds V_{RTH} and VSEN2 falls below the fixed falling threshold V_{FTH}, (0.55V, TYP), in SGM852B, both internal comparators output high, the internal 1μA (TYP) current source I_{CD_RST} starts charging external capacitor at C_{D_RST} pin. Once the voltage at C_{D_RST} pin exceeds V_{RTH_RST} (1.234V, TYP), the nRESET outputs high and then another 1μA (TYP) current source I_{CD_GATE} starts charging external capacitor at C_{D_GATE} pin. Once the voltage at C_{D_GATE} pin exceeds V_{RTH_GATE} (1.234V, TYP), the GATE pin starts to drive an external N-MOSFET with a voltage level of 2 × V_{DD}. Accordingly, the corresponding delay time can be programmed by choosing the capacitors at C_{D_RST} pin and C_{D_GATE} pin. If either of the two comparators outputs low, the nRESET outputs low and charge pump is disabled.

Comparators

The comparators can provide threshold voltage to monitor VSEN1 and VSEN2 sensing voltage, V_{VSEN1} and V_{VSEN2}. For SGM852A, both VSEN1 and VSEN2 are connected to the positive input of the corresponding comparator, while the internal reference is connected to the negative input of the two comparators. So when both VSEN1 and VSEN2 exceed V_{RTH}, the nRESET outputs high after a C_{D_RST} controlled delay time. For SGM852B, VSEN1 is connected to the positive input of the comparator with the internal reference connecting to the negative input of the comparator, while VSEN2 is connected to the negative input of the comparator with the internal reference connecting to the positive input of the comparator. Therefore, for SGM852B, when VSEN1 exceeds V_{RTH} and VSEN2 falls below V_{FTH}, both comparators output high, and the nRESET outputs high after a C_{D_RST}-controlled delay time. If either of the comparators outputs low, the nRESET outputs low.

Power-On Reset (POR)

The device resets all fault latches and starts to monitor V_{VSEN1} and V_{VSEN2} once V_{CC} exceeds 2.6V.

Charge Pump

The charge pump with an internal oscillator is designed to drive external N-MOSFET with a voltage level of 2 × V_{DD}.

Regulators

The input voltage of the SGM852 is range from 3V to 16V. The built-in regulator provides 5V internal V_{DD} if V_{CC} is above 5V, and it tracks V_{CC} if V_{CC} is below 5V.

Push-Pull Reset Output

The nRESET is a push-pull reset output pin. When both internal comparators output high, the nRESET asserts high after C_{D_RST}-controlled delay time. And if either of the comparators outputs low, nRESET asserts low after C_{D_RST} is discharged.

GATE Output

When nRESET asserts high, the charge pump is enabled after C_{D_GATE}-controlled delay time. And then, GATE provides a voltage of 2 × V_{DD} to drive the external N-MOSFET. If nRESET asserts low, the charge pump is disabled after C_{D_GATE} discharged, and GATE will be discharged to 0V.

Over-Temperature Protection (OTP)

The SGM852 may heat up due to power dissipation, and then enter into the thermal shutdown state. The thermal shutdown threshold T_{SD} is +155℃ (TYP). The OTP will turn off charge pump and timer function during this state. Accordingly, both nRESET and GATE output low. And the device will be shut down and remain off until the IC temperature drops below +135℃ (TYP).

APPLICATION INFORMATION

VSENx Transient Immunity

The VSEN1 and VSEN2 pins of the SGM852 have certain anti-interference ability. Once the transient duration exceeds the corresponding maximum allowed time, the nRESET pin will go low.

Adjustable Input Sensing Threshold

The dual sense inputs, VSEN1 and VSEN2, can monitor system voltage through a resistive divider network with V_{RTH} in a wide range. As shown in Figure 4, V_S is the system voltage. The trigger voltage of system V_{S_TH} can be calculated by equation (1):

$$V_{S\_TH} = V_{TH} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

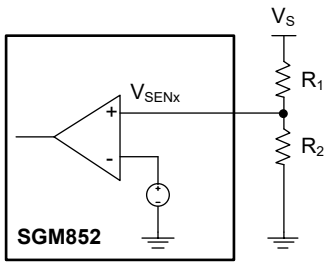


Figure 4. Setting Trigger Voltage of System

The absolute maximum voltages of VSEN1 and VSEN2 are not allowed to exceed 3V. Due to the leakage currents of them are 100nA, the accuracy of V_{S_TH} should be taken into consideration. However, low value resistor will cause more power consumption. Appropriate selection of resistance value is also very critical.

The appropriate resistance value can be selected through the following equation based on the amount of acceptable error.

$$R_1 = \frac{V_{S\_TH} \times \varepsilon}{I_{SENSE}} \quad (2)$$

V_{S_TH} is the system trigger voltage that nRESET pin asserts high, and ε is maximum acceptable error on V_{S_TH}, I_{SENSE} is the leakage current of VSEN1 and VSEN2 pins. R_2 can be calculated by equation (3):

$$R_2 = \frac{V_{TH} \times R_1}{V_{S\_TH} - V_{TH}} \quad (3)$$

Adjustable Delay (C_{D_RST}, C_{D_GATE})

Users should choose external capacitors to set the charge time from internal 1μA (TYP) current source and thus set nRESET and GATE pins output delay time. When the input voltage exceeds the POR threshold voltage, VSEN1 and VSEN2 pins will start to monitor system voltages. Once both outputs of the comparators are high, a 1μA (TYP) current source starts charging external capacitor at C_{D_RST} pin. Once the voltage at C_{D_RST} pin exceeds V_{RTH_RST}, the nRESET outputs high and then another 1μA (TYP) current source starts charging external capacitor at C_{D_GATE} pin. Once the voltage at C_{D_GATE} pin exceeds V_{RTH_GATE}, the GATE pin start to drive an external N-MOSFET with 2 × V_{DD} voltage level by the charge pump circuit. The delay time can be calculated by equations (4) and (5):

$$t_{CD\_RST} = \frac{1.234V \times C_{CD\_RST}}{1\mu A} \quad (4)$$

$$t_{CD\_GATE} = \frac{1.234V \times C_{CD\_GATE}}{1\mu A} \quad (5)$$

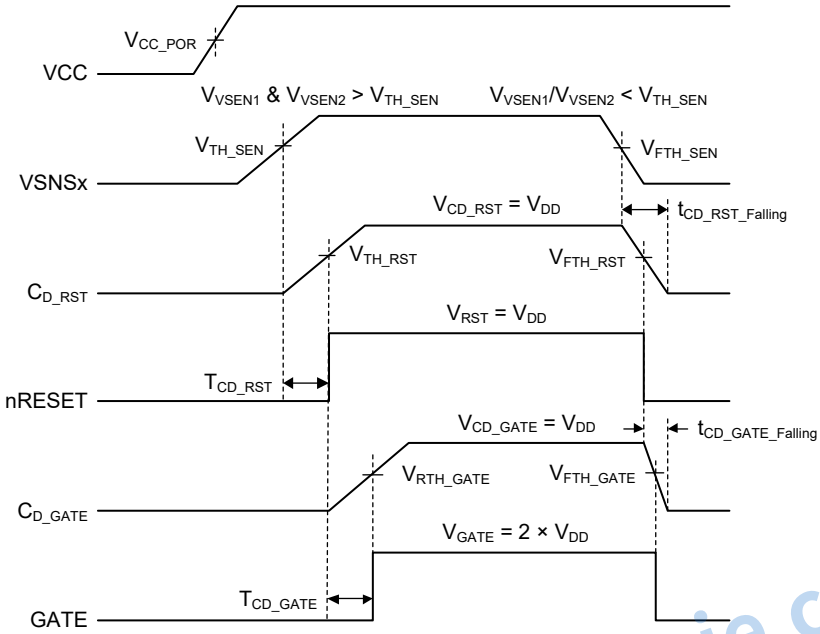
where:

t_{CD_RST} and t_{CD_GATE} are in seconds

C_{CD_RST} and C_{CD_GATE} are in Farads.

When either output of the comparators is low, the respective capacitors start to discharge on C_{D_RST} and C_{D_GATE} pins. Once the voltage level is lower than 1.184V (50mV Hysteresis, TYP), the nRESET and GATE go low. Figure 5 shows the time sequence.

APPLICATION INFORMATION (continued)



NOTE: 1. V_{DD} is only internally used. It tracks V_{CC} if V_{CC} is below 5V, and it is close to 5V if V_{CC} is above 5V.

Figure 5. SGM852A Timing Sequence Diagram

Typical Application Circuits

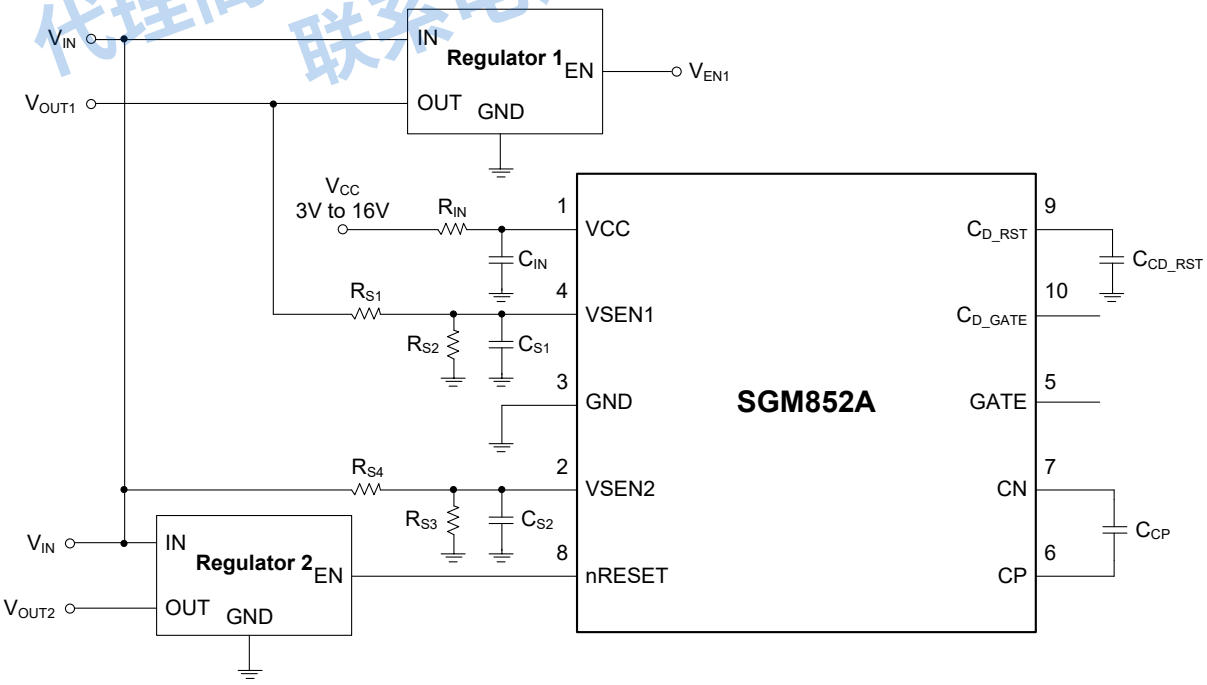


Figure 6. Power on Sequential Control Application Circuit of SGM852A

APPLICATION INFORMATION (continued)

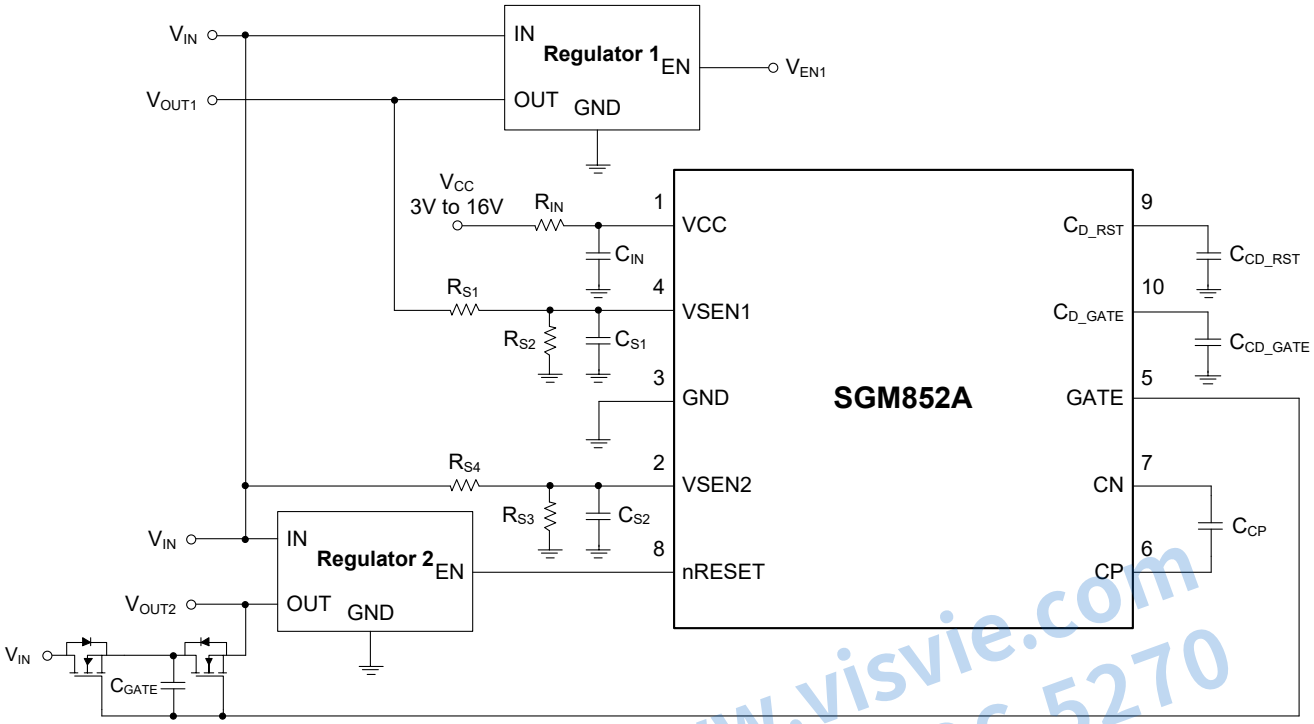


Figure 7. Drive N-MOSFET to Control Output Connection of SGM852A

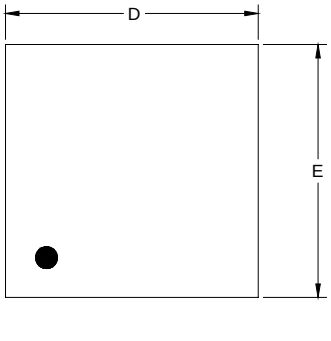
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

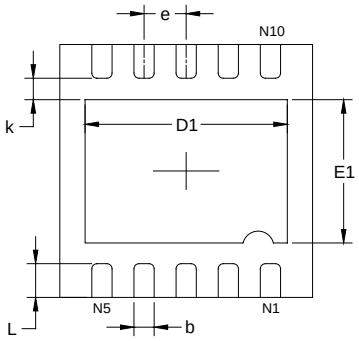
Changes from Original (SEPTEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

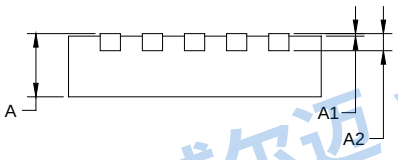
TDFN-3×3-10L



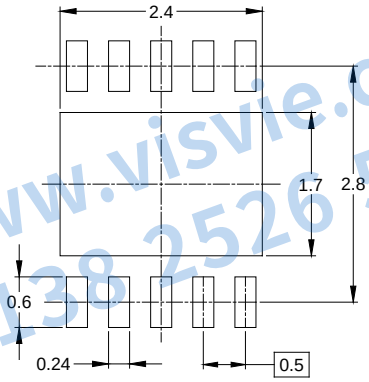
TOP VIEW



BOTTOM VIEW



SIDE VIEW



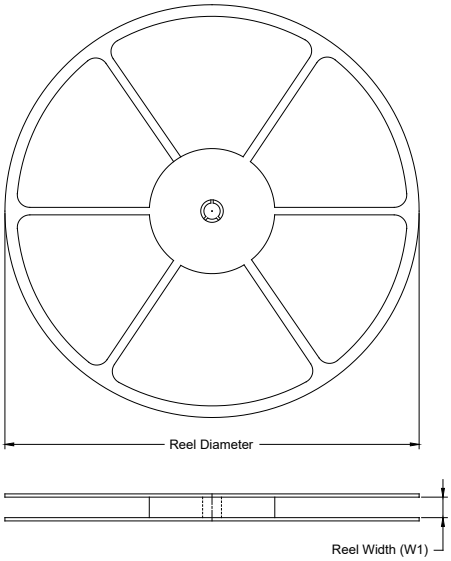
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

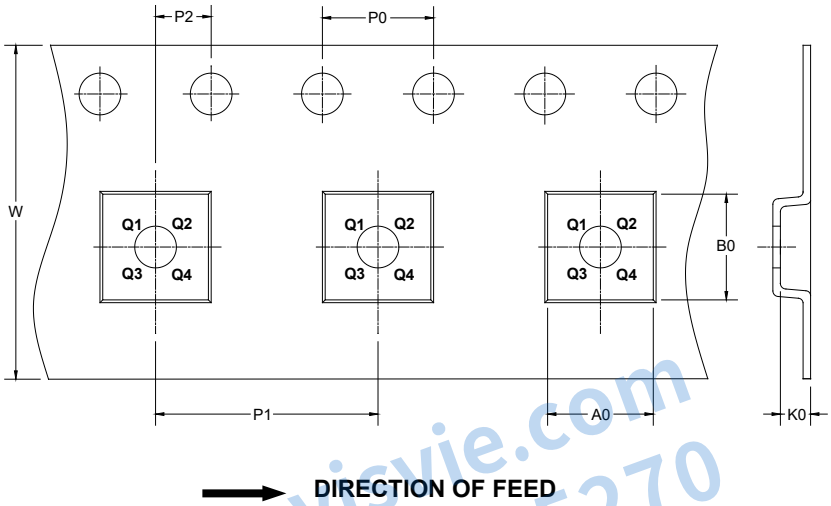
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



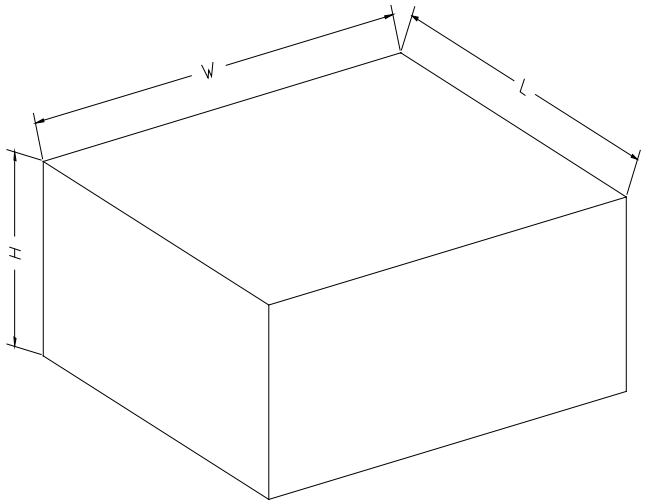
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002