# SGM61061
# 6A High Efficiency Synchronous Buck Converter

## GENERAL DESCRIPTION

The SGM61061 device is a 2.8V to 5.5V synchronous Buck converter with constant off-time architecture that is optimized solution for high efficiency and compact size. The device integrates switches capable of delivering an output current up to 6A.

When MODE input is lower than 0.4V or floating, SGM61061 enters into a pulse frequency modulation (PFM) mode. At medium to heavy loads, the device operates in pulse width modulation (PWM) mode with 1.4MHz (TYP) switching frequency. At light loads, the device automatically enters in power-save mode (PSM) to maintain high efficiency over the entire load current range. When MODE input voltage is more than 1.2V, SGM61061 enters into a pulse width modulation (PWM) mode over the entire load current range. In shutdown state, the current consumption is reduced to 0.5μA (MAX).

The SGM61061 can dynamic regulate output voltage by MODE/VCON pin to meet some situations need change output voltage directly. When MOED/VCON pin get an appropriate voltage value (from 0.6V to 1.1V), SGM61061 will work in PWM mode and internal reference voltage changes smoothly to achieve a new output voltage without changing external resistor divider.

The SGM61061 is available in a Green TQFN-2×3-12L package.

## FEATURES

- **6A Maximum Output Current**
- **2.8V to 5.5V Input Voltage Range**
- **Low $R_{DSON}$ Internal Switches: 20mΩ/13mΩ**
- **Quiescent Current ($V_{IN}$ = 3.6V): 46μA (TYP)**
- **1.4MHz Switching Frequency (Constant Off-Time)**
- **Low Dropout with 100% Duty Cycle**
- **External Control of Operation Mode**
- **External Control of VCON**
- **Adjustable Output Voltage from 0.6V to $V_{IN}$**
- **Output Discharge Function**
- **1.3ms of Internal Soft-Start Time and Pre-bias Startup**
- **Cycle-by-Cycle Over-Current Protection**
- **Hiccup Mode OCP/Short-Circuit Protection**
- **Stable with Low-ESR Output Ceramic Capacitors**
- **Thermal Shutdown Protection**
- **Available in a Green TQFN-2×3-12L Package**

## APPLICATIONS

Battery-Powered Applications
Point-of-Load
Processor Power Supplies
Hard Disk Drives (HDD)/Solid State Drives (SSD)

## TYPICAL APPLICATION

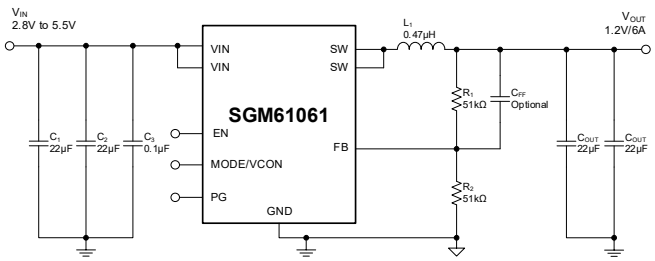
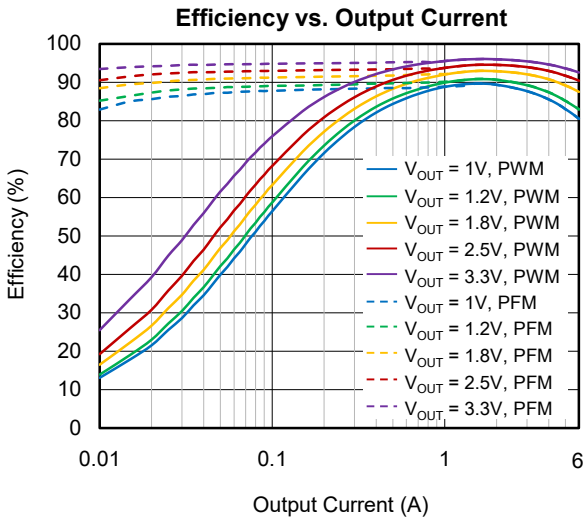



**Figure 1. Typical Application Circuit**

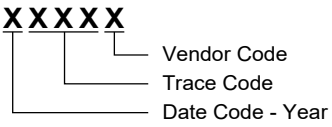


# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM61061 | TQFN-2×3-12L | -40℃ to +125℃ | SGM61061XTSS12G/TR | 05HSS<br>XXXXX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Pin Voltages Referred to GND
VIN, FB, EN, PG ..... -0.3V to 6V
SW (DC) ..... -0.3V to $V_{IN}$ + 0.3V
SW (AC, Less than 10ns) while Switching ..... -3V to 8V
Package Thermal Resistance
TQFN-2×3-12L, $\theta_{JA}$ ..... 74℃/W
Junction Temperature Range ..... -40℃ to +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... 4000V
CDM ..... 1000V

## RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, $V_{IN}$ ..... 2.8V to 5.5V
Output Voltage Range, $V_{OUT}$ ..... 0.6V to $V_{IN}$
Maximum $V_{PG}$ ..... 5.5V
Output Current Range, $I_{OUT}$ ..... 0A to 6A
Junction Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings can cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods can affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

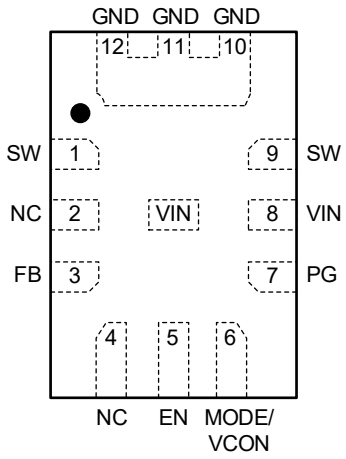
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits can be more susceptible to damage because even small parametric changes have a probability of causing the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




TQFN-2×3-12L

## PIN DESCRIPTION

| PIN | NAME | I/O | FUNCTION |
|---|---|---|---|
| 1, 9 | SW | O | Switching Node Output of the Converter. Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin. |
| 2, 4 | NC | -- | No Connection. This pin can be left open or connected to any other pin. |
| 3 | FB | I | Feedback Pin for Internal Control Loop. Connect this pin to an external feedback divider. |
| 5 | EN | I | Device Enable Input. Enable: High voltage level. |
| 6 | MODE/VCON | I | PWM and PFM Selection. When MODE voltage is more than 1.2V, the device enters PWM mode. When MODE voltage is lower than 0.4V or floating, the device enters PFM mode.<br>Analog Voltage Dynamic Regulation. Analog voltage input pin which control output voltage by PWM mode. |
| 7 | PG | O | Power Good Open-Drain Output Pin. The output of this pin is an open-drain with internal 520kΩ pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level, otherwise it is low. There is a 150μs delay between when $V_{FB}$ reaches PG threshold to when the PG pin goes high. |
| 8, Exposed Pad | VIN | P | Power Supply Voltage Input. A decoupling capacitor is required to ground to reduce switching spikes. The input capacitor should be placed as close as possible to the IC pins. |
| 10, 11, 12 | GND | G | Ground Pin. Connect these pins to larger copper areas to the negative terminals of the input and output capacitors. |

NOTE: I = input, O = output, P = power, G = ground.

## ELECTRICAL CHARACTERISTICS

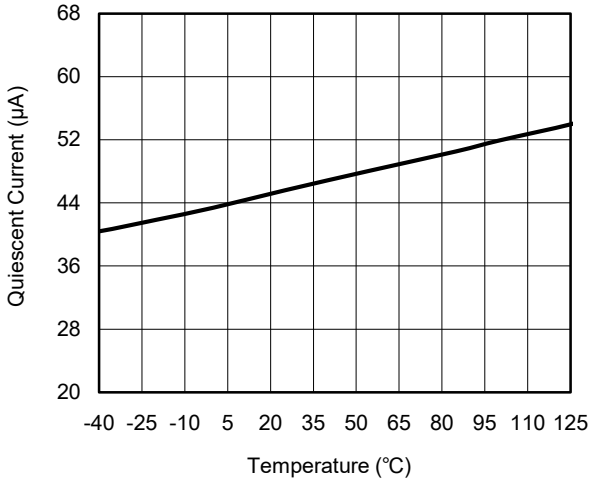
($V_{IN}$ = 3.6V and $T_J$ = -40℃ to +125℃, and all typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| Quiescent Current into VIN Pin | $I_Q$ | Not switching, $V_{IN}$ = 3.6V, $V_{EN}$ = 2V, $V_{FB}$ = 0.65V | $T_J$ = +25℃ | | 46 | 60 | μA |
| | | | $T_J$ = -40℃ to +125℃ | | | 70 | |
| Shutdown Current into VIN Pin | $I_{SD}$ | $V_{EN}$ = 0V | $T_J$ = +25℃ | | 0.02 | 0.5 | μA |
| | | | $T_J$ = -40℃ to +125℃ | | | 1.8 | |
| Input Under-Voltage Lockout Threshold | $V_{UVLO}$ | $V_{IN}$ rising, no Load | | 2.4 | 2.55 | 2.7 | V |
| Input Under-Voltage Lockout Hysteresis | | $V_{IN}$ falling hysteresis, no Load | | | 300 | | mV |
| Thermal Shutdown | $T_{JSD}$ | Junction temperature rising | | | 150 | | ℃ |
| | | Junction temperature falling | | | 130 | | |
| **EN Input** | | | | | | | |
| High-Level Threshold at EN Pin | $V_{IH}$ | | | 1.2 | | | V |
| Low-Level Threshold at EN Pin | $V_{IL}$ | | | | | 0.4 | V |
| EN Input Leakage Current | $I_{ENLKG}$ | $V_{EN}$ = 2V | | | 2 | | μA |
| | | $V_{EN}$ = 0V | | | 0 | | |
| **Soft-Start, Power Good** | | | | | | | |
| Soft-Start Time | $t_{SS}$ | Time from $V_{EN}$ high to 95% of $V_{OUT}$ nominal | | | 1.3 | | ms |
| Power Good Threshold | $V_{PG}$ | $V_{FB}$ rising, referenced to $V_{FB}$ nominal | | | 90 | | % × $V_{FB\_NOM}$ |
| | | $V_{FB}$ falling, referenced to $V_{FB}$ nominal | | | 85 | | |
| Power Good Over-Voltage Threshold | $V_{PG\_OV}$ | PG OV threshold rising | | | 115 | | |
| | | PG OV threshold falling | | | 110 | | |
| Power Good Low-Level Output Voltage | $V_{PG\_OL}$ | $I_{SINK}$ = 1mA | | | 0.13 | 0.3 | V |
| PG Internal Pull-Up Resistor | $R_{PG}$ | | | | 520 | | kΩ |
| Power Good Delay Time | $t_{PG\_DLY}$ | PG rising edge | | | 150 | | μs |
| **Output and Feedback** | | | | | | | |
| Feedback Regulation Voltage (ADJ) | $V_{FB\_NOM}$ | $V_{IN}$ = 2.8V to 5.5V, $T_J$ = +25℃ | | 0.594 | 0.600 | 0.606 | V |
| Feedback Input Leakage Current | $I_{FB\_LKG}$ | $V_{FB}$ = 0.65V | | | 1 | 100 | nA |
| Output Discharge Resistor | $R_{DIS}$ | $V_{EN}$ = low, $V_{OUT}$ = 1.8V | | | 40.5 | | Ω |
| **Power Switch** | | | | | | | |
| High-side FET On-Resistance | $R_{DSON}$ | | | | 20 | 36 | mΩ |
| Low-side FET On-Resistance | | | | | 13 | 24 | |
| PMOS SW Leakage Current | $I_{SWLKG}$ | $V_{IN}$ = 3.6V | | | 0.02 | 1.5 | μA |
| NMOS SW Leakage Current | | | | -1 | -0.01 | | |
| High-side Peak Current Limit | $I_{LIM\_H}$ | Output short, $T_J$ = +25℃ | | 7.5 | 8.8 | 10.1 | A |
| Low-side Valley Current Limit | $I_{LIM\_L}$ | | | | 6 | | |
| Low-side Negative Current Limit | $I_{LIM\_LN}$ | In forced PWM mode when OVP | | | -2 | | |
| Low-side ZCD Threshold | $I_{ZCD}$ | PFM mode, $V_{OUT}$ = 1.8V | | | 0.09 | | |
| Switching Frequency | $f_{SW}$ | PWM mode, $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 2A | | | 1.4 | | MHz |
| **Controller** | | | | | | | |
| Minimum On-Time | $t_{ON\_MIN}$ | | | | 75 | | ns |
| Minimum Off-Time | $t_{OFF\_MIN}$ | | | | 50 | | ns |
| Mode Forced PWM Threshold | $V_{M\_PWM}$ | $V_{IN}$ = 3.6V, $V_{EN}$ = 2V | | 1.2 | | | V |
| Mode PFM Threshold | $V_{M\_PFM}$ | $V_{IN}$ = 3.6V, $V_{EN}$ = 2V | | | | 0.4 | V |

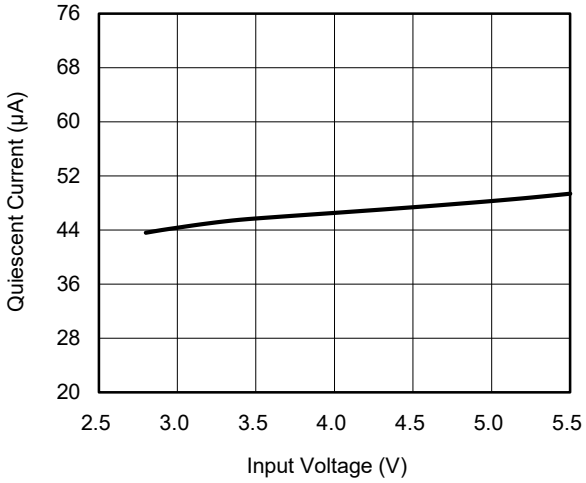
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

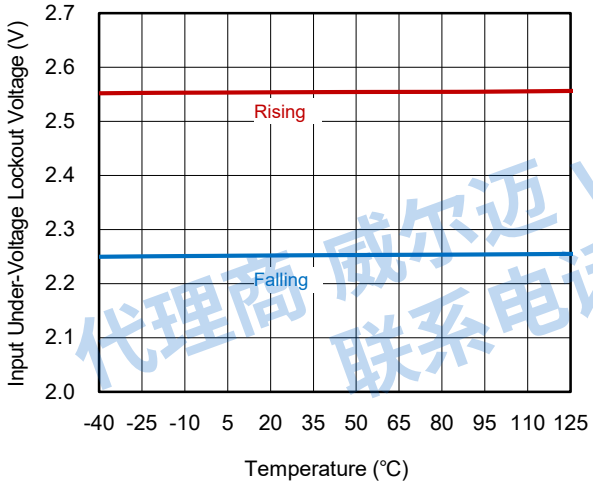
Quiescent Current vs. Temperature



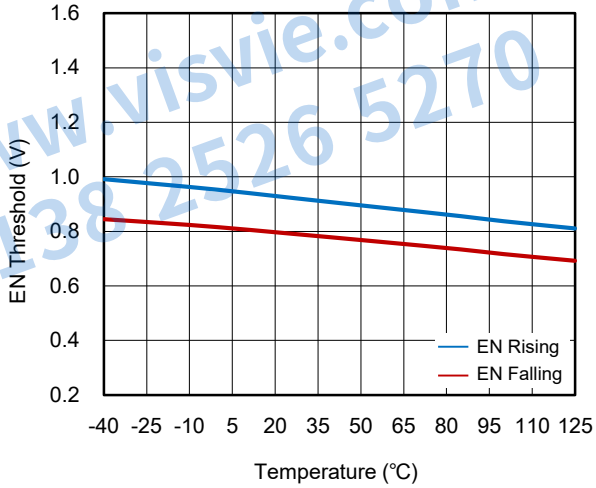

Quiescent Current vs. Input Voltage



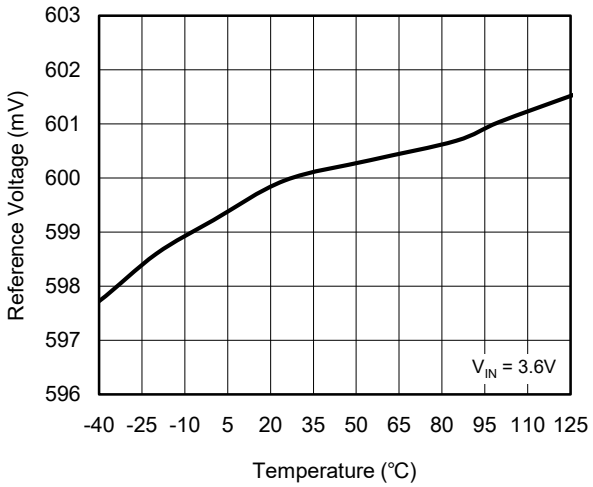

$V_{IN}$ UVLO vs. Temperature



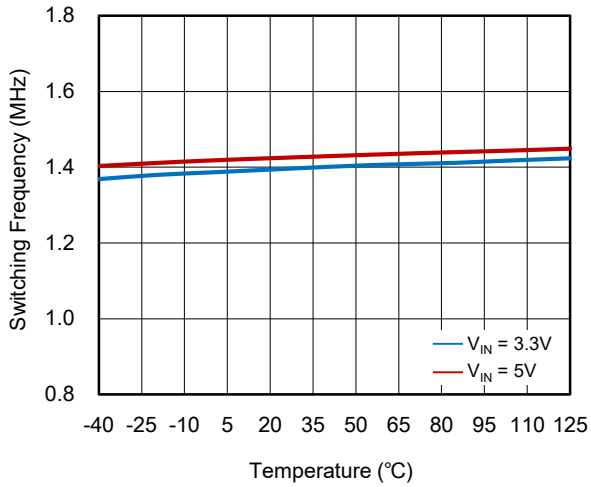

EN Threshold vs. Temperature




Reference Voltage vs. Temperature



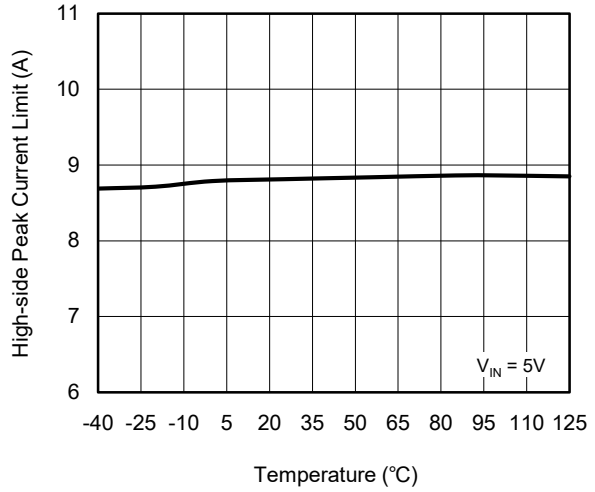

Switching Frequency vs. Temperature



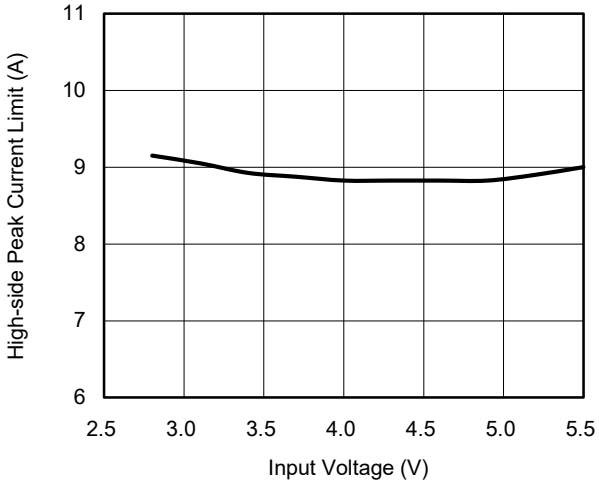
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

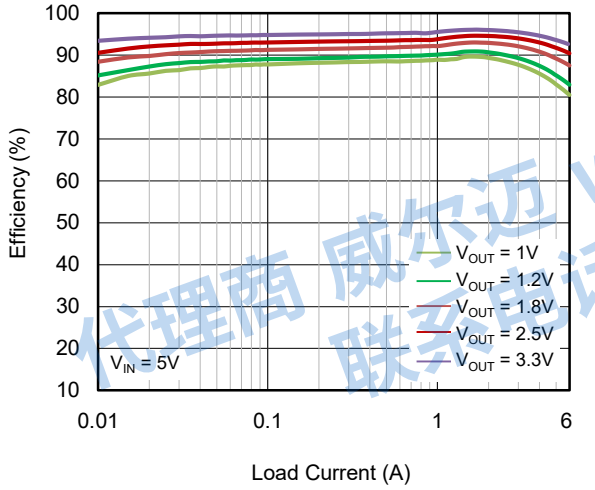
High-side Peak Current Limit vs. Temperature



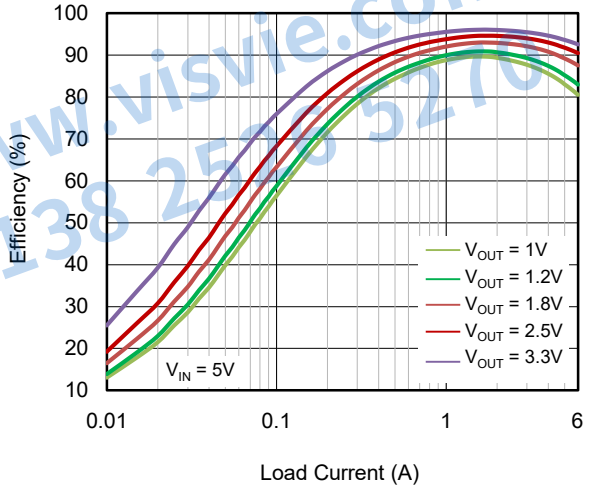

High-side Peak Current Limit vs. Input Voltage




Efficiency vs. Load Current (PFM)




Efficiency vs. Load Current (PWM)

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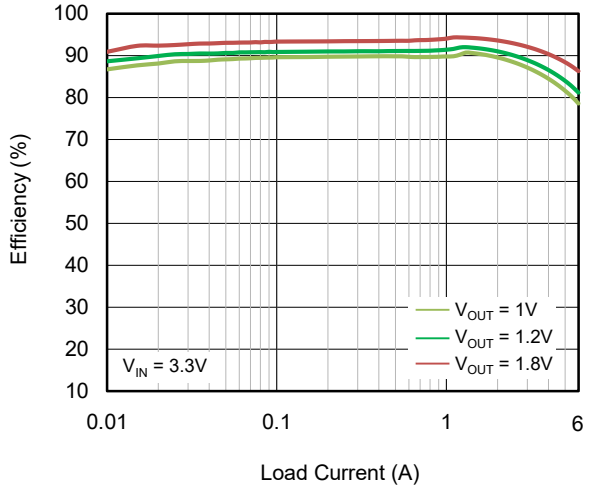
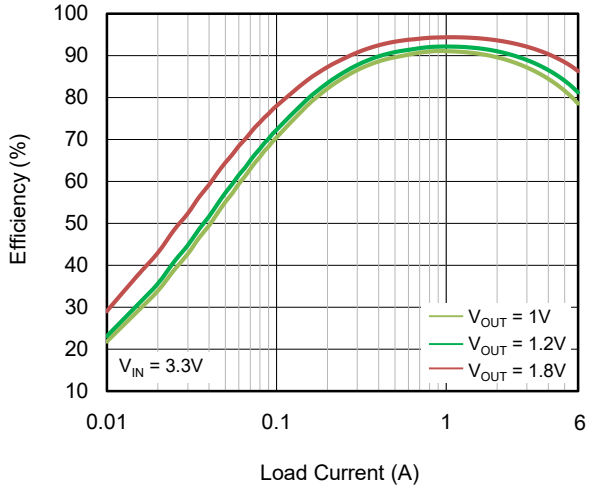


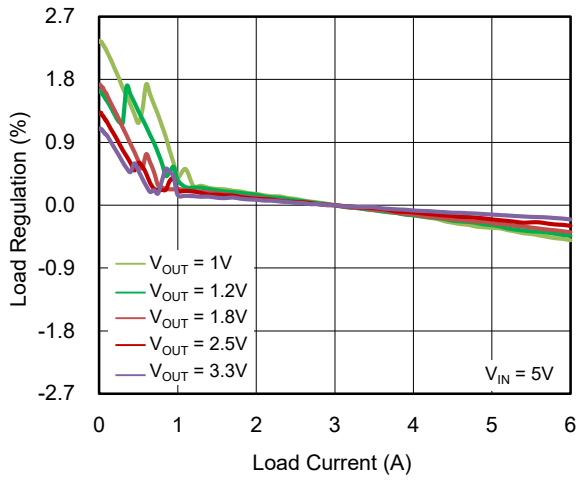

Efficiency vs. Load Current (PWM)



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

Load Regulation vs. Load Current (PFM)

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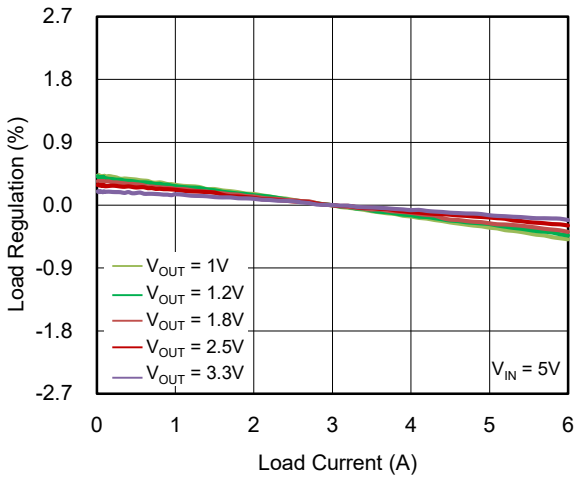
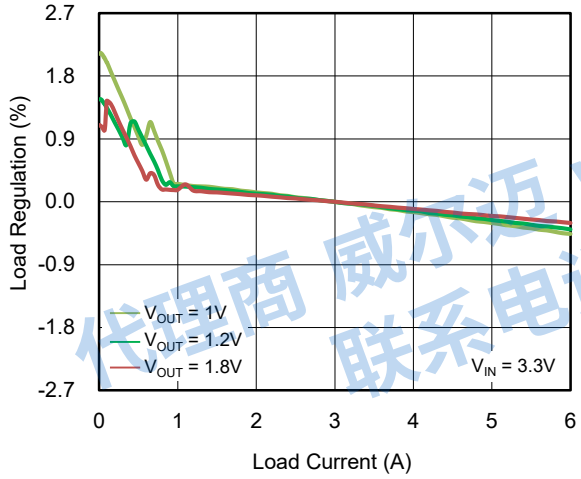
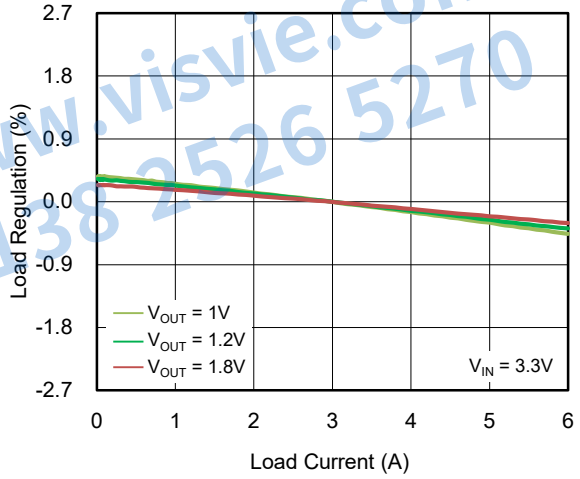


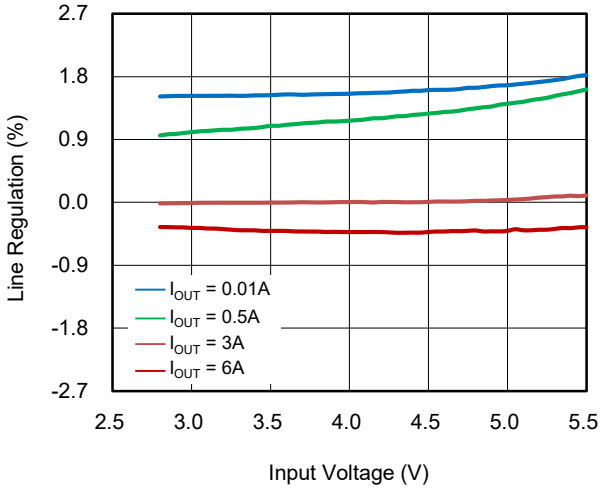

Load Regulation vs. Load Current (PFM)



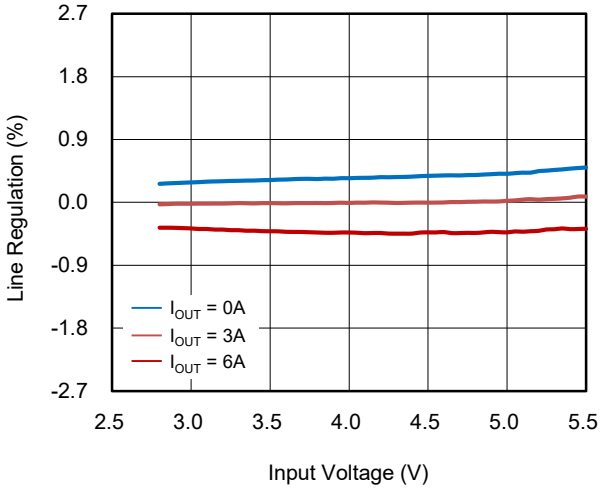

Load Regulation vs. Load Current (PWM)




Line Regulation vs. Input Voltage (PFM)



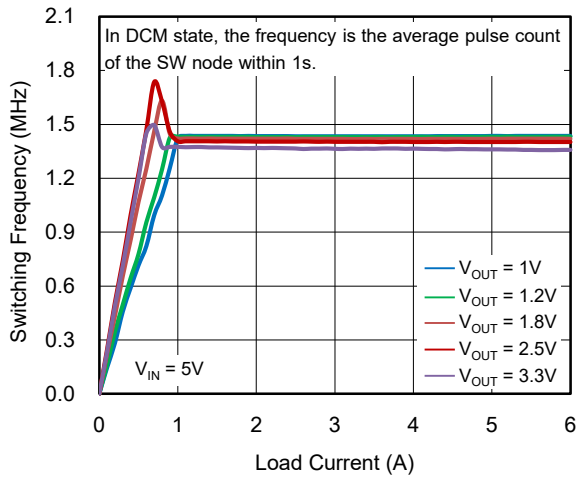

Line Regulation vs. Input Voltage (PWM)



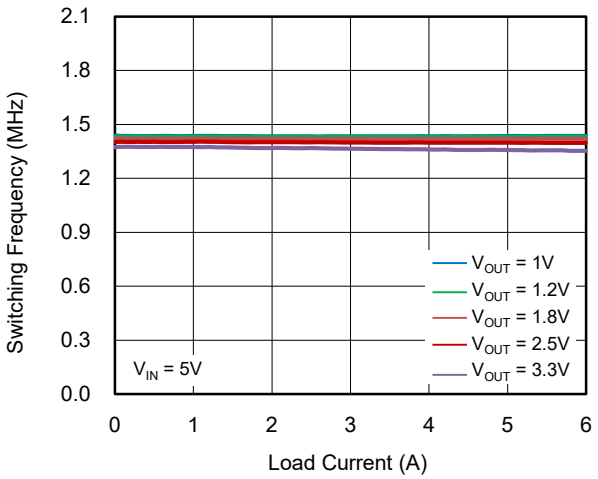
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

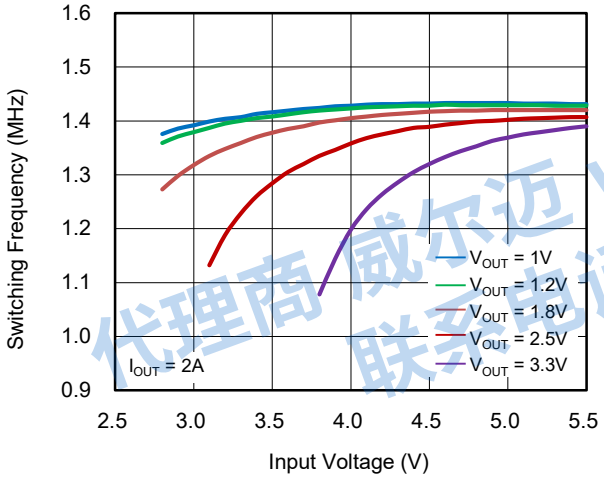
Switching Frequency vs. Load Current (PFM)



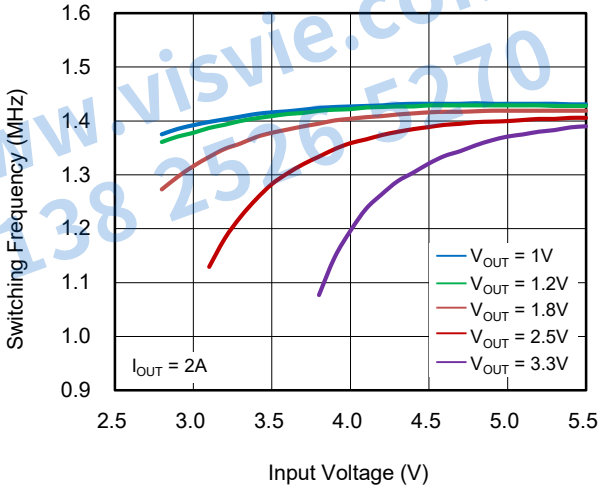

Switching Frequency vs. Load Current (PWM)



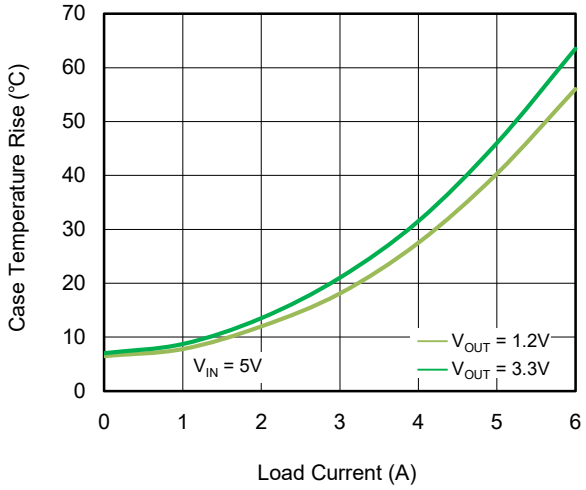

Switching Frequency vs. Input Voltage (PFM)



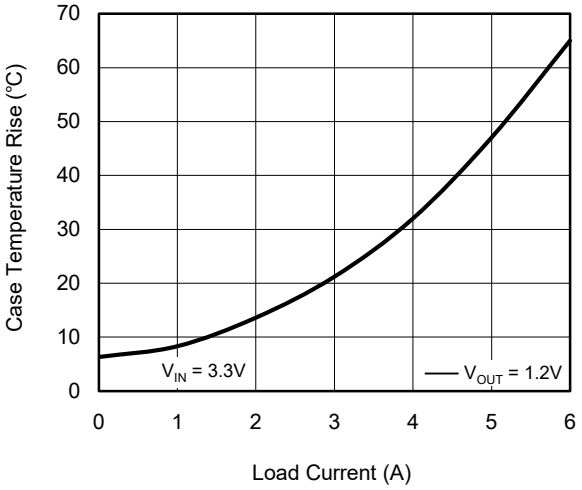

Switching Frequency vs. Input Voltage (PWM)




Case Temperature Rise vs. Load Current (1)




Case Temperature Rise vs. Load Current (1)



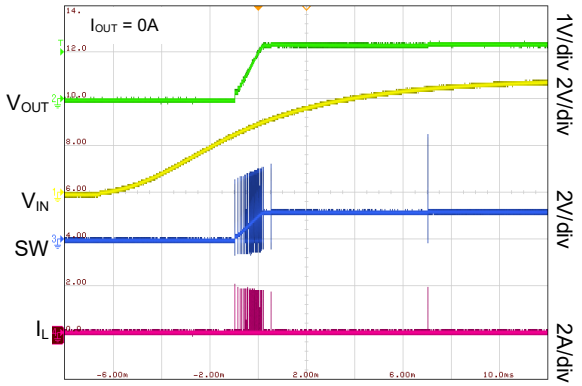



NOTE: 1. Demo board specifications: 75×75 mm², 4 layers, 1mm thickness. Copper thickness: outer layer 2 ounces, inner layer 0.5 ounces.

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

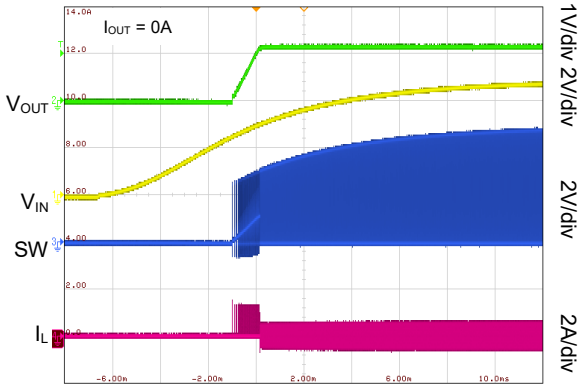
$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

Power Up (PFM)



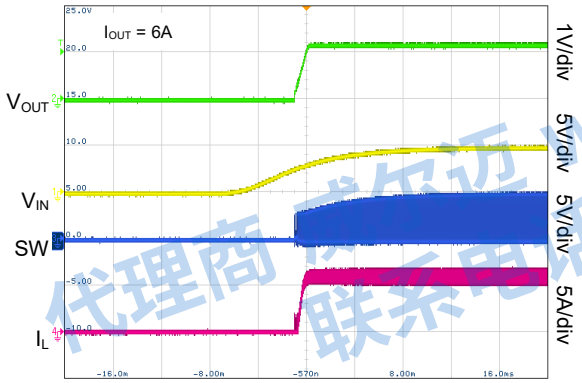

Time (2ms/div)

Power Up (PWM)



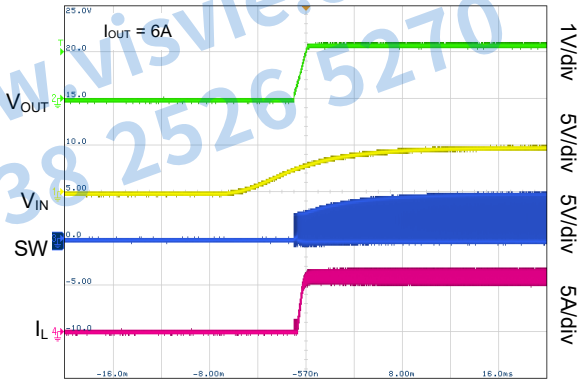

Time (2ms/div)

Power Up (PFM)



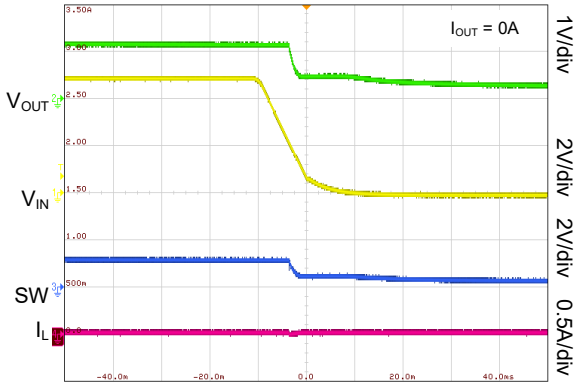

Time (4ms/div)

Power Up (PWM)



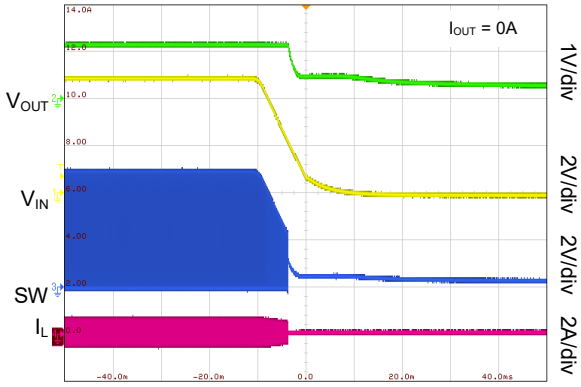

Time (4ms/div)

Power Off (PFM)




Time (10ms/div)

Power Off (PWM)

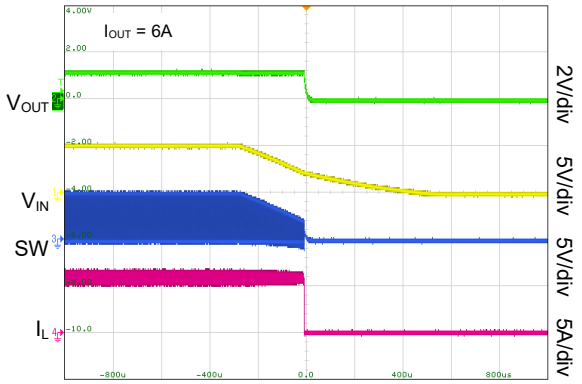



Time (10ms/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

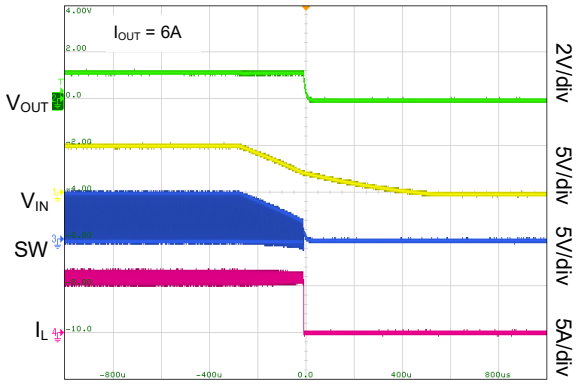
$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

Power Off (PFM)



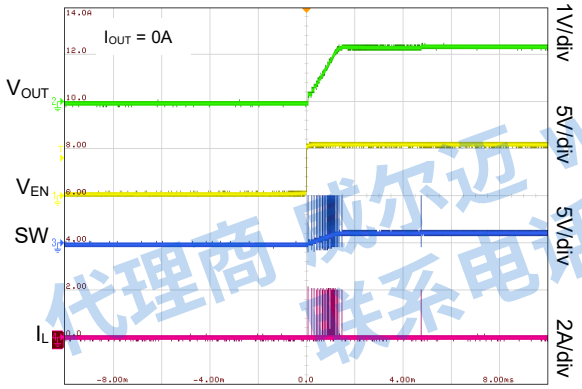

Time (200μs/div)

Power Off (PWM)



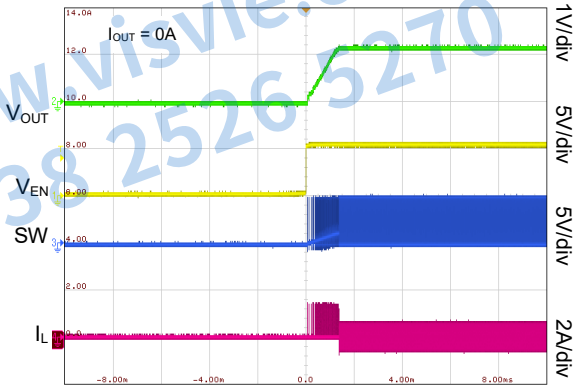

Time (200μs/div)

Enable On (PFM)



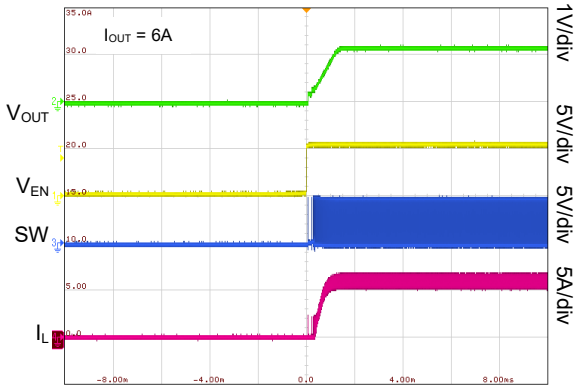

Time (2ms/div)

Enable On (PWM)



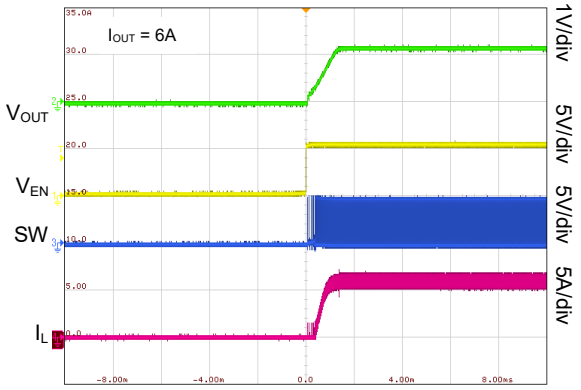

Time (2ms/div)

Enable On (PFM)




Time (2ms/div)

Enable On (PWM)

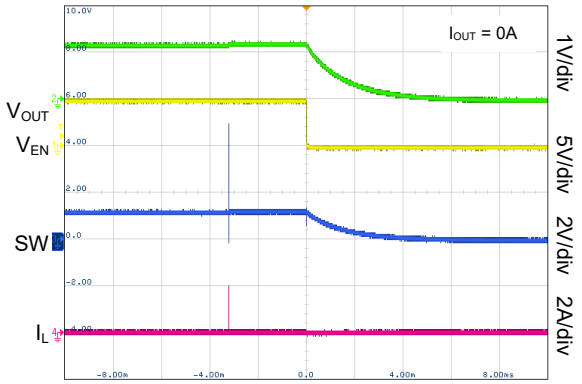



Time (2ms/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

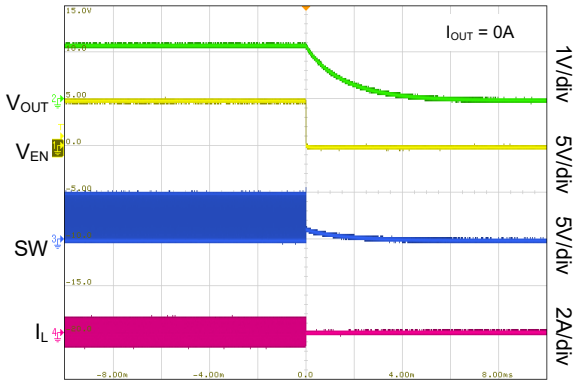
$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

Enable Shutdown (PFM)



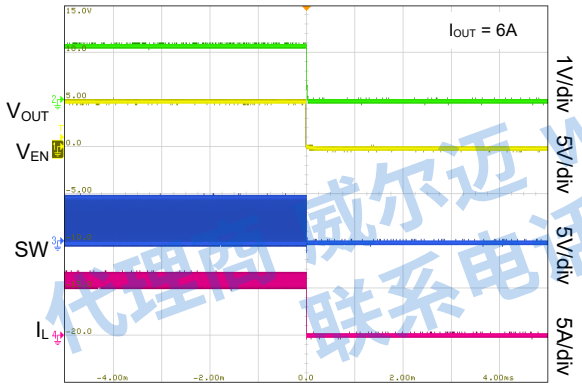

Time (2ms/div)

Enable Shutdown (PWM)




Time (2ms/div)

Enable Shutdown (PFM)

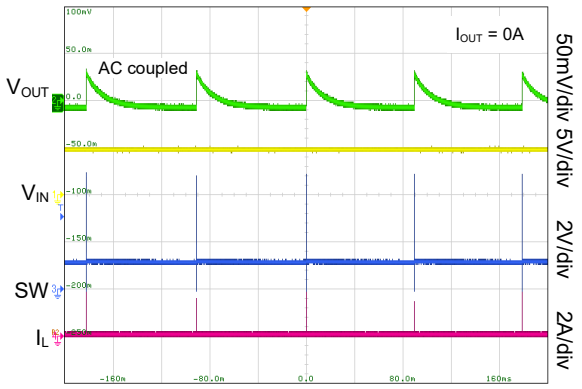



Time (1ms/div)

Enable Shutdown (PWM)

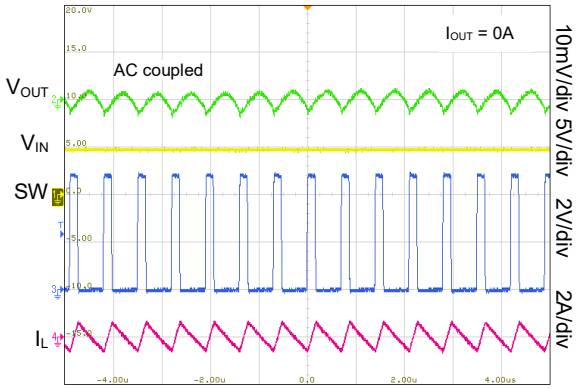

Time (1ms/div)

Steady State (PFM)




Time (40ms/div)

Steady State (PWM)

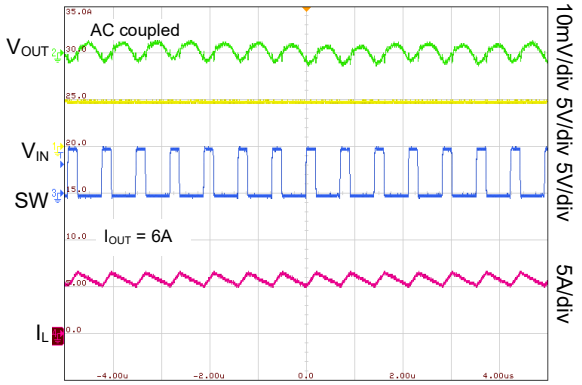



Time (1μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

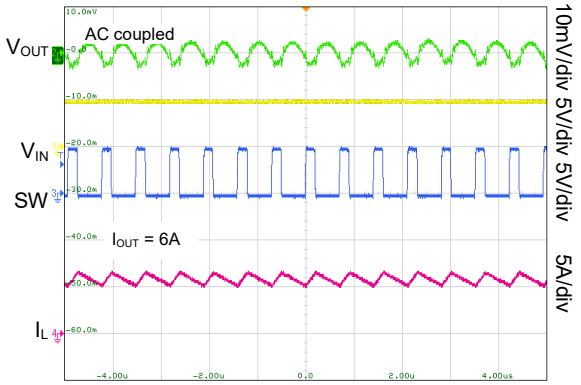
$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

Steady State (PFM)



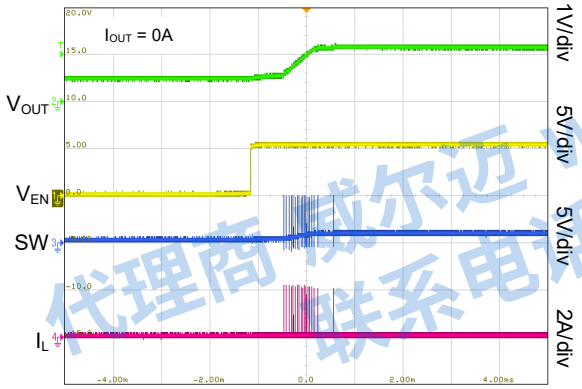

Time (1μs/div)

Steady State (PWM)



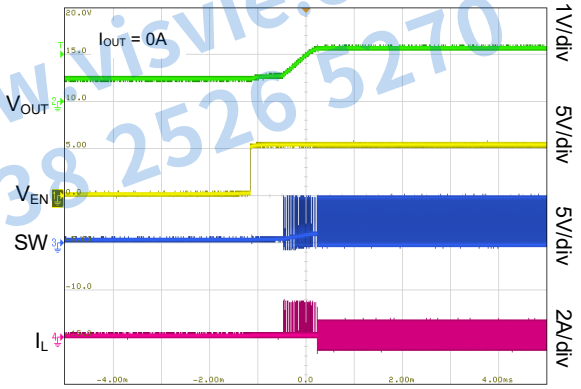

Time (1μs/div)

$V_{OUT}$ Pre-bias Startup (PFM)



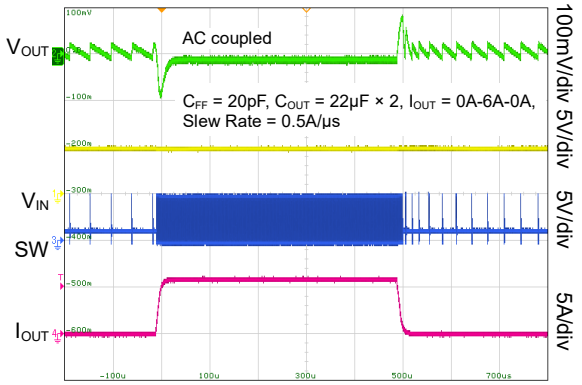

Time (1ms/div)

$V_{OUT}$ Pre-bias Startup (PWM)



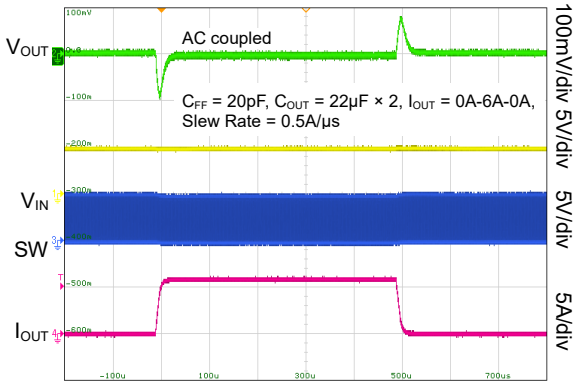

Time (1ms/div)

Load Transient (PFM)




Time (100μs/div)

Load Transient (PWM)

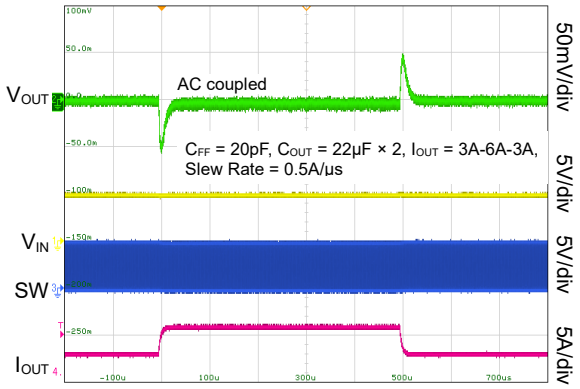



Time (100μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

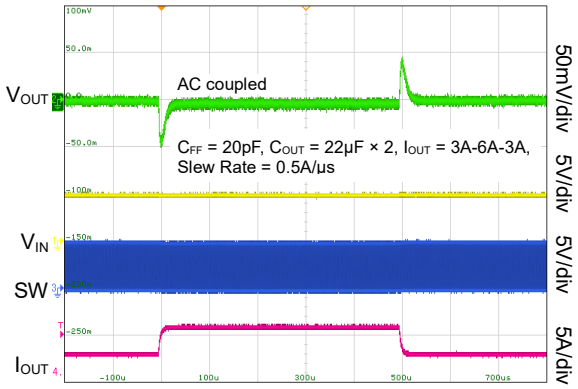
$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

Load Transient (PFM)



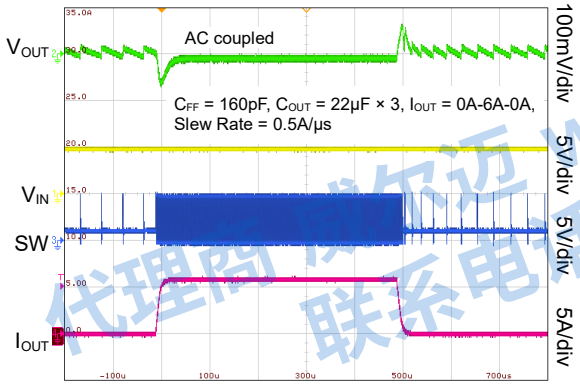

Time (100μs/div)

Load Transient (PWM)



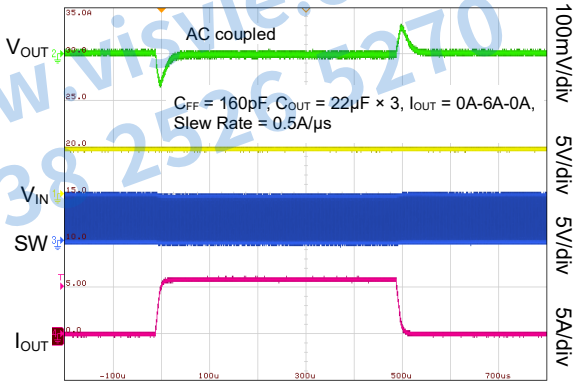

Time (100μs/div)

Load Transient (PFM)



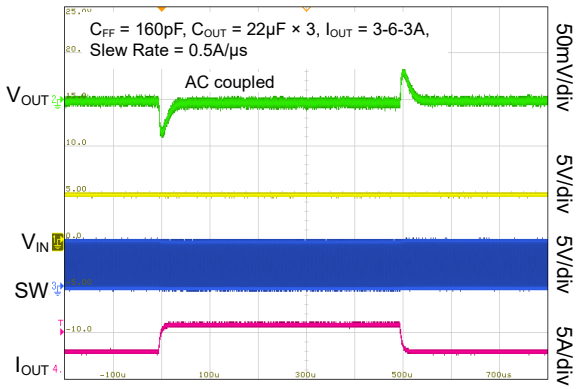

Time (100μs/div)

Load Transient (PWM)




Time (100μs/div)

Load Transient (PFM)




Time (100μs/div)

Load Transient (PWM)


Time (100μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $L_1$ = 0.47μH, DCR = 11mΩ, and $C_{OUT}$ = 22μF × 2, unless otherwise noted.

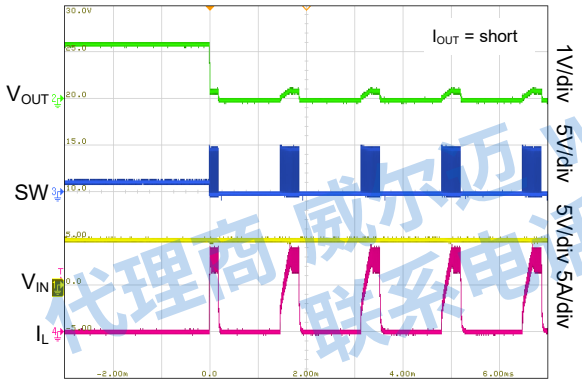
Hiccup with Output Short (PFM, Steady)


Time (1ms/div)

Hiccup with Output Short (PWM, Steady)

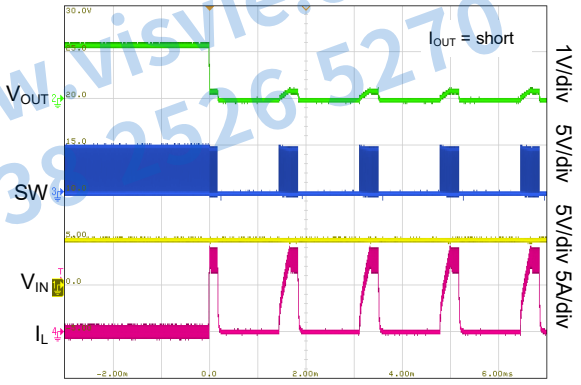

Time (1ms/div)

Hiccup with Output Short (PFM, Entry)



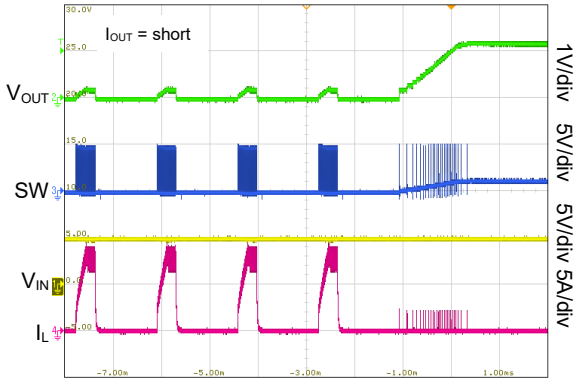

Time (1ms/div)

Hiccup with Output Short (PWM, Entry)



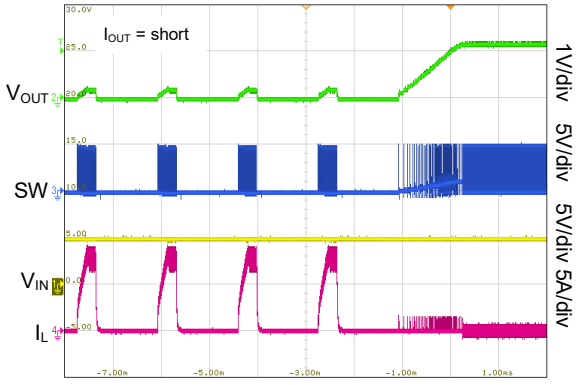

Time (1ms/div)

Hiccup with Output Short (PFM, Recover)




Time (1ms/div)

Hiccup with Output Short (PWM, Recover)




Time (1ms/div)

## FUNCTIONAL BLOCK DIAGRAM

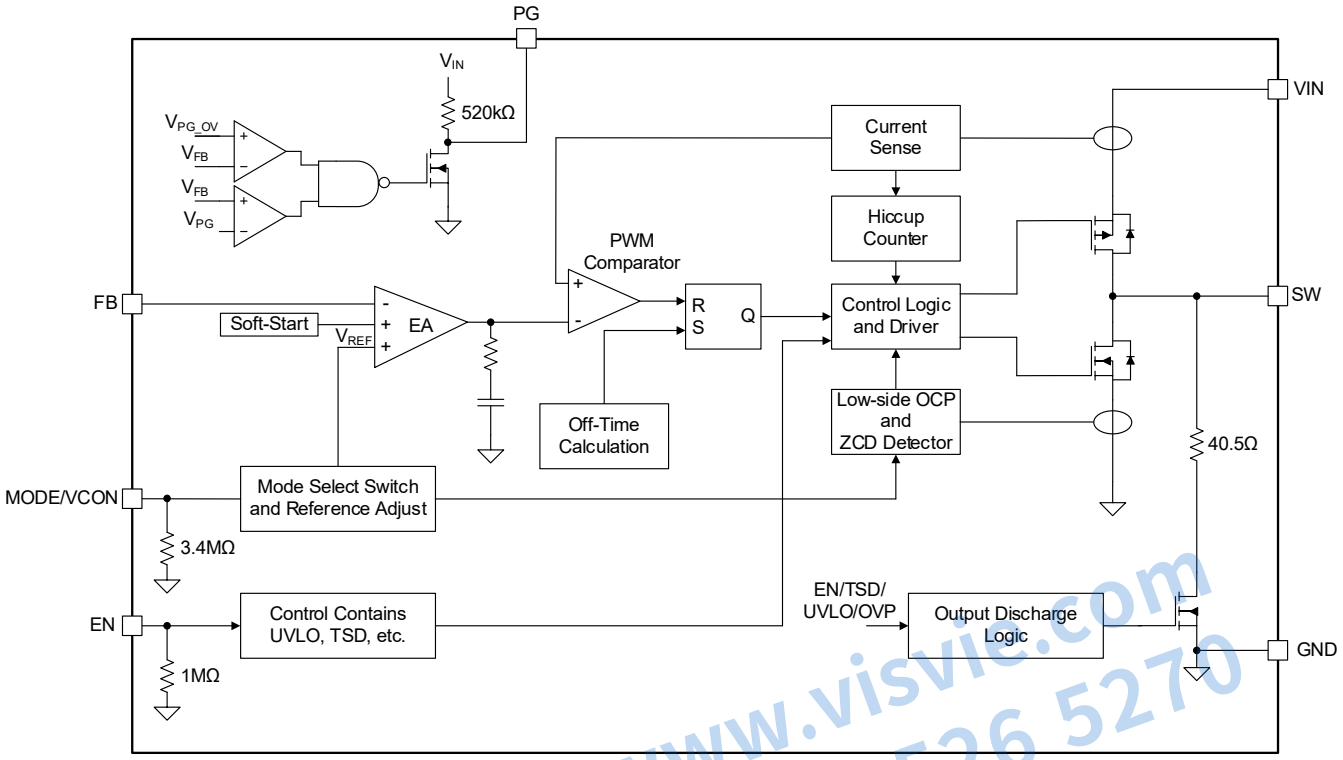



Figure 2. SGM61061 Block Diagram

# DETAILED DESCRIPTION

## Overview

The SGM61061 is a high efficiency synchronous Buck switching converter. The device operates in an adaptive off-time with peak current control scheme. The device operates at a typically 1.4MHz switching frequency to regulate the output voltage and uses the off-time PWM control for the moderate to heavy load currents. Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit sets the required off-time for the high-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current at PWM state.

## Under-Voltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, under-voltage lockout is implemented that shuts down the device when input voltage lower than $V_{UVLO}$ (when $V_{IN}$ voltage falls) with 300mV hysteresis. When the input voltage is higher than 2.55V, the device will recover to normal operation.

## Soft-Start and Pre-biased Output

A 1.3ms internal soft-start circuit is included to prevent input inrush current and input voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage ($V_{REF}$ = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61061 is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turning on, a bias on the output is likely to exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output voltage cannot drop too much during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device cannot be able to start up properly. The output ramp is automatically initiated to the bias voltage and ramps up to the nominal output value.

## Device Enable and Disable

The SGM61061 is enabled by setting the EN pin input to higher than 1.2V. It is disabled when EN pin falls lower than 0.4V. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the setting point voltage.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. The output discharge FET is turned on.

## Power Good Output (PG)

The SGM61061 has a power good output. The PG pin is pulled to high-level once FB voltage reaches 90% of the reference voltage, and is driven low once FB voltage falls below typically 85% of the reference voltage. If the FB voltage is higher than 115% of the reference voltage, the PG pin becomes low, then the FB voltage is reduced to 110% of the reference voltage, and the PG pin is pulled to the high-level. The PG pin is an open-drain output with internal pull-up resistor connected to $V_{IN}$. It is recommended that the sink current should not exceed 1mA. There is a 150μs delay between when $V_{FB}$ reaches PG threshold to when the PG pin is pulled to high. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

**Table 1. PG Output State in Different Conditions**

| Reason | Conditions | PG State | |
|---|---|---|---|
| | | High | Low |
| FB Voltage | EN = High, $V_{PG\_OV} \geq V_{FB} \geq V_{PG}$ | √ | |
| | EN = High, $V_{FB} < V_{PG}$ | | √ |
| | EN = High, $V_{FB} > V_{PG\_OV}$ | | √ |
| Shutdown by EN | EN = Low | | √ |
| Thermal Shutdown | $T_J > T_{JSD}$ | | √ |
| UVLO (1) | $1V < V_{IN} < V_{UVLO}$ | | √ |
| Power Supply Removal (1) | $V_{IN} \leq 1V$ | Uncertainty | |

NOTE: 1. PG pin is connected to VIN pin with an external 510kΩ resistor.

## DETAILED DESCRIPTION (continued)

### Power-Save Mode

At light load conditions, the SGM61061 shifts to the power-save mode to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in power-save mode. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal value again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

### Low Dropout Operation (100% Duty Cycle)

When the input voltage gradually drops to the regulation output voltage, the SGM61061 can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

$V_{IN\_MIN}$ is minimum input voltage to maintain output voltage in regulation.
$I_{OUT\_MAX}$ is maximum output current.
$R_{DSON}$ is high-side MOSFET on-resistance.
$R_L$ is inductor DC resistance (DCR).

### Mode Switch and Output Voltage Dynamic Regulation

This device can switch between PWM and PFM work modes. SGM61061 switches to PWM mode if the MODE/VCON pin voltage is more than 1.2V. Once MODE/VCON pin voltage falls below 0.4V or floats, SGM61061 will switch to PFM mode which keeps the high efficiency in the whole load range. Although the efficiency is low when load is light in PWM mode, the $V_O$ ripple is low and the frequency is relatively fixed.

When output voltage need to change in operation, it can be regulated by MODE/VCON pin. Internal reference voltage will increase linearly with MODE/VCON pin voltage changes from 0.6V to 1.1V, as Figure 3. It should be noted that if this function is used, the VCON pin must to be powered first. Output voltage changes without changing external resistor divider and SGM61061 will switch to PWM mode. The accuracy is 3% typically and the range of VREF voltage regulation is from 0.35V to 0.6V in VCON function. The accuracy is 10% typically when reference voltage changes from 0.1V to 0.35V. The reference voltage can be calculated by Equation 2:

$$V_{REF} = 0.985 \times V_{CON} - 0.486V \quad (2)$$

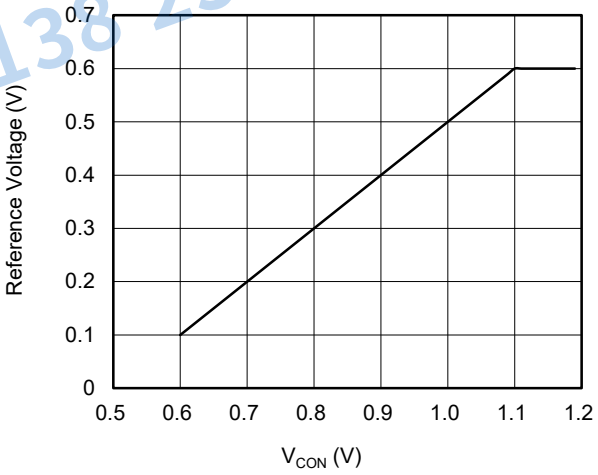



**Figure 3. Reference Voltage Relation to the VCON**

## DETAILED DESCRIPTION (continued)

### Current Limit and Hiccup Mode Short-Circuit Protection

The switch current limit avoids high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The SGM61061 keeps sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off. After keeping for 30μs (TYP), low-side current limit circuit is enabled and shield the adaptive off-time circuit. The on-time of the low-side switch is determined by the inductor, the output voltage and the value of the low-side current limit.

If the current limit persists uninterrupted for more than 64 cycles, the device stops switching and turns the output discharge circuit on. A new soft-start is initiated automatically (hiccup) after 1.2ms (TYP). The hiccup repeats until the overload or short-circuit fault is cleared.

### Negative Current Limit

In PFM mode, the low-side MOSFET will be turned off once the low-side current fall to $I_{ZCD}$ to maintain high efficiency at light load. However in PWM mode, the $I_{ZCD}$ changed to negative current, which is define as negative current limit ($I_{LIM\_LN}$). When the input and output conditions are unchanged, if the low-side current drops to $I_{LIM\_LN}$, the low-side MOSFET will be turned off in advance, then the high-side MOSFET is turned on.

### Output Over-Voltage Protection (OVP)

The device contains an over-voltage protection circuit to avoid high overshoots of the output voltage during operation. Usually an OVP occurs after removal of an overload condition. Upon removal of the overload condition, the regulator output rises quickly because the high inductor current charges the output capacitor rapidly, especially if $C_{OUT}$ is small. The error amplifier will respond and re-adjust itself but not as fast as the output filter (LC) and an overshoot occurs.

To minimize the overshoots, the device monitors the FB pin voltage and compares it to the internal OVP threshold. OVP is triggered while the FB voltage rising above 115% of reference voltage, and is released while the FB voltage falls below typically 110% of reference voltage. In PFM mode, the switching stops and discharge circuit is turned on at OVP protection. In PWM mode, discharge circuit is turned on and high-side MOSFET is kept off, low-side MOSFET is turned on once every 40μs (TYP). Every time a low-side MOSFET is on, it is turned off when the current flowing through it reaches the negative current limit. When the FB voltage drops below the OVP threshold, the discharge circuit and low-side MOSFET is turned off and high-side MOSFET can be turned on again in the next cycle.

### Output Discharge Function

If the device is in any of the following states: UVLO, shutdown by EN, OTP, or OVP, an internal output discharge FET is turned on and discharges the output through the SW pin smoothly, the resistance of discharge FET is about 40.5Ω (TYP).

### Thermal Shutdown

Thermal protection is designed to protect the die against overheating damage. If the junction temperature exceeds $T_{JSD}$ threshold, the switching stops and the device shuts down. Automatic recovery with a soft-start will begin when the junction temperature drops below the +130℃ falling threshold.

# APPLICATION INFORMATION

In this section, power supply design with the SGM61061 synchronous Buck converter and selection of the external components will be explained based on the typical application that is applicable for various input and output voltage combinations.

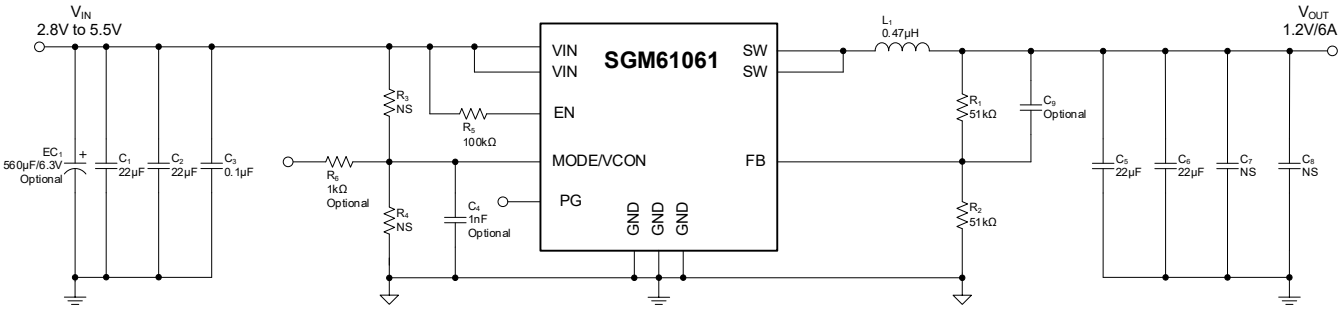



**Figure 4. SGM61061 Circuit for 1.2V Output**

## Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 4. The selected components are given in Table 3.

**Table 2. Design Parameters for the Application Example**

| Design Parameter | Example Value |
|---|---|
| Input Voltage | 2.8V to 5.5V |
| Output Voltage | 1.2V |
| Output Current | ≤ 6A |

**Table 3. Selected Components for the Design Example**

| Ref | Description | Manufacturer |
|---|---|---|
| $C_1$, $C_2$, $C_5$, $C_6$ | 22μF, 16V, X5R, 0805, Ceramic | Standard |
| $C_3$ | 0.1μF, 16V, X7R, 0603, Ceramic | Standard |
| $C_4$ | 1nF, 25V, X7R, 0603, Ceramic, Optional | Standard |
| $C_9$ | 20pF, 50V, C0G, 0603, Ceramic, Optional | Standard |
| $L_1$ | 0.47μH, DCR = 11mΩ, $I_{SAT(20\%)}$ = 14.5A, $I_{RMS(\Delta T = 40K)}$ = 6.8A, SRF = 122MHz, 4mm × 4mm × 1.8mm, P/N: 744373240047 | Wurth |
| $R_1$, $R_2$ | 51kΩ, 1%, 0603, 1/16W Chip Resistor | Standard |
| $R_5$ | 100kΩ, 1%, 0603, 1/16W Chip Resistor | Standard |
| $R_6$ | 1kΩ, 1%, 0603, 1/16W Chip Resistor, Optional | Standard |

NOTE: $R_6$ and $C_4$ are recommended when the VCON voltage regulator function is used. If the long input power cable is used, or the input voltage is on/off by air-break switch, $EC_1$ should be installed.

## Input Capacitor Selection ($C_{IN}$)

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. In most cases, two 22μF input capacitors are recommended, a larger value reduces input voltage ripple and improve system stability. Usually a 0.1μF low ESR ceramic capacitor needs to be connected between the VIN and GND pins as closely as possible.

## Inductor Selection (L)

The important factors for inductor selection are inductance (L), saturation current ($I_{SAT}$), RMS rating ($I_{RMS}$), DC resistance (DCR) and dimensions. Use Equation 3 to find the inductor peak current ($I_{L\_MAX}$) and peak-to-peak ripple current ($\Delta I_L$) in static conditions:

$$I_{L\_MAX} = I_{O\_MAX} + \frac{\Delta I_L}{2}$$
$$\Delta I_L = V_{OUT} \times \frac{1-D}{L \times f_{SW}} \quad (3)$$

$I_{O\_MAX}$ is the maximum load current, $D = V_{OUT}/V_{IN}$ represents duty cycle and $f_{SW}$ is the switching frequency.

Typically, the peak-to-peak inductor current is selected between 10% and 30% of the maximum output current. The inductor of that the saturation current is 20% high than $I_{L\_MAX}$ is recommended. The inductor initial tolerance can be as high as -20% to +20% of the nominal value and proper current derating is usually required. More generally, choosing the saturation current above high-side limit is enough. It should be noted that low-side current should avoid falling to negative current limit when no load in PWM mode. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Larger inductance values reduce the ripple current but lead to sluggish transient response. $L_1$ = 0.47μH is the recommended values for the typical application.

# APPLICATION INFORMATION (continued)

## Output Capacitor Selection ($C_{OUT}$)

The architecture of the SGM61061 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep the resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Bias voltage can cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. $C_{OUT}$ = 2 × 22μF is the recommended values for the typical application.

## Output Voltage Setting

Use Equation 4 to select the $R_1/R_2$ resistor divider to set the $V_{OUT}$. The parasitic capacitance of the FB pin and $R_1$ form a low-pass filter, which can effectively filter out high-frequency interference input from the FB pin. However, it also adds a pole to the control loop, and if the frequency of this pole is too low, the stability of the system will be reduced.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (4)$$

The recommended resistors values for common output voltages are listed in Table 4.

**Table 4. Resistor Values for Common Output Voltages**

| $V_{OUT}$ (V) | $R_1$ (kΩ) | $R_2$ (kΩ) | $C_9$ (pF), Optional |
|---|---|---|---|
| 0.6 | 51 (1%) | NC | NC |
| 1.2 | 51 (1%) | 51 (1%) | 20 |
| 3.3 | 232 (1%) | 51 (1%) | 10 |

NOTE: The value of $C_9$ needs to match the value of $R_1$ and $R_2$.

## Load Transient Optimization

A feed-forward capacitor ($C_9$) reduces the output ripple in PSM and improves the load transient response. If it is necessary to reduce the drop of output voltage at load transient, the response speed of the system can be improved by increasing the $C_{FF}$ ($C_9$) capacitance value. However, excessive $C_{FF}$ ($C_9$) capacitance will reduce the stability of the system, which can be compensated by increasing the output capacitance value.



# ADDITIONAL TYPICAL APPLICATION CIRCUITS

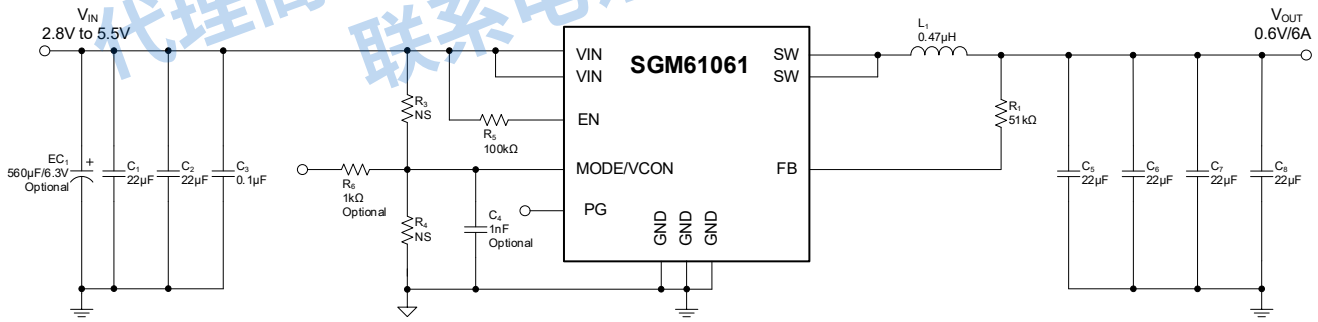



**Figure 5. Additional Typical Application with 0.6V $V_{OUT}$**

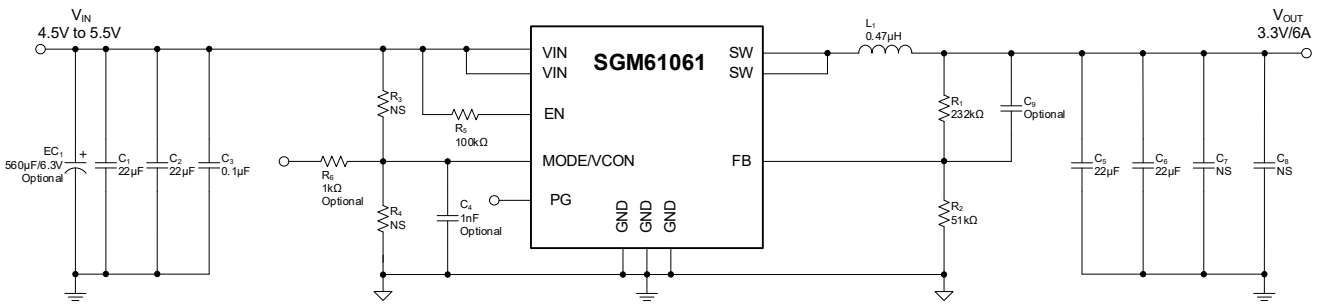


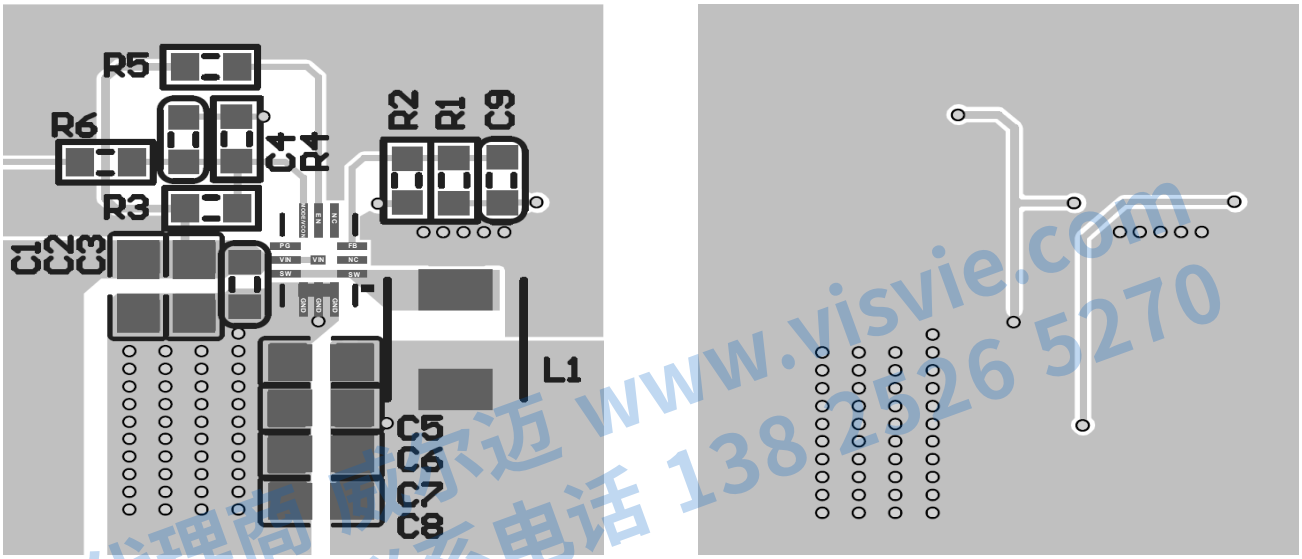

**Figure 6. Additional Typical Application with 3.3V $V_{OUT}$**

## Layout Guidelines

A good printed-circuit-board (PCB) layout is a critical element of any high-performance design. Follow the guidelines below for designing a good layout for the SGM61061.

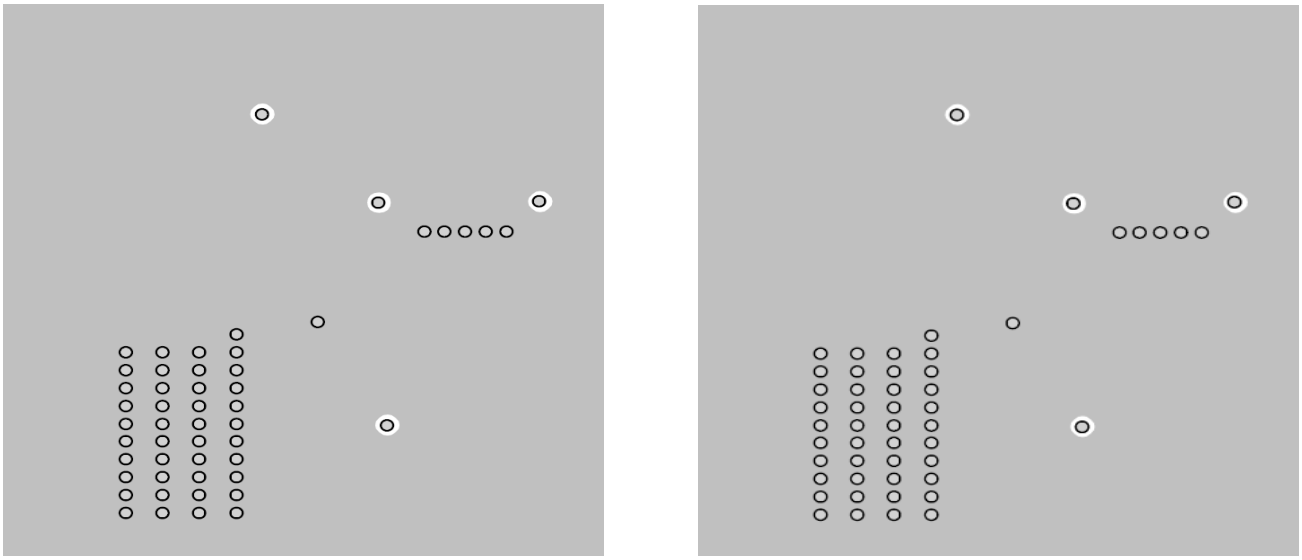
- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device GND pin to minimize the AC current loops.
- Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep the signal traces like the FB sense line away from SW or other noisy sources.
- Use GND planes in middle layers for shielding and minimizing the ground potential drifts.

Refer to Figure 5 to Figure 6 for a recommended PCB layout.




Top Layer Bottom Layer

Figure 7. Top Layer and Bottom Layer



Middle Layer1 Middle Layer2

Figure 8. Middle Layer and Middle Layer

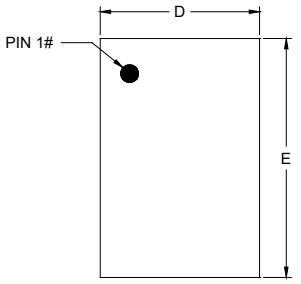
# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

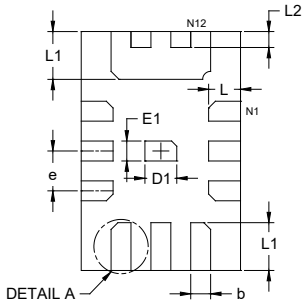
| Changes from Original (NOVEMBER 2023) to REV.A | Page |
|---|---|
| Changed from Product Preview to Production Data | All |

# PACKAGE OUTLINE DIMENSIONS

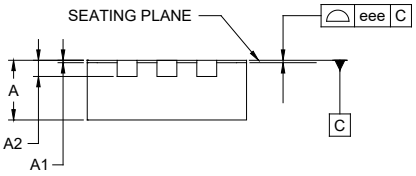
## TQFN-2×3-12L




TOP VIEW

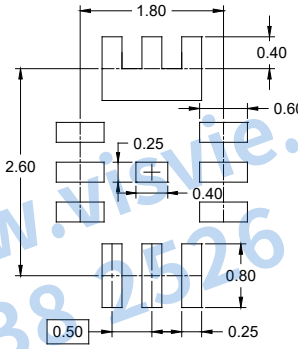



BOTTOM VIEW




SIDE VIEW


**DETAIL A**
ALTERNATE TERMINAL CONSTRUCTION




**RECOMMENDED LAND PATTERN** (Unit: mm)

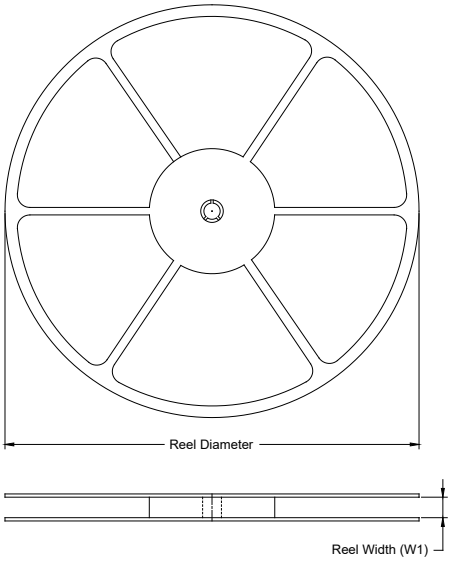


| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | 0.700 | - | 0.800 |
| A1 | 0.000 | - | 0.050 |
| A2 | 0.203 REF | | |
| b | 0.200 | - | 0.300 |
| D | 1.900 | - | 2.100 |
| E | 2.900 | - | 3.100 |
| D1 | 0.300 | - | 0.500 |
| E1 | 0.150 | - | 0.350 |
| e | 0.500 BSC | | |
| L | 0.300 | - | 0.500 |
| L1 | 0.500 | - | 0.700 |
| L2 | 0.200 REF | | |
| eee | 0.080 | | |

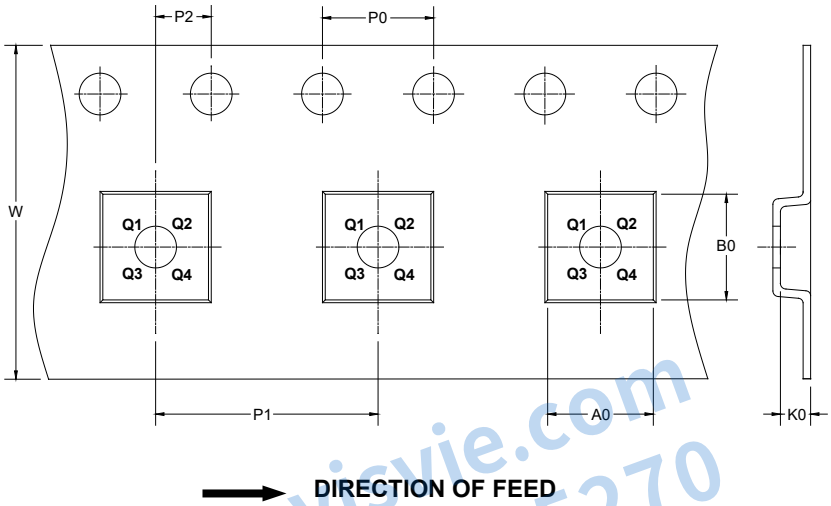
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

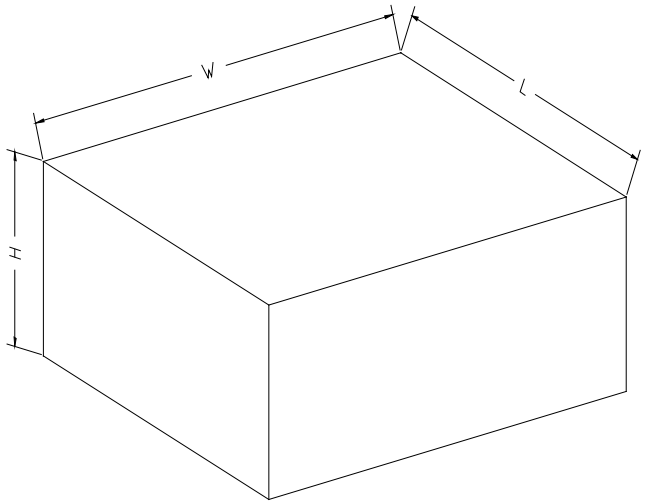


## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TQFN-2×3-12L | 7" | 9.5 | 2.30 | 3.20 | 1.00 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002