

PCA9546A Low Voltage 4-Channel I²C and SMBus Switch with Reset Function

1 Features

- 1-of-4 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Active-Low Reset Input
- Three Address Pins, Allowing up to Eight PCA9546A Devices on the I²C Bus
- Channel Selection Via I²C Bus, in Any Combination
- Power-up With All Switch Channels Deselected
- Low R_{ON} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA Per JESD 78
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I²C Slave Address Conflicts (For Example, Multiple, Identical Temp Sensors)

3 Description

The PCA9546A is a quad bidirectional translating switch controlled via the I²C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SC_n/SD_n channel or combination of channels can be selected, determined by the contents of the programmable control register.

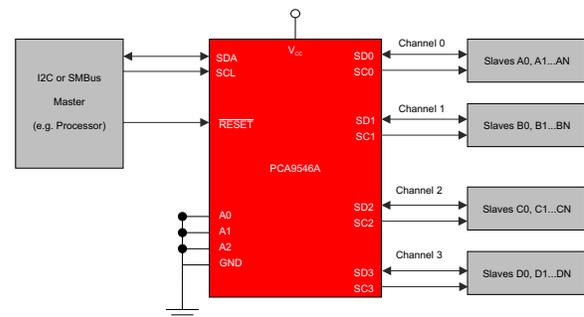
An active-low reset ($\overline{\text{RESET}}$) input allows the PCA9546A to recover from a situation in which one of the downstream I²C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V_{CC} pin can be used to limit the maximum high voltage, which will be passed by the PCA9546A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5-V tolerant.

Packaging Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
PCA9546A	SOIC (D) (16)	9.90 mm x 3.91 mm
	TVSOP (DGV) (16)	3.60 mm x 4.40 mm
	SOIC (DW) (16)	10.3 mm x 7.50 mm
	TSSOP (PW) (16)	5.00 mm x 4.40 mm
	VQFN (RGV) (16)	4.00 mm x 4.00 mm
	VQFN (RGY) (16)	4.50 mm x 3.50 mm

- (1) For all available packages, see the orderable addendum at the end of the datasheet.



Copyright © 2016, Texas Instruments Incorporated

Simplified Application Diagram

Table of Contents

1 Features	1	8.4 Device Functional Modes.....	11
2 Applications	1	8.5 Programming.....	11
3 Description	1	8.6 Control Register.....	14
4 Revision History	2	9 Application Information Disclaimer	16
5 Pin Configuration and Functions	3	9.1 Application Information.....	16
6 Specifications	4	9.2 Typical Application.....	16
6.1 Absolute Maximum Ratings.....	4	10 Power Supply Recommendations	19
6.2 ESD Ratings.....	4	10.1 Power-On Reset Requirements.....	19
6.3 Recommended Operating Conditions.....	4	11 Layout	21
6.4 Thermal Information.....	4	11.1 Layout Guidelines.....	21
6.5 Electrical Characteristics.....	5	11.2 Layout Example.....	21
6.6 I ² C Interface Timing Requirements.....	6	12 Device and Documentation Support	22
6.7 Interrupt and Reset Timing Requirements.....	7	12.1 Receiving Notification of Documentation Updates.....	22
6.8 Switching Characteristics.....	7	12.2 Support Resources.....	22
7 Parameter Measurement Information	8	12.3 Trademarks.....	22
8 Detailed Description	10	12.4 Electrostatic Discharge Caution.....	22
8.1 Overview.....	10	12.5 Glossary.....	22
8.2 Functional Block Diagram.....	10	13 Mechanical, Packaging, and Orderable Information	22
8.3 Feature Description.....	11		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2021) to Revision I (June 2022)	Page
• Changed TSSOP (PW) (16) From: 9.70 mm x 4.40 mm To: 5.00 mm x 4.40 mm in the <i>Packaging Information</i> table.....	1

Changes from Revision G (May 2016) to Revision H (March 2021)	Page
• Changed the <i>Packaging Information</i> table.....	1
• Moved the Package thermal impedance to the <i>Thermal Information</i> table.....	4
• Added the <i>Thermal Information</i> table.....	4
• Changed the V _{PORR} row in the <i>Electrical Characteristics</i>	5
• Added V _{PORF} row to the <i>Electrical Characteristics</i>	5
• Changed the I _{CC} Low inputs and High inputs values in the <i>Electrical Characteristics</i>	5
• Changed the R _{on} (4.5 V to 5.5 V) TYP value From: 9 Ω To: 10 Ω in the <i>Electrical Characteristics</i>	5
• Changed the R _{on} (3 V to 3.6 V) TYP value From: 11 Ω To: 13 Ω in the <i>Electrical Characteristics</i>	5
• Changed the <i>Power Supply Recommendations</i>	19

Changes from Revision F (April 2014) to Revision G (May 2016)	Page
• Revised pack material addendum; pin 1 quadrant	22

Changes from Revision E (January 2008) to Revision F (April 2014)	Page
• Added $\overline{\text{RESET}}$ Errata section.....	11

5 Pin Configuration and Functions

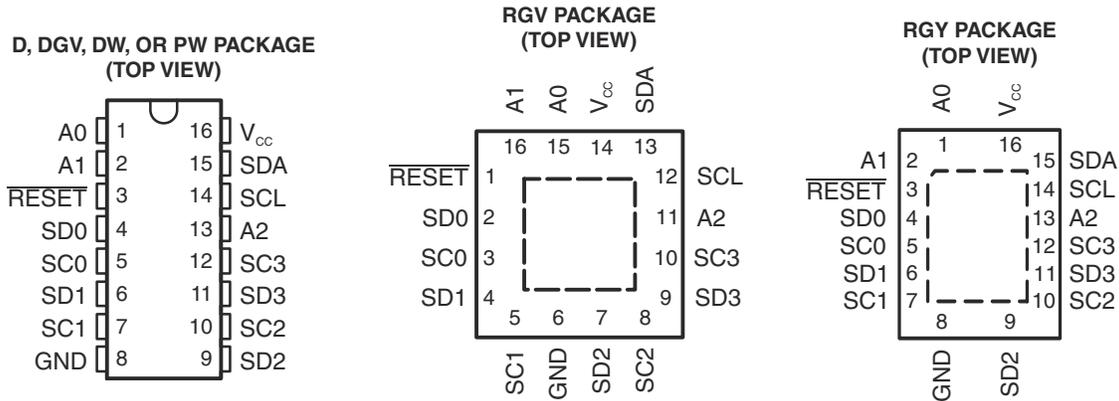


Table 5-1. Pin Functions

NAME	PIN NO.		DESCRIPTION
	D, DGV, DW, PW, AND RGY	RGV	
A0	1	15	Address input 0. Connect directly to V _{CC} or ground
A1	2	16	Address input 1. Connect directly to V _{CC} or ground
A2	13	11	Address input 2. Connect directly to V _{CC} or ground
GND	8	6	Ground
RESET	3	1	Active low reset input. Connect to V _{DPUM} ⁽¹⁾ through a pull-up resistor, if not used.
SD0	4	2	Serial data 0. Connect to V _{DPU0} ⁽¹⁾ through a pull-up resistor
SC0	5	3	Serial clock 0. Connect to V _{DPU0} ⁽¹⁾ through a pull-up resistor
SD1	6	4	Serial data 1. Connect to V _{DPU1} ⁽¹⁾ through a pull-up resistor
SC1	7	5	Serial clock 1. Connect to V _{DPU1} ⁽¹⁾ through a pull-up resistor
SD2	9	7	Serial data 2. Connect to V _{DPU2} ⁽¹⁾ through a pull-up resistor
SC2	10	8	Serial clock 2. Connect to V _{DPU2} ⁽¹⁾ through a pull-up resistor
SD3	11	9	Serial data 3. Connect to V _{DPU3} ⁽¹⁾ through a pull-up resistor.
SC3	12	10	Serial clock 3. Connect to V _{DPU3} ⁽¹⁾ through a pull-up resistor
SCL	14	12	Serial clock line. Connect to V _{DPUM} ⁽¹⁾ through a pull-up resistor
SDA	15	13	Serial data line. Connect to V _{DPUM} ⁽¹⁾ through a pull-up resistor
V _{CC}	16	14	Supply power

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I²C reference voltage while V_{DPU0} - V_{DPU3} are the slave channel reference voltages.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
V _I	Input voltage ⁽²⁾	-0.5	7	V
I _I	Input current		±20	mA
I _O	Output current		±25	mA
	Continuous current through V _{CC}		±100	mA
	Continuous current through GND		±100	mA
P _{tot}	Total power dissipation		400	mW
T _A	Operating free-air temperature	-40	85	°C
T _{stg}	Storage temperature	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	±2000	V
		±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	5.5	V
V _{IH}	High-level input voltage	SCL, SDA	0.7 × V _{CC}	6
		A2–A0, RESET	0.7 × V _{CC}	V _{CC} + 0.5
V _{IL}	Low-level input voltage	SCL, SDA	-0.5	0.3 × V _{CC}
		A2–A0, RESET	-0.5	0.3 × V _{CC}
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	PCA9546A						UNIT	
	DGV	DW	PW	RGV	RGY	D		
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	120	57	122.3	63.2	50	92.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{PORR}	Power-on reset voltage, V _{CC} rising	No load,	V _I = V _{CC} or GND		1.2	1.5		V
V _{PORF}	Power-on reset voltage, V _{CC} falling ⁽²⁾	No load,	V _I = V _{CC} or GND		0.8	1		V
V _{pass}	Switch output voltage	V _{SWin} = V _{CC} ,	I _{SWout} = -100 μA	5 V		3.6		V
				4.5 V to 5.5 V	2.6	4.5		
				3.3 V		1.9		
				3 V to 3.6 V	1.6	2.8		
				2.5 V		1.5		
				2.3 V to 2.7 V	1.1	2		
I _{OL}	SCL, SDA			V _{OL} = 0.4 V	2.3 V to 5.5 V	3	7	mA
				V _{OL} = 0.6 V		6	10	
I _I	SCL, SDA	V _I = V _{CC} or GND		2.3 V to 5.5 V				±1
	SC3–SC0, SD3–SD0							±1
	A2–A0							±1
	RESET ⁽⁴⁾							±1
I _{CC}	Operating mode	f _{SCL} = 100 kHz	V _I = V _{CC} or GND, I _O = 0	5.5 V		3	12	μA
				3.6 V		3	11	
				2.7 V		3	10	
	Standby mode	Low inputs	5.5 V		1.6	2		
			3.6 V		1	1.3		
			2.7 V		0.7	1.1		
		High inputs	5.5 V		1.6	2		
			3.6 V		1	1.3		
2.7 V		0.7	1.1					
ΔI _{CC}	Supply-current change	SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V _{CC} or GND			8	15	μA
			SCL or SDA input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.3 V to 5.5 V		8	15	
C _i	A2–A0	V _I = V _{CC} or GND		2.3 V to 5.5 V		4.5	6	pF
	RESET					4.5	5.5	
C _{io(OFF)} ⁽³⁾	SCL, SDA	V _I = V _{CC} or GND,	Switch OFF	2.3 V to 5.5 V		15	19	pF
	SC3–SC0, SD3–SD0					6	8	
R _{ON}	Switch on-state resistance	V _O = 0.4 V,	I _O = 15 mA	4.5 V to 5.5 V	4	10	16	Ω
			I _O = 10 mA	3 V to 3.6 V	5	13	20	
				2.3 V to 2.7 V	7	16	45	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), T_A = 25°C.

(2) The power-on reset circuit resets the I2C bus logic with V_{CC} < V_{PORF}.

(3) C_{io(ON)} depends on internal capacitance and external capacitance added to the SCn lines when channel(s) are ON.

(4) RESET = V_{CC} (held high) when all other input voltages, V_I = GND.

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#))

		MIN	MAX	UNIT
I²C BUS—STANDARD MODE				
f _{scl}	I ² C clock frequency	0	100	kHz
t _{sch}	I ² C clock high time	4		μs
t _{scl}	I ² C clock low time	4.7		μs
t _{sp}	I ² C spike time		50	ns
t _{sds}	I ² C serial-data setup time	250		ns
t _{sdh}	I ² C serial-data hold time	0 ⁽¹⁾		ns
t _{icr}	I ² C input rise time		1000	ns
t _{icf}	I ² C input fall time		300	ns
t _{ocf}	I ² C output fall time	10-pF to 400-pF bus	300	ns
t _{buf}	I ² C bus free time between stop and start	4.7		μs
t _{sts}	I ² C start or repeated start condition setup	4.7		μs
t _{sth}	I ² C start or repeated start condition hold	4		μs
t _{sps}	I ² C stop condition setup	4		μs
t _{vdL(Data)}	Valid data time (high to low) ⁽²⁾	SCL low to SDA output low valid	1	μs
t _{vdH(Data)}	Valid data time (low to high) ⁽²⁾	SCL low to SDA output high valid	0.6	μs
t _{vd(ack)}	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	1	μs
C _b	I ² C bus capacitive load		400	pF

- (1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
- (2) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see [Figure 7-1](#))

		MIN	MAX	UNIT
I²C BUS—FAST MODE				
f _{scl}	I ² C clock frequency	0	400	kHz
t _{sch}	I ² C clock high time	0.6		μs
t _{scl}	I ² C clock low time	1.3		μs
t _{sp}	I ² C spike time		50	ns
t _{sds}	I ² C serial-data setup time	100		ns
t _{sdh}	I ² C serial-data hold time	0 ⁽¹⁾		ns
t _{icr}	I ² C input rise time	20 + 0.1C _b ⁽²⁾	300	ns
t _{icf}	I ² C input fall time	20 + 0.1C _b ⁽²⁾	300	ns
t _{ocf}	I ² C output fall time	10-pF to 400-pF bus	20 + 0.1C _b ⁽²⁾	ns
t _{buf}	I ² C bus free time between stop and start	1.3		μs
t _{sts}	I ² C start or repeated start condition setup	0.6		μs
t _{sth}	I ² C start or repeated start condition hold	0.6		μs
t _{sps}	I ² C stop condition setup	0.6		μs
t _{vdL(Data)}	Valid data time (high to low) ⁽³⁾	SCL low to SDA output low valid	1	μs
t _{vdH(Data)}	Valid data time (low to high) ⁽³⁾	SCL low to SDA output high valid	0.6	
t _{vd(ack)}	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	1	μs
C _b	I ² C bus capacitive load		400	pF

- (1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
- (2) C_b = total bus capacitance of one bus line in pF
- (3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see [Figure 7-1](#))

6.7 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{WL}	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
$t_{rst}^{(1)}$	RESET time (SDA clear)		500	ns
$t_{REC(STA)}$	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

- (1) t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL} .

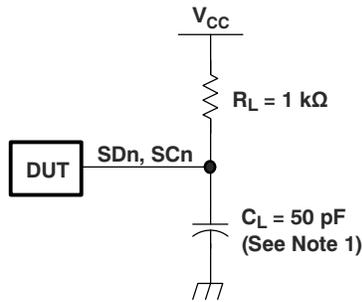
6.8 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see [Figure 7-1](#))

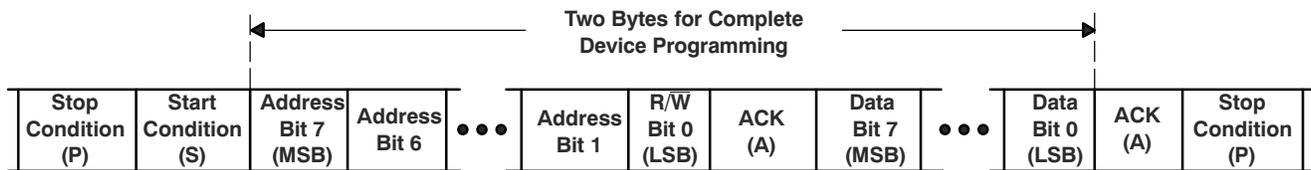
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^{(1)}$	Propagation delay time	SDA or SCL	SDn or SCn		0.3	ns
					1	

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

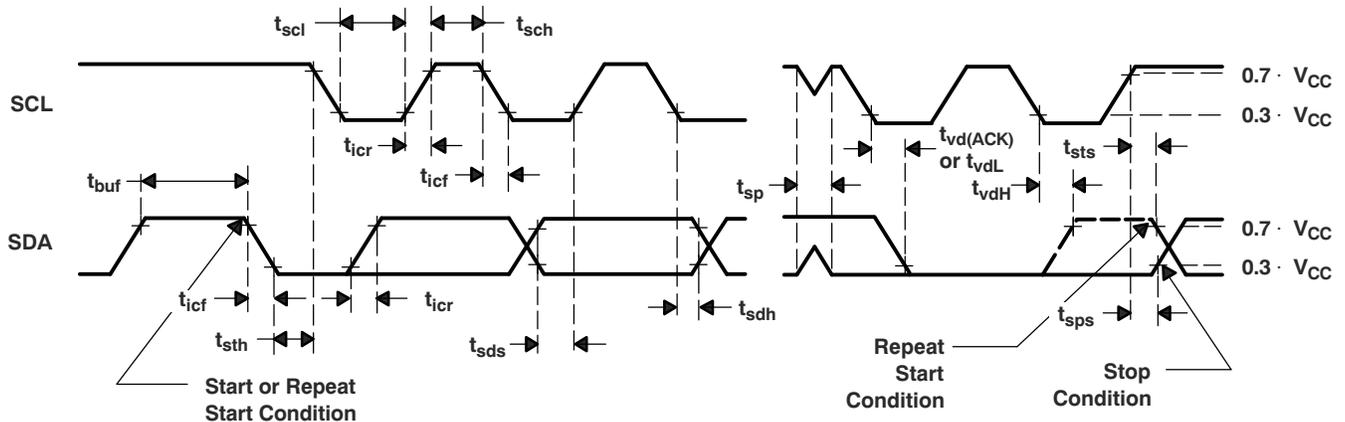
7 Parameter Measurement Information



Copyright © 2016, Texas Instruments Incorporated
I²C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I ² C address + R/W
2	Control register data



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 7-1. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

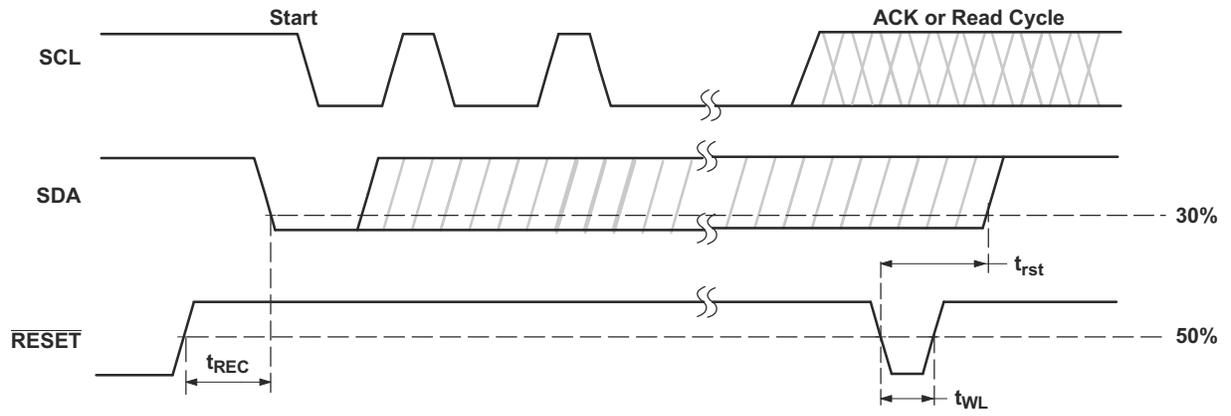


Figure 7-2. Reset Timing

8 Detailed Description

8.1 Overview

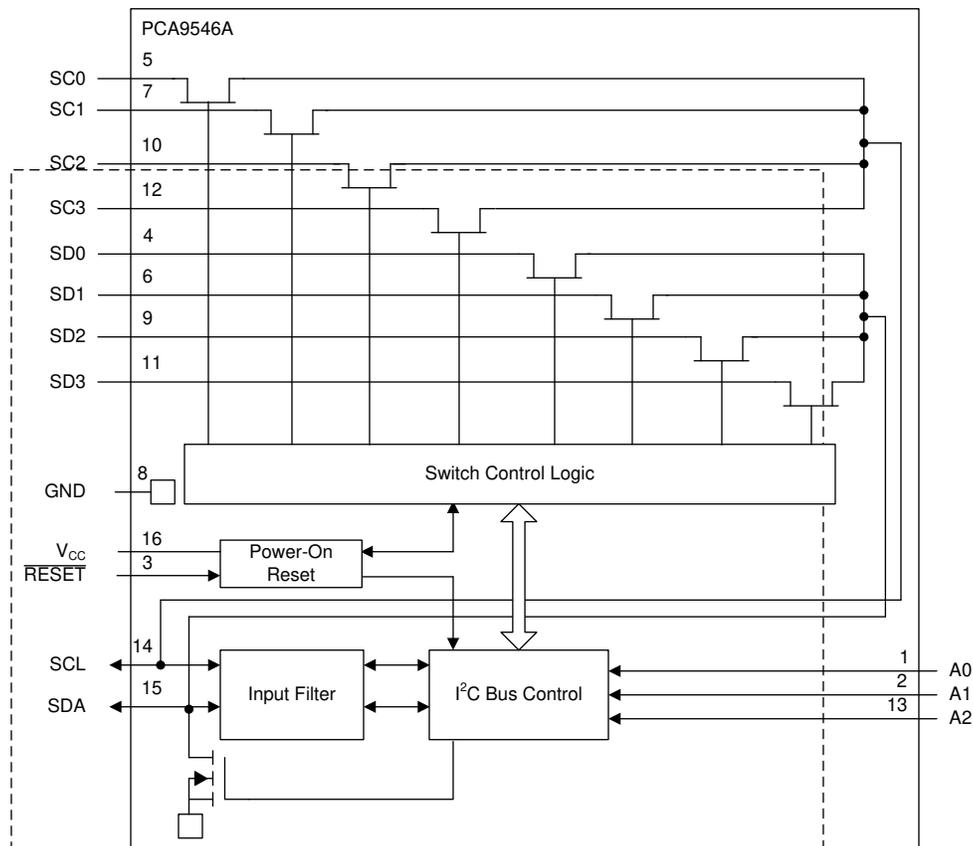
The PCA9546A is a 4-channel, bidirectional translating I²C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels.

The device offers an active-low $\overline{\text{RESET}}$ input which resets the state machine and allows the PCA9546A to recover should one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC} , also known as a power-on reset (POR). Both the $\overline{\text{RESET}}$ function and a POR will cause all channels to be deselected.

The connections of the I²C data path are controlled by the same I²C master device that is switched to communicate with multiple I²C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The PCA9546A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

8.3 Feature Description

The PCA9546A is a 4-channel, bidirectional translating switch for I²C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9546A features I²C control using a single 8-bit control register in which the four least significant bits control the enabling and disabling of the 4 switch channels of I²C data flow. Depending on the application, voltage translation of the I²C bus can also be achieved using the PCA9546A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I²C bus enters a fault state, the PCA9546A can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

8.4 Device Functional Modes

8.4.1 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of t_{WL} , the PCA9546A resets its registers and I²C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to V_{CC} through a pull-up resistor.

8.4.1.1 $\overline{\text{RESET}}$ Errata

If RESET voltage set higher than V_{CC} , current will flow from RESET pin to V_{CC} pin.

System Impact

V_{CC} will be pulled above its regular voltage level

System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than V_{CC}

8.4.2 Power-On Reset

When power is applied to V_{CC} , an internal power-on reset holds the PCA9546A in a reset condition until V_{CC} has reached V_{POR} . At this point, the reset condition is released, and the PCA9546A registers and I²C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below V_{POR} to reset the device.

8.5 Programming

8.5.1 I²C Interface

The I²C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see [Figure 8-1](#)).

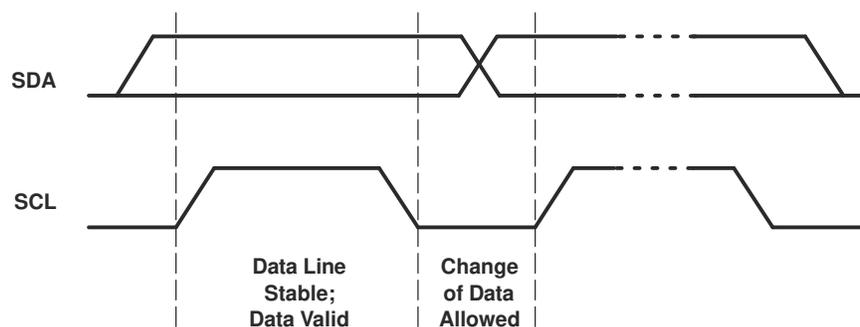


Figure 8-1. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 8-2).

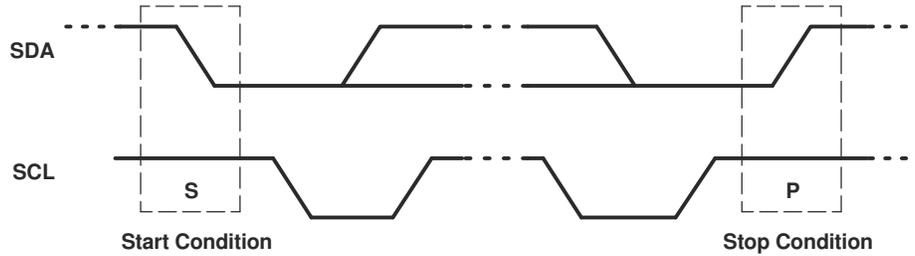


Figure 8-2. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 8-3).

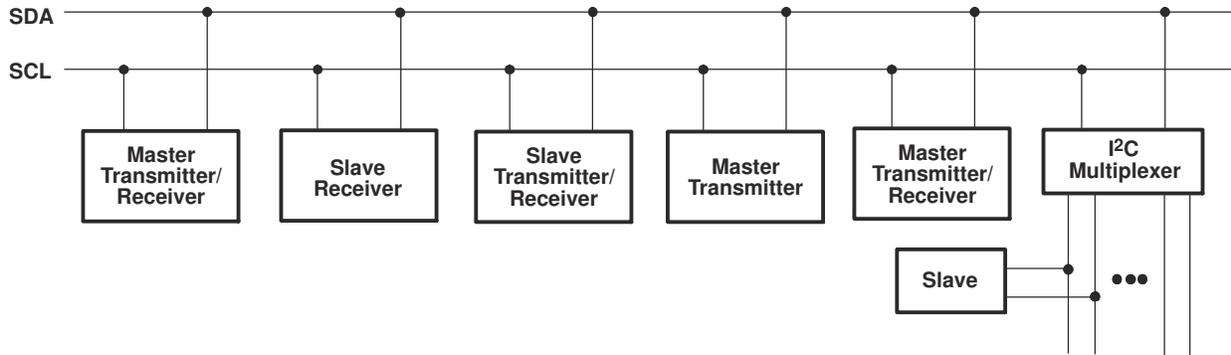


Figure 8-3. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 8-4). Setup and hold times must be taken into account.

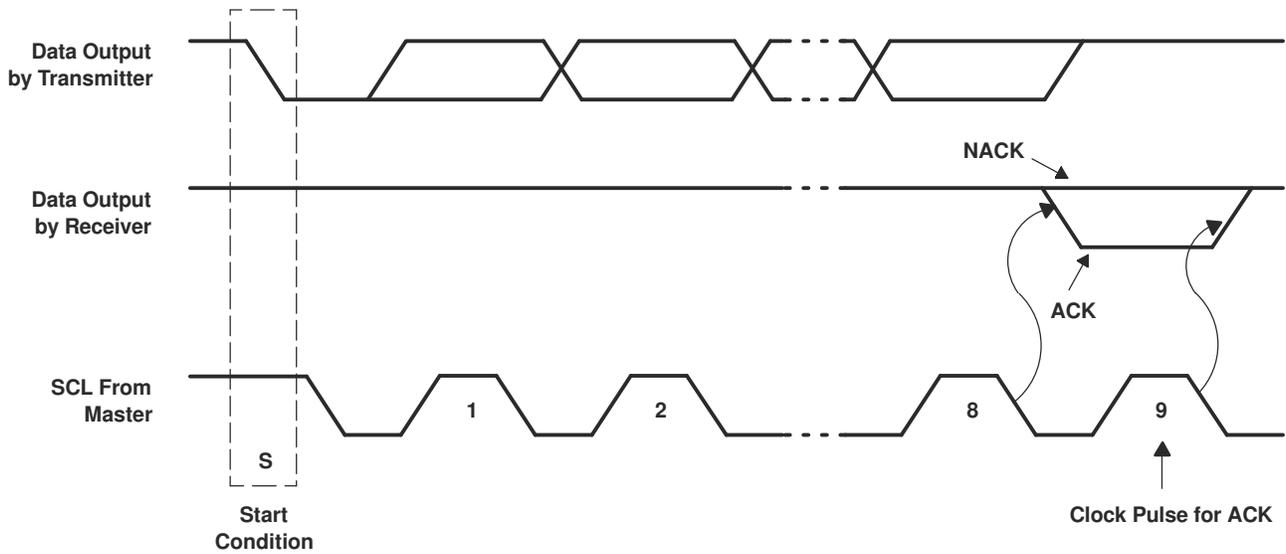


Figure 8-4. Acknowledgment on the I²C Bus

Data is transmitted to the PCA9546A control register using the write mode shown in Figure 8-5.

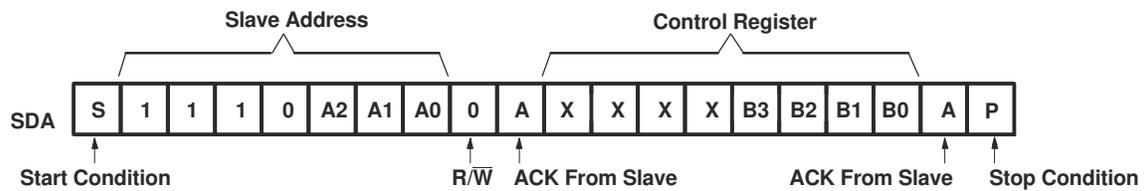


Figure 8-5. Write Control Register

Data is read from the PCA9546A control register using the read mode shown in Figure 8-6.

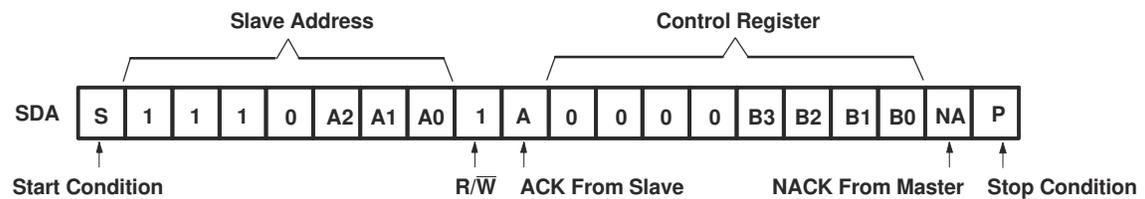


Figure 8-6. Read Control Register

8.6 Control Register

8.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9546A is shown in [Figure 8-7](#). To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low.

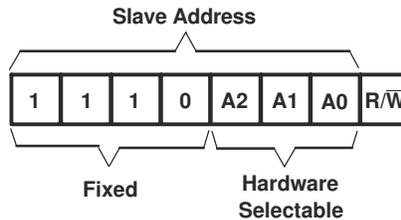


Figure 8-7. PCA9546A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

8.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9546A, which is stored in the control register (see [Figure 8-8](#)). If multiple bytes are received by the PCA9546A, it will save the last byte received. This register can be written and read via the I²C bus.

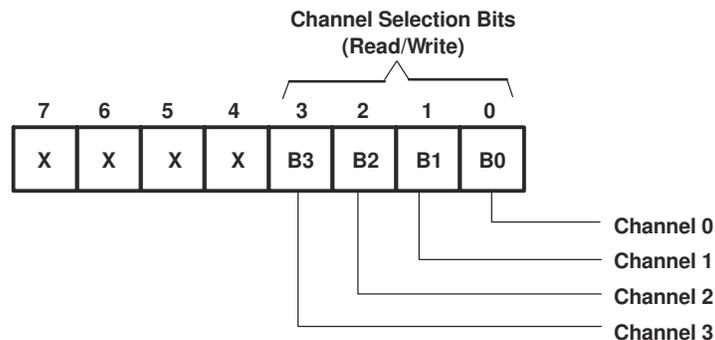


Figure 8-8. Control Register

8.6.3 Control Register Definition

One or several SC_n/SD_n downstream pairs, or channels, are selected by the contents of the control register (see [Table 8-1](#)). This register is written after the PCA9546A has been addressed. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SC_n/SD_n lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur right after the acknowledge cycle.

Table 8-1. Control Register Write (Channel Selection), Control Register Read (Channel Status)⁽¹⁾

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	X	0	Channel 1 disabled
							1	Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

- (1) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 and 2 are enabled. Care must be taken not to exceed the maximum bus capacity.

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

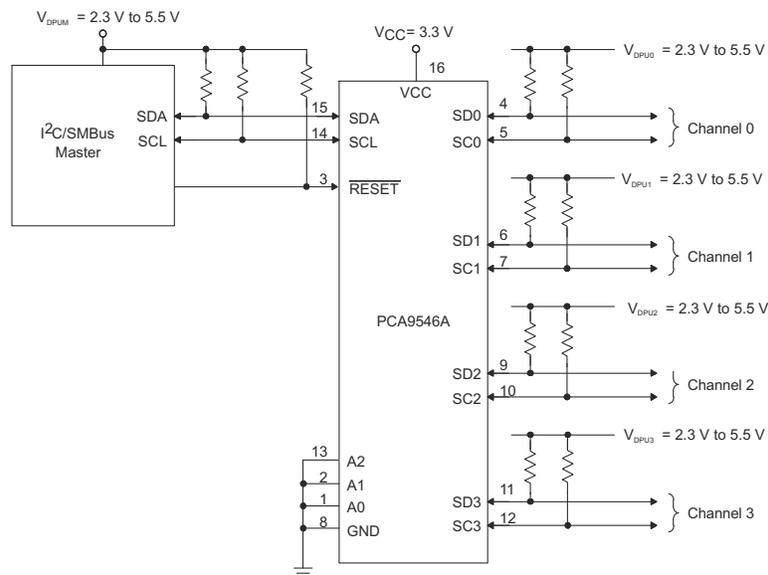
Applications of the PCA9546A will contain an I²C (or SMBus) master device and up to four I²C slave devices. The downstream channels are ideally used to resolve I²C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location must be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I²C master can move on and read the next channel.

In an application where the I²C bus will contain many additional slave devices that do not result in I²C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See [Design Requirements](#) and [Detailed Design Procedure](#)).

9.2 Typical Application

A typical application of the PCA9546A will contain anywhere from 1 to 5 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels ($V_{DPU0} - V_{DPU3}$). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, $V_{pass} = V_{DPUX}$. Once the maximum V_{pass} is known, V_{CC} can be selected easily using [Figure 9-2](#). In an application where voltage translation is necessary, additional design requirements must be considered (See [Design Requirements](#)).

[Figure 9-1](#) shows an application in which the PCA9546A can be used.



Copyright © 2016, Texas Instruments Incorporated

Figure 9-1. PCA9546A Typical Application Schematic

9.2.1 Design Requirements

The A0, A1, and A2 pins are hardware selectable to control the slave address of the PCA9546A. These pins may be tied directly to GND or V_{CC} in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p .

The pass-gate transistors of the PCA9546A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I²C bus to another.

Figure 9-2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) section of this data sheet). In order for the PCA9546A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 9-2, $V_{pass(max)}$ is 2.7 V when the PCA9546A supply voltage is 4 V or lower, so the PCA9546A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 9-1).

9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX} , $V_{OL(max)}$, and I_{OL} as shown in Equation 1:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, $f_{SCL} = 400$ kHz) and bus capacitance, C_b as shown in Equation 2:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9546A, $C_{iO(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

9.2.3 Application Curves

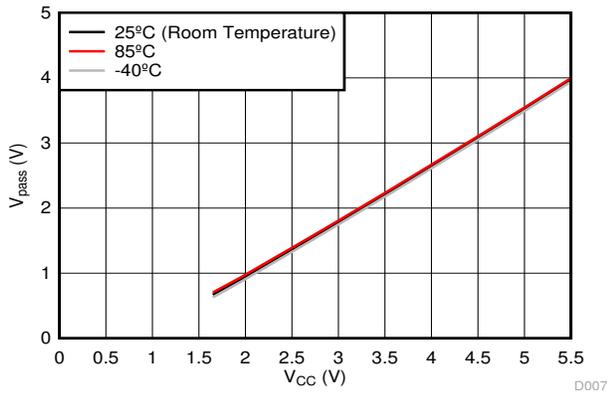
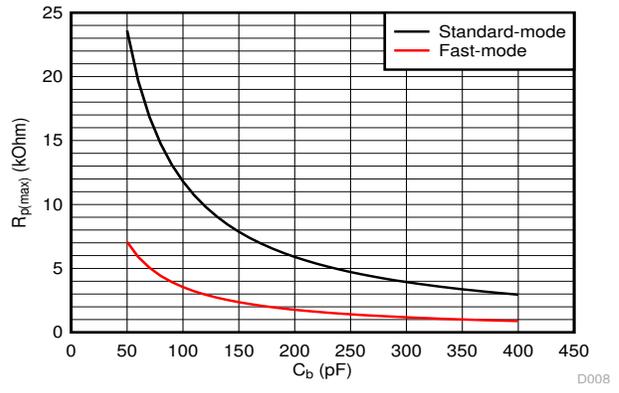
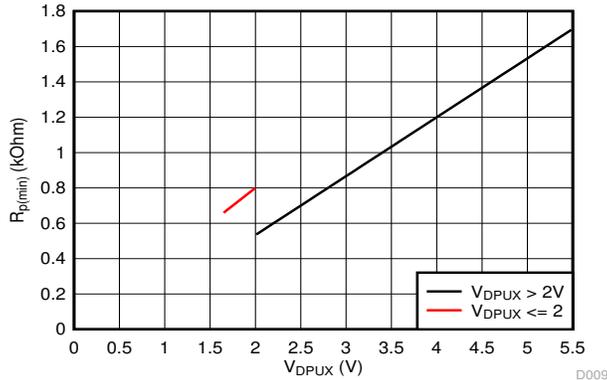


Figure 9-2. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



Standard-mode ($f_{SCL} = 100$ kHz, $t_r = 1$ μ s) Fast-mode ($f_{SCL} = 400$ kHz, $t_r = 300$ ns)

Figure 9-3. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



$V_{OL} = 0.2 \cdot V_{DPUX}$, $I_{OL} = 2$ mA when $V_{DPUX} \leq 2$ V

$V_{OL} = 0.4$ V, $I_{OL} = 3$ mA when $V_{DPUX} > 2$ V

Figure 9-4. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{DPUX})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9546A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power application cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 10-1](#) and [Figure 10-2](#).

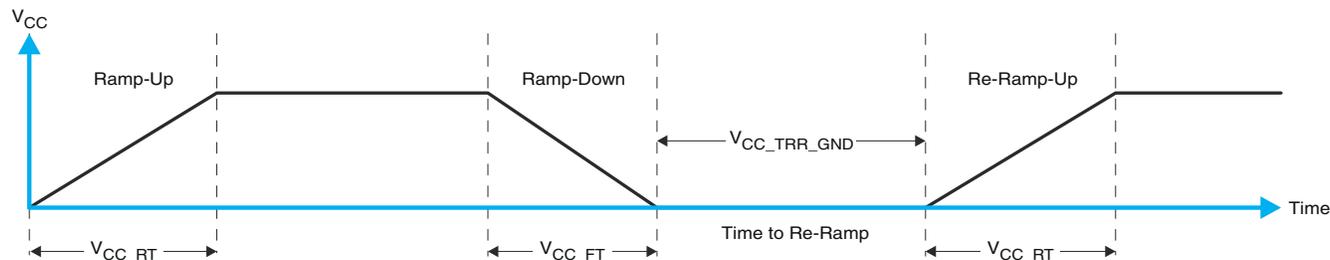


Figure 10-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

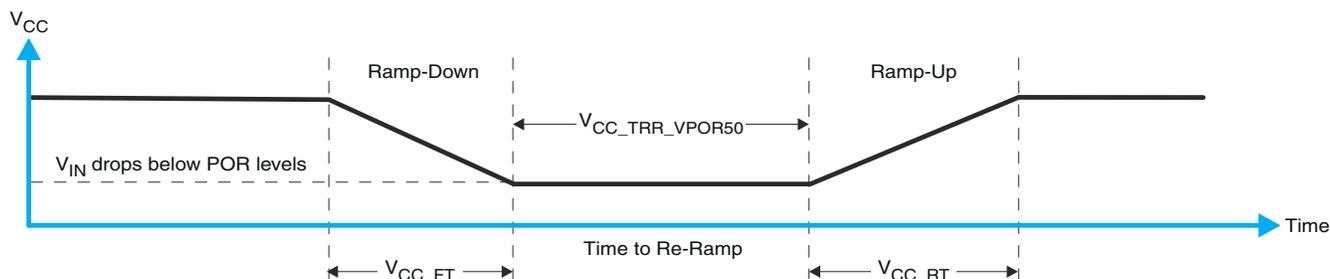


Figure 10-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

[Table 10-1](#) specifies the performance of the power-on reset feature for PCA9546A for both types of power-on reset.

Table 10-1. Recommended Supply Sequencing And Ramp Rates⁽¹⁾

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 10-1	1		100	ms
V_{CC_RT}	Rise rate	See Figure 10-1	0.01		100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 10-1	0.001			ms
$V_{CC_TRR_VPOR50}$	Time to re-ramp (when V_{CC} drops to $V_{POR_MIN} - 50$ mV)	See Figure 10-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when $V_{CCX_GW} = 1$ μ s	See Figure 10-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when $V_{CCX_GH} = 0.5 \times V_{CCX}$	See Figure 10-3				μ s
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. [Figure 10-3](#) and [Table 10-1](#) provide more information on how to measure these specifications.

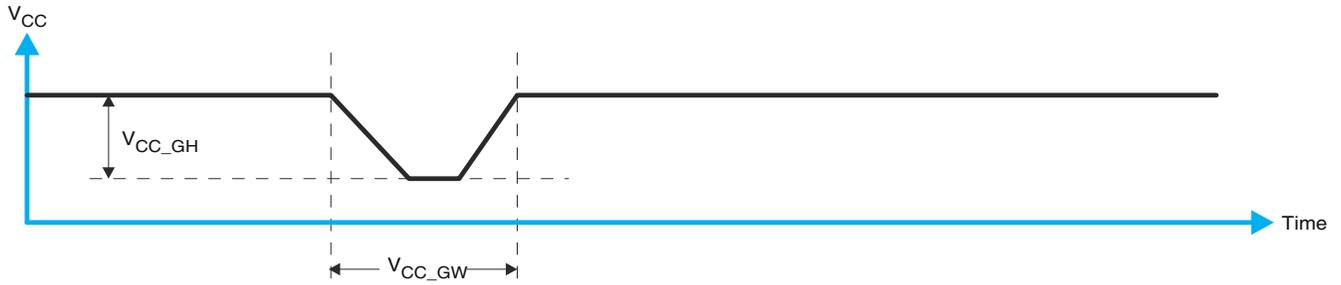


Figure 10-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 10-4 and Table 10-1 provide more details on this specification.

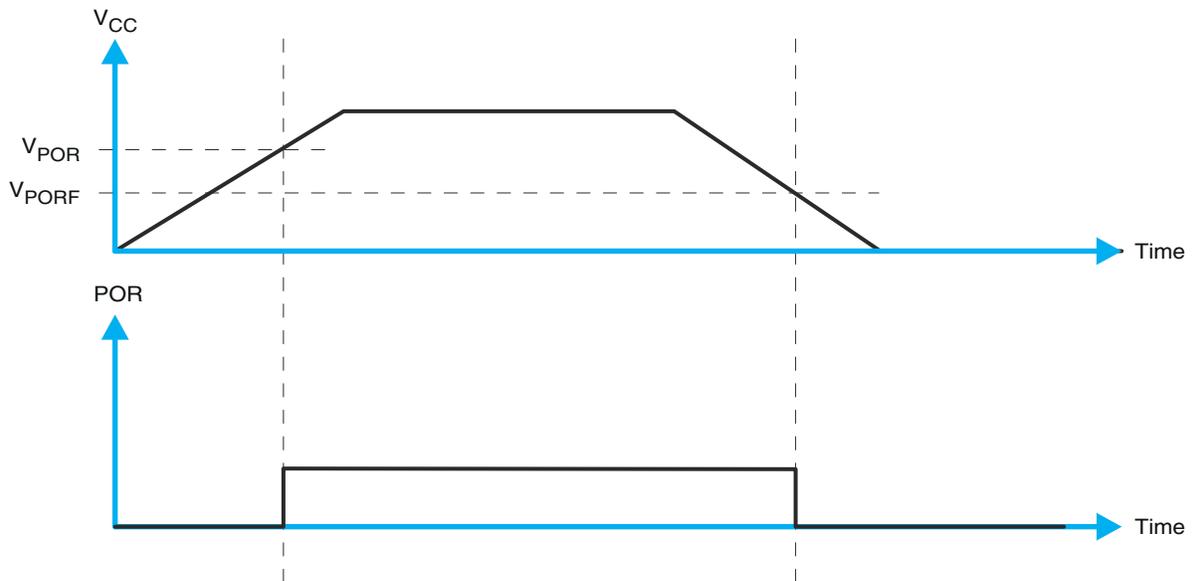


Figure 10-4. V_{POR}

11 Layout

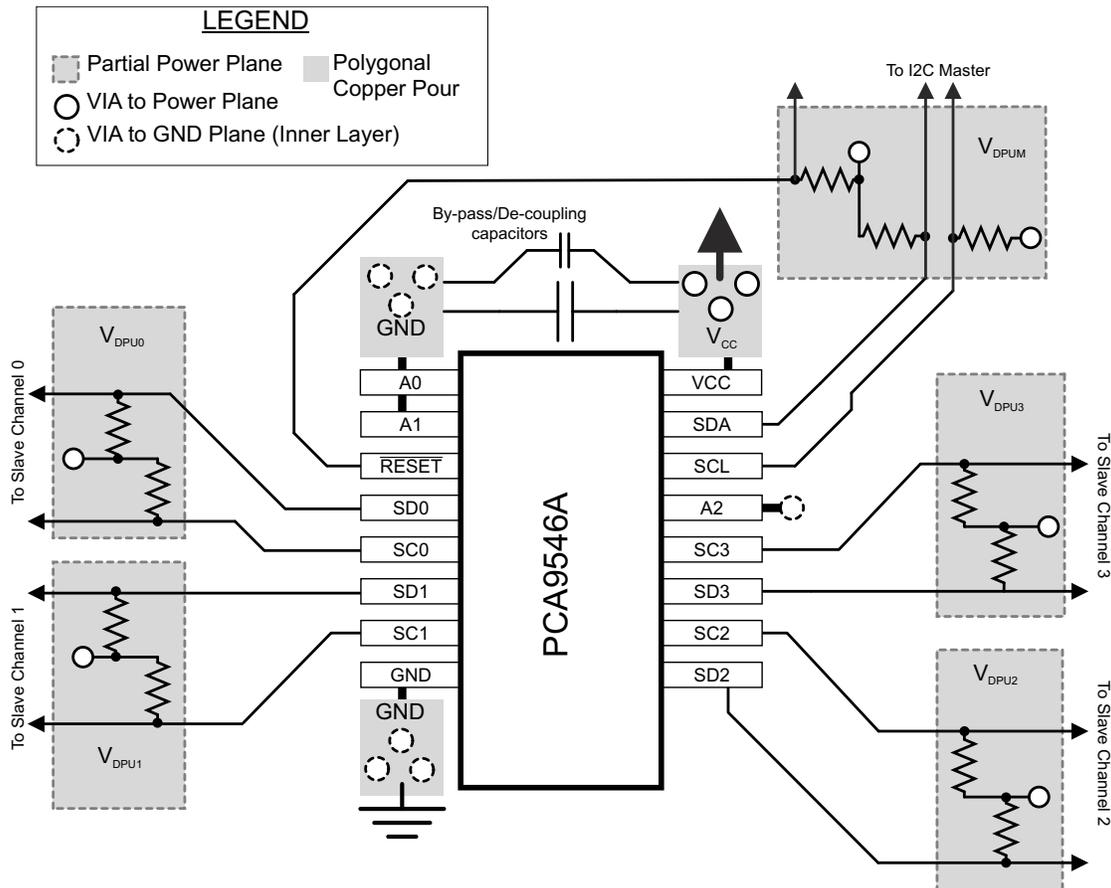
11.1 Layout Guidelines

For PCB layout of the PCA9546A, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I²C bus capacitance added by PCB parasitics, data lines (SC_n and SD_n) must be as short as possible and the widths of the traces must also be minimized (e.g. 5-10 mils depending on copper weight).

11.2 Layout Example



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCA9546ADGVR	NRND	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD546A
PCA9546ADGVR.A	NRND	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD546A
PCA9546ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9546A
PCA9546ADR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9546A
PCA9546ADRG4.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9546A
PCA9546ADT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	PCA9546A
PCA9546ADW	NRND	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9546A
PCA9546ADW.A	NRND	Production	SOIC (DW) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9546A
PCA9546ADWR	NRND	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9546A
PCA9546ADWR.A	NRND	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9546A
PCA9546APW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	PD546A
PCA9546APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD546A
PCA9546APWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD546A
PCA9546APWRE4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD546A
PCA9546APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD546A
PCA9546APWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	PD546A
PCA9546ARGVR	Active	Production	VQFN (RGV) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD546A
PCA9546ARGVR.B	Active	Production	VQFN (RGV) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD546A
PCA9546ARGVRG4.B	Active	Production	VQFN (RGV) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD546A
PCA9546ARGYR	NRND	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD546A
PCA9546ARGYR.A	NRND	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD546A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

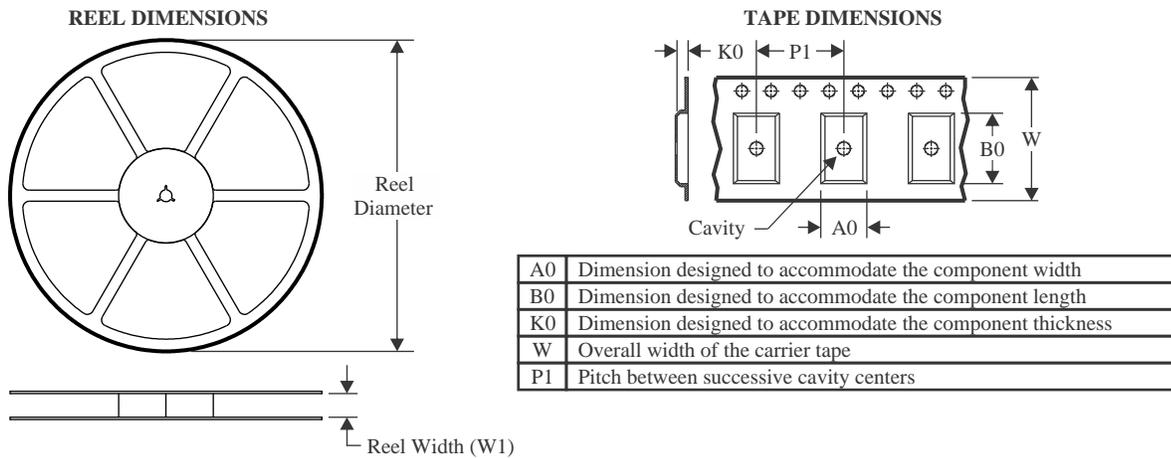
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

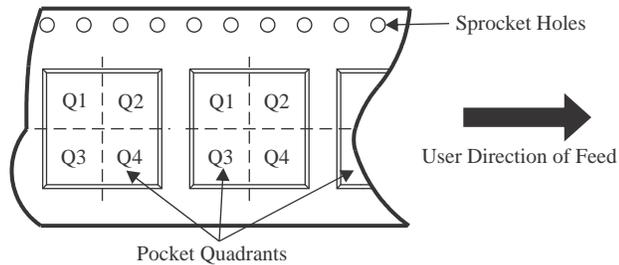
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



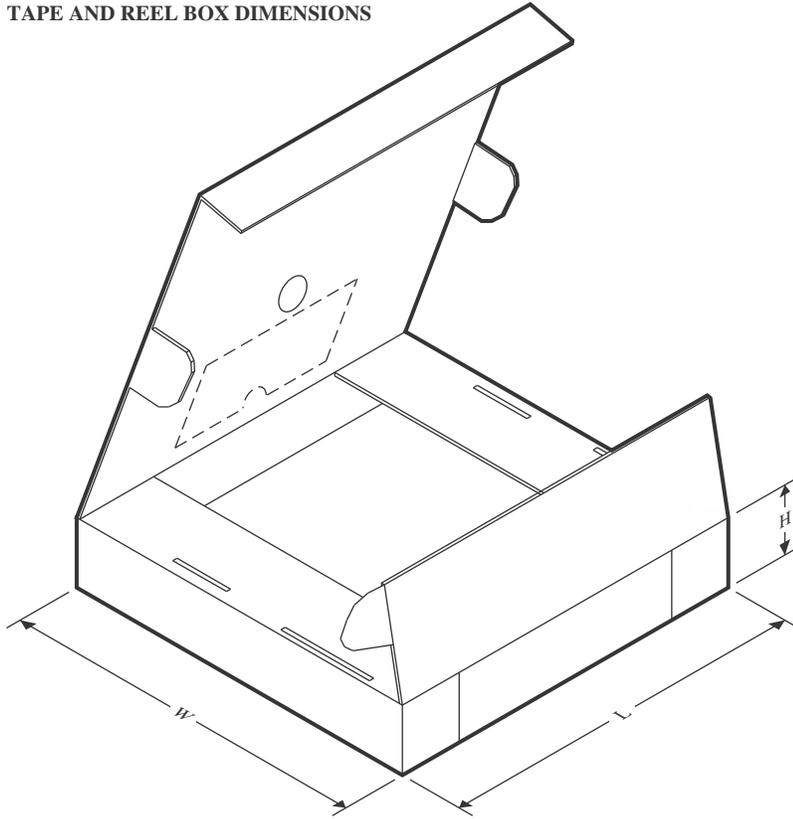
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9546ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9546ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
PCA9546ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9546APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9546ARGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCA9546ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

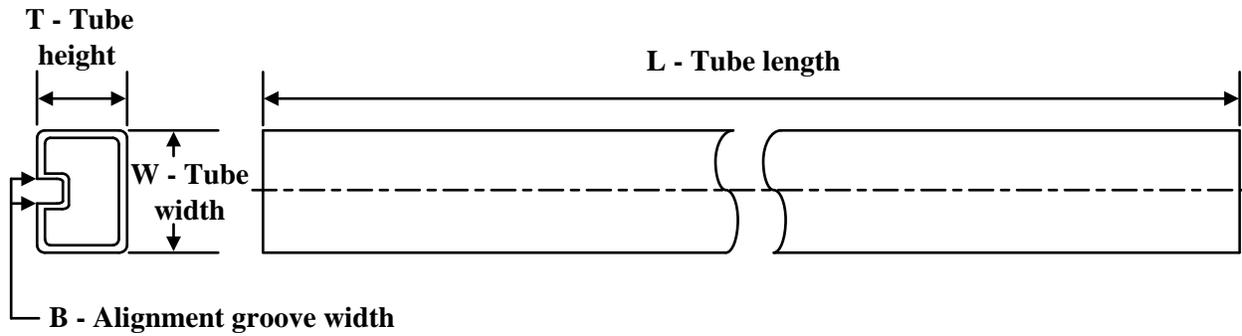
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9546ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
PCA9546ADR	SOIC	D	16	2500	356.0	356.0	35.0
PCA9546ADWR	SOIC	DW	16	2000	350.0	350.0	43.0
PCA9546APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
PCA9546ARGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
PCA9546ARGYR	VQFN	RGY	16	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
PCA9546ADW	DW	SOIC	16	40	506.98	12.7	4826	6.6
PCA9546ADW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

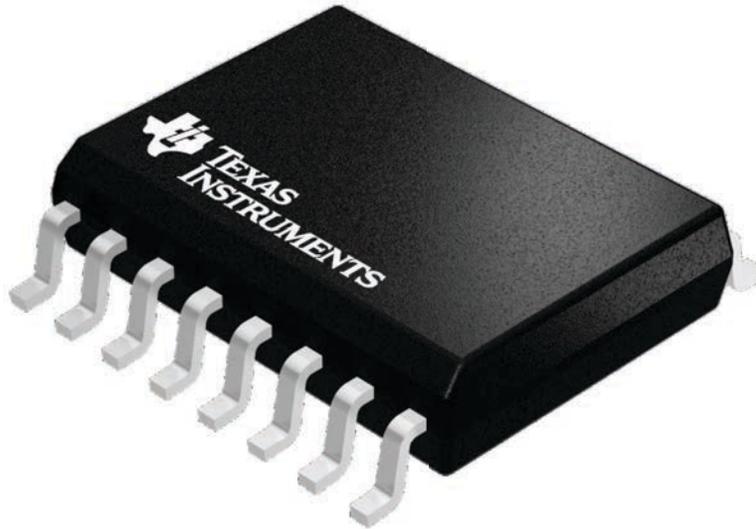
DW 16

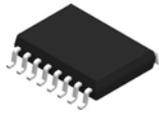
SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



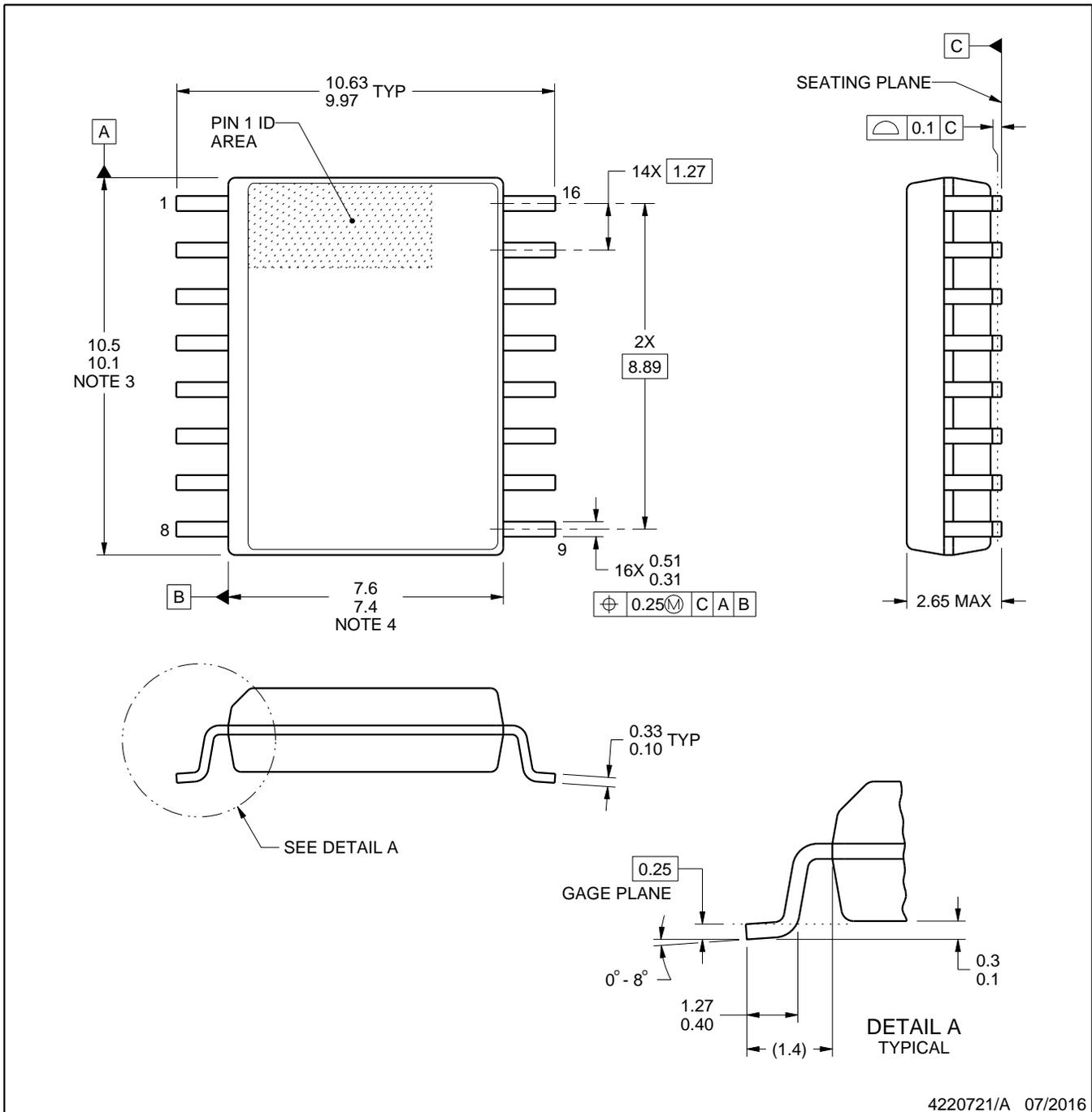


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

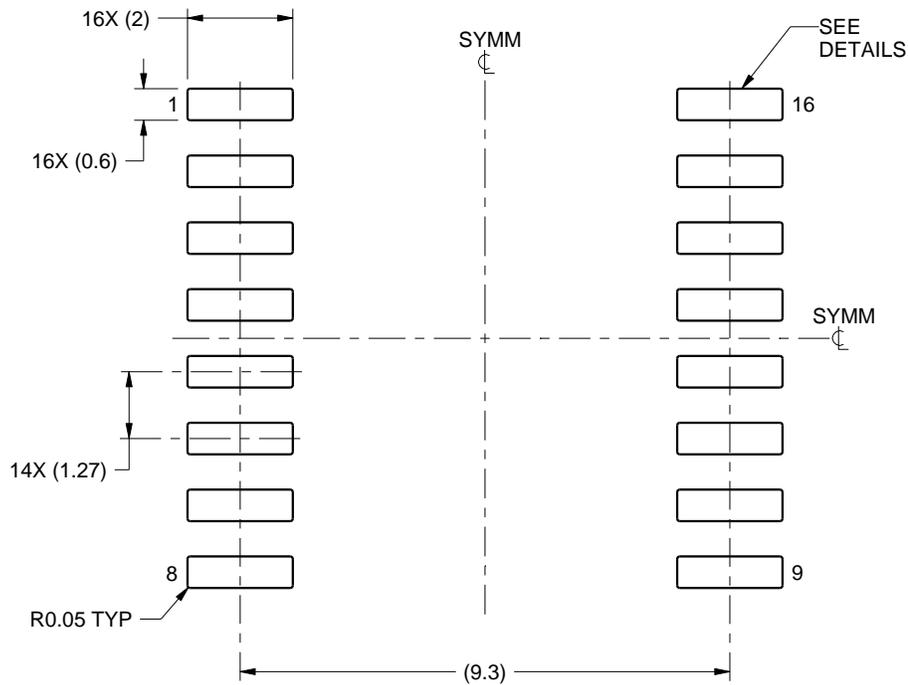
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

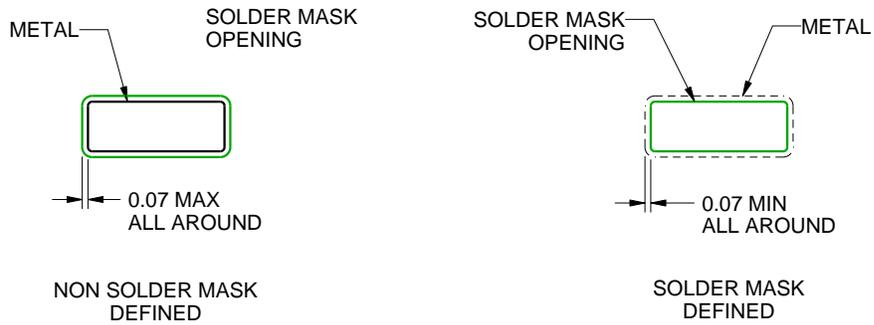
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

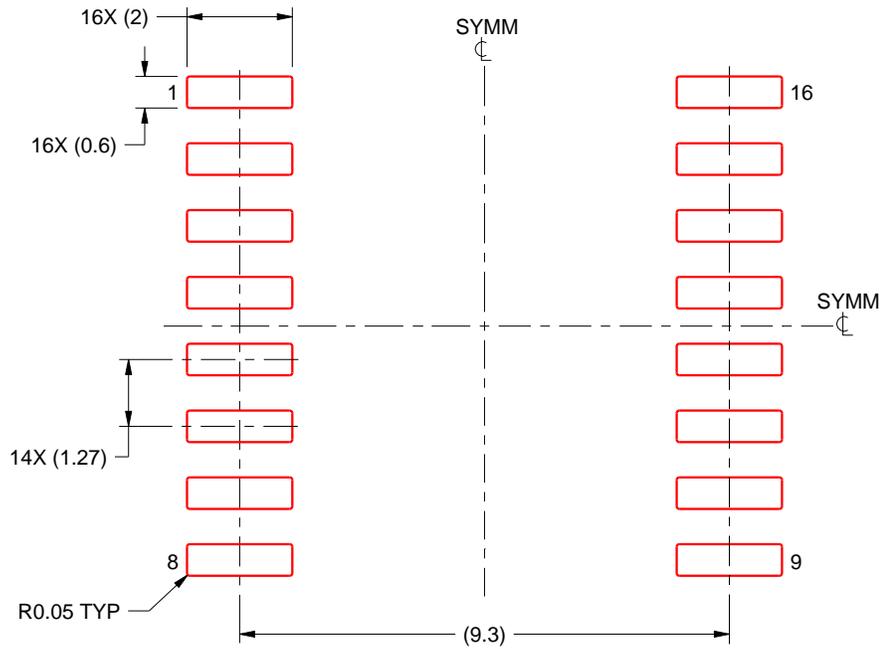
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

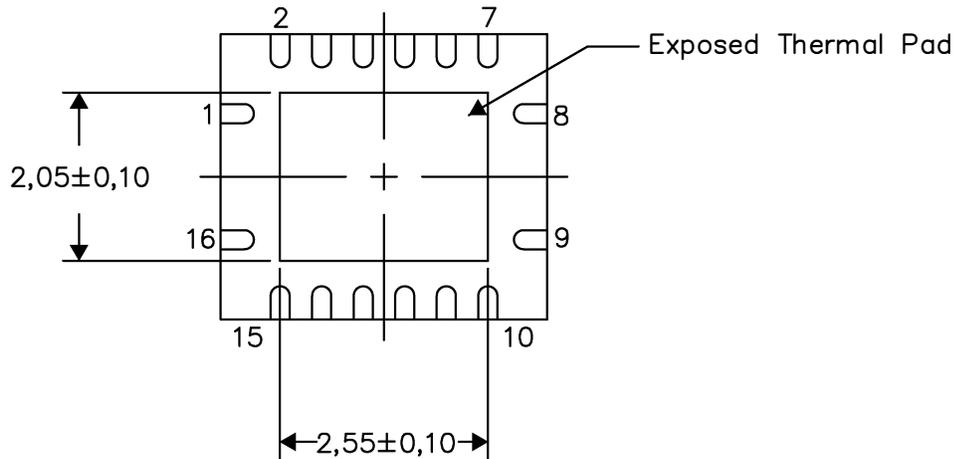
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

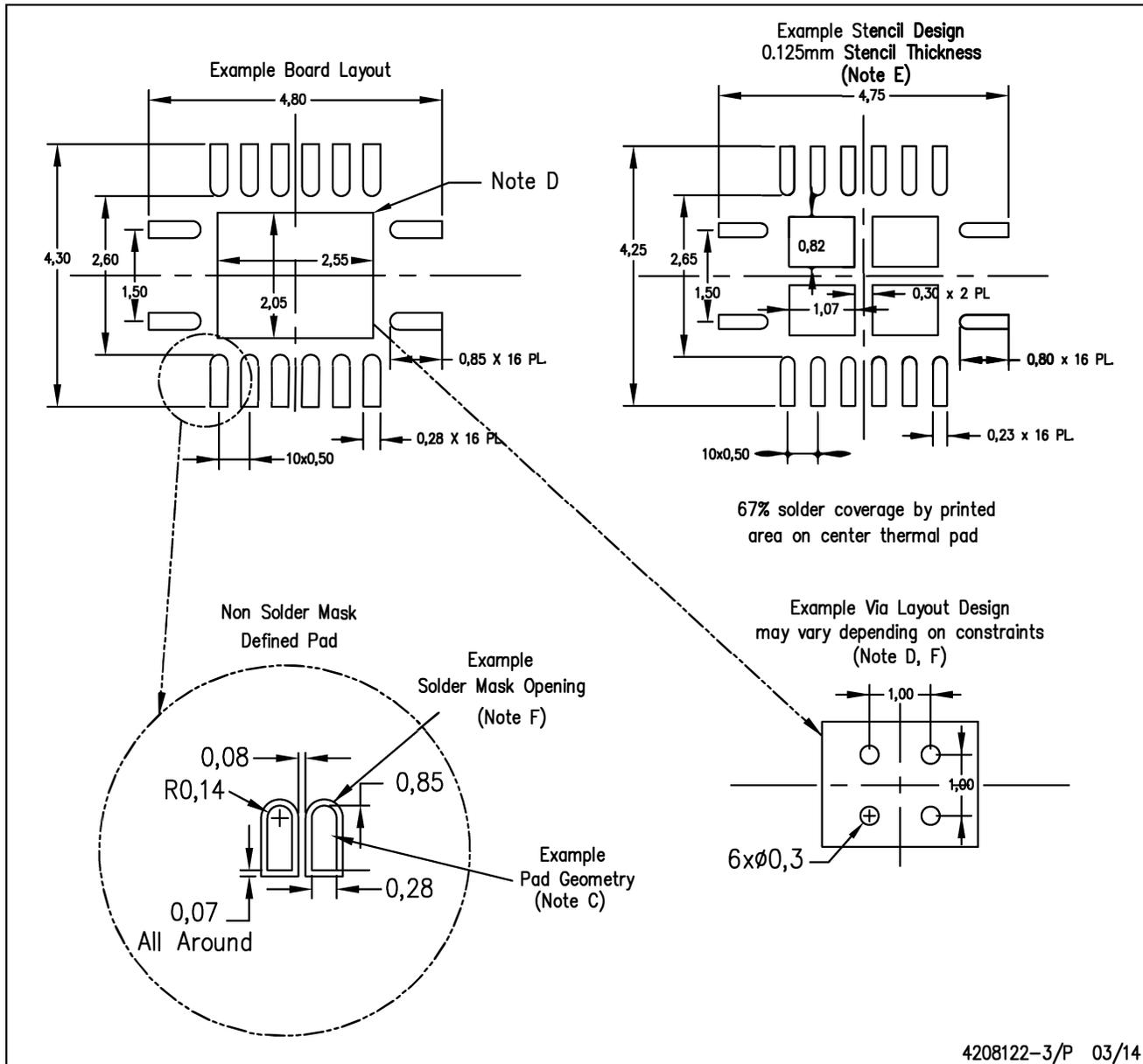
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

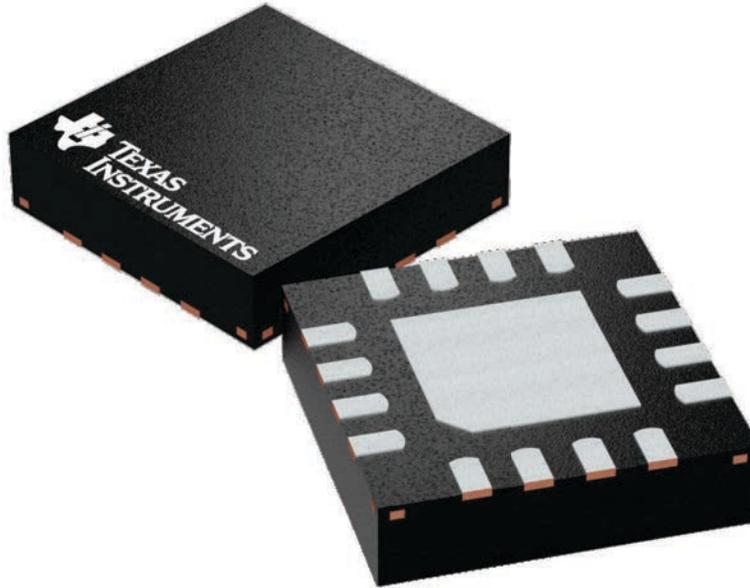
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

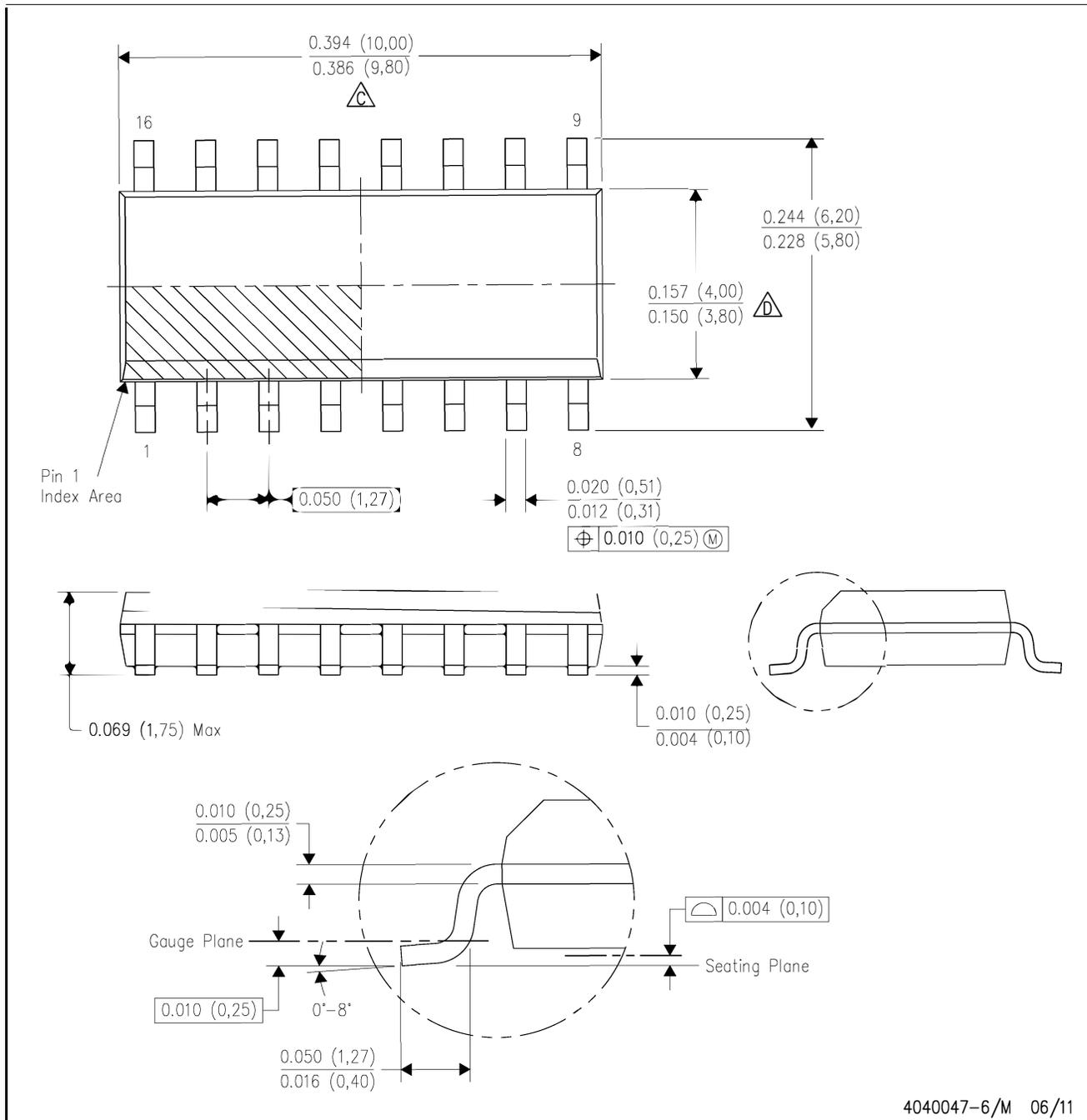
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

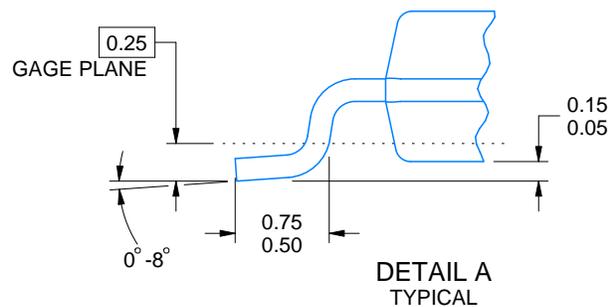
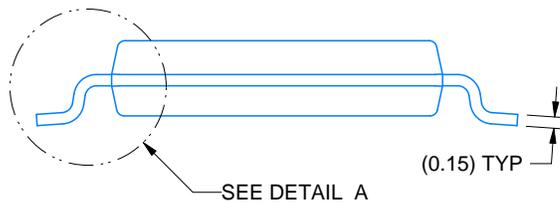
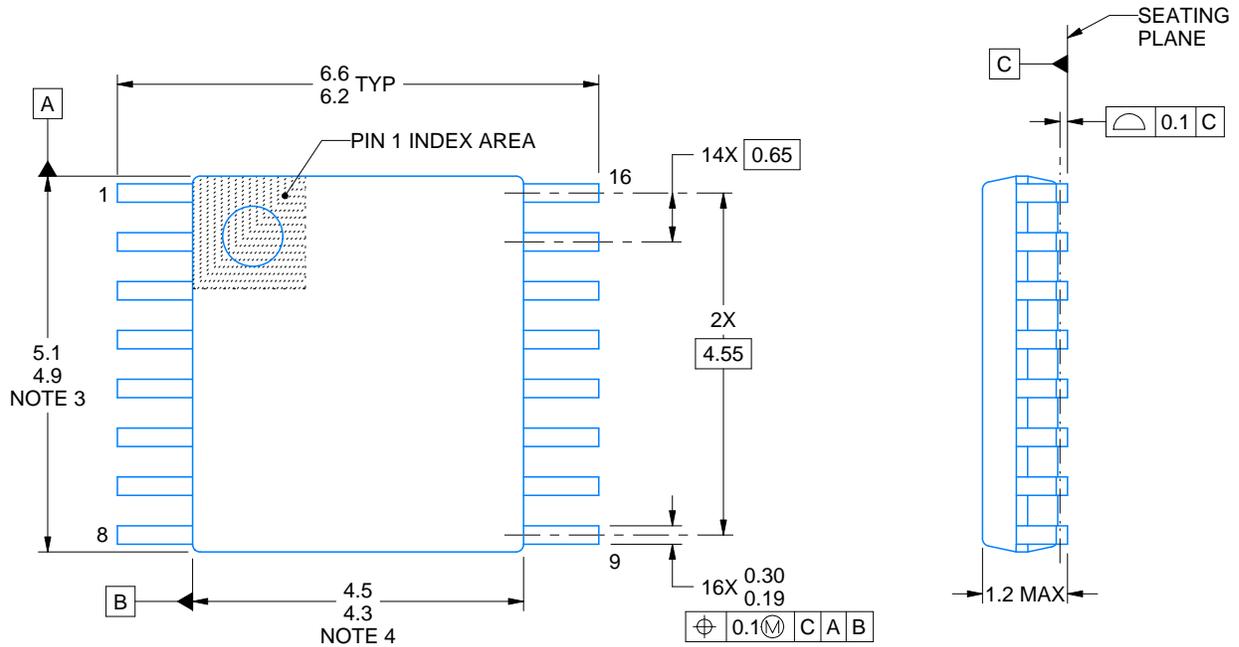
PW0016A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES:

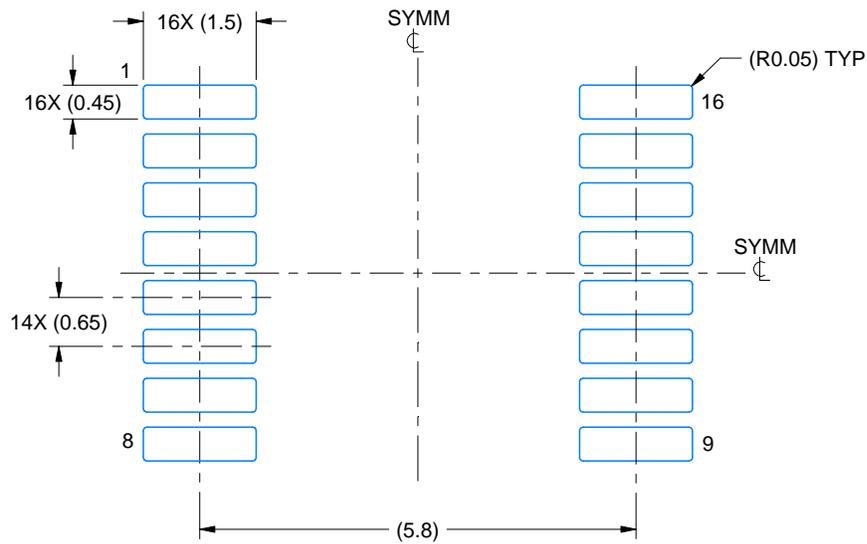
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

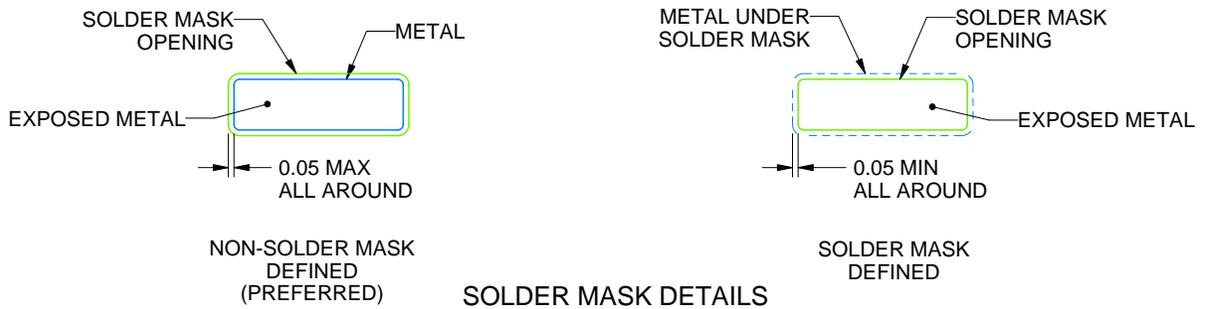
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

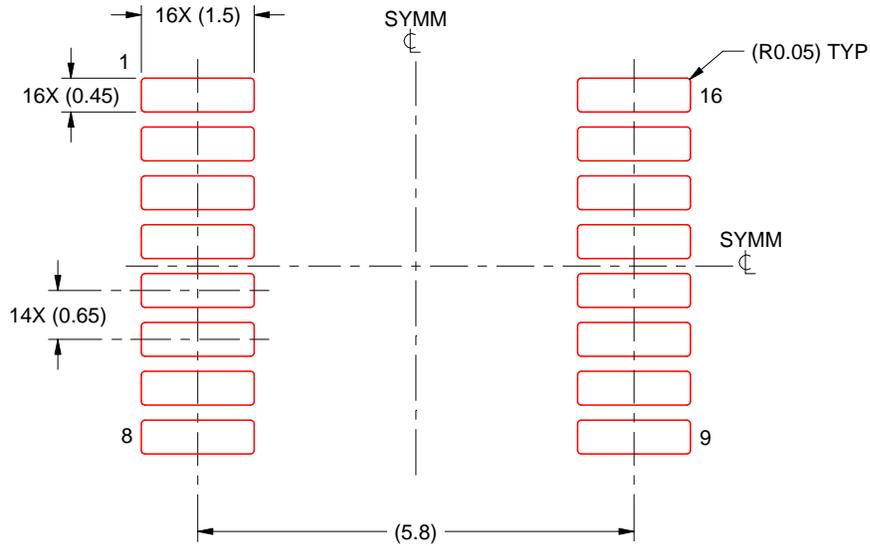
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.