DRV870x-Q1 Automotive H-Bridge Gate Driver

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
- Functional Safety-Capable
  - Documentation available to aid DRV8702-Q1 DRV8703-Q1 functional safety system design
- Single H-Bridge Gate Driver
  - Drives Four External N-Channel MOSFETs
  - Supports 100% PWM Duty Cycle
- 5.5 to 45-V Operating Supply-Voltage Range
- Three Control-Interface Options
  - PH/EN, Independent H-Bridge, and PWM
- Serial Interface for Configuration (DRV8703-Q1)
- Smart Gate Drive Architecture
  - Adjustable Slew-Rate Control
- Independent Control of Each H-Bridge
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Current-Shunt Amplifier
- Integrated PWM Current Regulation
- Low-Power Sleep Mode
- Protection Features
  - Supply Undervoltage Lockout (UVLO)
  - Charge-Pump Undervoltage (CPUV) Lockout
  - Overcurrent Protection (OCP)
  - Gate-Driver Fault (GDF)
  - Thermal Shutdown (TSD)
  - Watchdog Timer (DRV8703-Q1)
  - Fault-Condition Output (nFAULT)

2 Applications

- Power Window Lift, Sunroof, Seats, Sliding Door, Trunk and Tailgate
- Relay Replacement
  - Application Report: *SLVA837*
  - TI Design: *TIDUCQ9*
- Brushed-DC Pumps

3 Description

The DRV870x-Q1 devices are small single H-bridge gate drivers that use four external N-channel MOSFETs targeted to drive a bidirectional brushed-DC motor.

A PH/EN, independent H-Bridge, or PWM interface allows simple interfacing to controller circuits. An internal sense amplifier provides adjustable current control. Integrated Charge-Pump allows for 100% duty cycle support and can be used to drive external reverse battery switch.

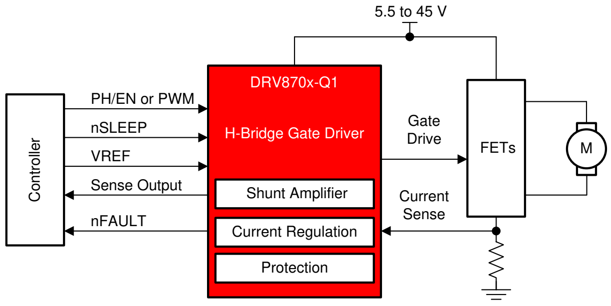
Independent Half Bridge mode allows sharing of half bridges to control multiple DC motors sequentially in a cost-efficient way. The gate driver includes circuitry to regulate the winding current using fixed off-time PWM current chopping.

The DRV870x-Q1 devices include Smart Gate Drive technology to remove the need for any external gate components (resistors and Zener diodes) while protecting the external FETs. The Smart Gate Drive architecture optimizes dead time to avoid any shoot-through conditions, provides flexibility in reducing electromagnetic interference (EMI) with programmable slew-rate control and protects against any gate-short conditions. Additionally, active and passive pulldowns are included to prevent any dv/dt gate turn on.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8702-Q1	VQFN (32)	5.00 mm × 5.00 mm
DRV8703-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2018) to Revision E (January 2021) — Page

- Added Functional Safety bullet.....1

Changes from Revision C (August 2018) to Revision D (December 2018) — Page

- Changed front page to remove second description.....1
- Deleted Gate-Drive Current figure.....1
- Added SL2 pin to the continous shunt amplifier input pin voltage.....7
- Added SL2 pin to the continous shunt amplifier input pin voltage.....7
- Changed IN1 to IN1/PH and IN2 to IN2/EN.....8
- Changed MODE typical pulldown resistance.....8
- Added MODE typical pullup resistance.....8
- Changed Wording in *VDS Configuration* section.....51

Changes from Revision B (March 2017) to Revision C (August 2018) — Page

- Changed the *Features* and *Descriptions* sections.....1
- Changed the type of the SL2 pin from O to I in the *Pin Functions* table.....5
- Changed SPI parameter name conventions.....13
- Changed the $V_{DS(OCP)}$ from 0.86 V to 0.96 V in the *OCP Threshold Voltage* graph.....15
- Changed the $I_{(CHOP)}$ equation in the *Current Regulation* and *Current Chopping Configuration* sections.....25
- Changed the current equation in the *Amplifier Output (SO)* section.....26
- Changed the description of the WD_EN bit in the *IDRIVE and WD Field Descriptions* table.....43

Changes from Revision A (November 2016) to Revision B (March 2017) — Page

- Changed the maximum voltage for AVDD from 5.7 to 5.75 in the *Absolute Maximum Ratings* table.....14
- Changed maximum V_{SP} value for GAIN_CS = 00 and GAIN_CS = 10 for the DRV8703-Q1 amplifier gain parameter in the *Electrical Characteristics* table.....14

- Added the $R_{(VDRAIN)}$ note to the *External Components* table.. 23
- Changed one resistor value from 32 kΩ to 65 kΩ in the *MODE Pin Block Diagram* 24
- Changed what happens when a fault condition is no longer present in the *Overcurrent Protection (OCP)* section.. 37
- Deleted A_V × from tthe **I**(CHOP) equation in the *Current Chopping Configuration* section.............................. 51

Changes from Revision * (October 2016) to Revision A (November 2016)	**Page**
• Released the full version of the data sheet	1

5 Pin Configuration and Functions

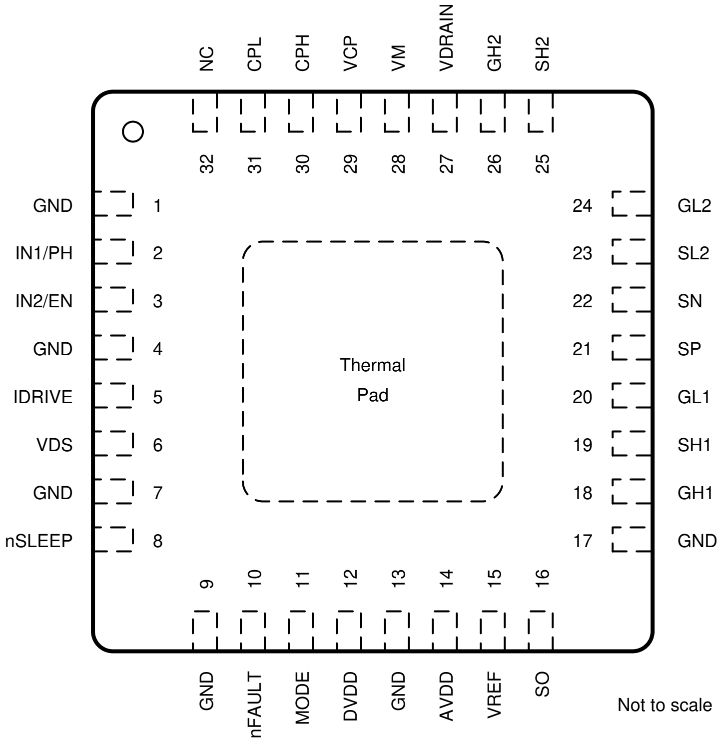


Figure 5-1. DRV8702-Q1 RHB Package With Wettable Flanks 32-Pin VQFN Top View

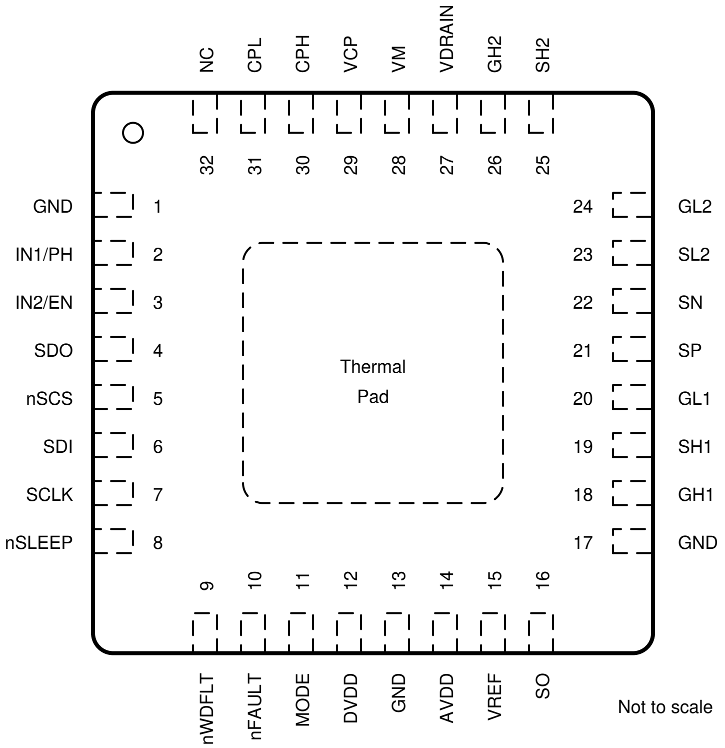


Figure 5-2. DRV8703-Q1 RHB Package With Wettable Flanks 32-Pin VQFN Top View

Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8702-Q1	DRV8703-Q1		
AVDD	14	14	PWR	Analog regulator. This pin is the 5-V analog supply regulator. Bypass this pin to ground with a 6.3-V, 1-µF ceramic capacitor.
CPH	30	30	PWR	Charge-pump switching node. Connect a 0.1-µF X7R capacitor rated for the supply voltage (VM) between the CPH and CPL pins.
CPL	31	31	PWR	Charge-pump switching node. Connect a 0.1-µF X7R capacitor rated for the supply voltage (VM) between the CPH and CPL pins.
DVDD	12	12	PWR	Logic regulator. This pin is the regulator for the 3.3-V logic supply. Bypass this pin to ground with a 6.3-V, 1-µF ceramic capacitor.
GH1	18	18	O	High-side gate. Connect this pin to the high-side FET gate.
GH2	26	26	O	High-side gate. Connect this pin to the high-side FET gate.
GL1	20	20	O	Low-side gate. Connect this pin to the low-side FET gate.
GL2	24	24	O	Low-side gate. Connect this pin to the low-side FET gate.
GND	1	1	PWR	Device ground. Connect this pin to the system ground.
GND	13	13	PWR	Device ground. Connect this pin to the system ground.
GND	17	17	PWR	Device ground. Connect this pin to the system ground.
GND	4	—	PWR	Device ground. Connect this pin to the system ground.
GND	7	—	PWR	Device ground. Connect this pin to the system ground.
GND	9	—	PWR	Device ground. Connect this pin to the system ground.
IDRIVE	5	—	I	Current setting pin for the gate drive. The resistor value or voltage forced on this pin sets the gate-drive current. For more information see the *Section 8.2.2.2* section.
IN1/PH	2	2	I	Input control pins. The logic of this pin is dependent on the MODE pin. This pin is connected to an internal pulldown resistor.

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8702-Q1	DRV8703-Q1		
IN2/EN	3	3	I	Input control pins. The logic of this pin is dependent on the MODE pin. This pin is connected to an internal pulldown resistor.
MODE	11	11	I	Mode control pin. Pull this pin to logic low to use H-bridge operation. Pull this pin to logic high for independent half-bridge operation. This pin is connected to an internal resistor divider. Operation of this pin is latched on power up or when exiting sleep mode. This pin is connected to an internal pullup and pulldown resistors.
NC	32	32	NC	No connect. No internal connection.
SCLK	—	7	I	SPI clock. This pin is for the SPI clock signal. This pin is connected to an internal pulldown resistor.
SDI	—	6	I	SPI input. This pin is for the SPI input signal. This pin is connected to an internal pulldown resistor.
SDO	—	4	OD	SPI output. This pin is for the SPI output signal. This pin is an open-drain output that requires an external pullup resistor.
SH1	19	19	I	High-side source. Connect this pin to the high-side FET source.
SH2	25	25	I	High-side source. Connect this pin to the high-side FET source
SL2	23	23	I	Low-side source. Connect this pin to the low-side FET source.
SN	22	22	I	Shunt-amplifier negative input. Connect this pin to the current-sense resistor.
SO	16	16	O	Shunt-amplifier output. The voltage on this pin is equal to the SP voltage times A_V plus an offset. Place no more than 1 nF of capacitance on this pin.
SP	21	21	I	Shunt-amplifier positive input. Connect this pin to the current-sense resistor.
VCP	29	29	PWR	Charge-pump output. Connect a 16-V, 1-µF ceramic capacitor between this pin and the VM pin.
VDRAIN	27	27	I	High-side FET drain connection. This pin is common for the two H-bridges.
VDS	6	—	I	VDS monitor setting pin. The resistor value or voltage forced on this pin sets the VDS monitor threshold. For more information see the *Section 8.2.2.3* section.
VM	28	28	PWR	Power supply. Connect this pin to the motor supply voltage. Bypass this pin to ground with a 0.1-µF ceramic plus a 10-µF (minimum) capacitor.
VREF	15	15	I	Current set reference input. The voltage on this pin sets the driver chopping current.
nWDFLT	—	9	OD	Watchdog fault indication pin. This pin is pulled logic low when a watchdog fault condition occurs. This pin is an open-drain output that requires an external pullup resistor.
nFAULT	10	10	OD	Fault indication pin. This pin is pulled logic low when a fault condition occurs. This pin is an open-drain output that requires an external pullup resistor.
nSCS	—	5	I	SPI chip select. This pin is the select and enable for SPI. This pin is active low.
nSLEEP	8	8	I	Device sleep mode. Pull this pin to logic low to put device into a low-power sleep mode with the FETs in high impedance (Hi-Z). This pin is connected to an internal pulldown resistor.

(1) I = input, O = output, PWR = power, NC = no connect, OD = open-drain output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	VM	–0.3	47	V
Charge pump voltage	VCP, CPH	–0.3	V_{VM} + 12	V
Charge pump negative switching pin	CPL	–0.3	V_{VM}	V
Internal logic regulator voltage	DVDD	–0.3	3.8	V
Internal analog regulator voltage	AVDD	–0.3	5.75	V
Drain pin voltage	VDRAIN	–0.3	47	V
Voltage difference between supply and VDRAIN	VM – VDRAIN	–10	10	V
Control pin voltage	IN1, IN2, nSLEEP, nFAULT, VREF, IDRIVE, VDS, MODE, nSCS, SCLK, SDI, SDO, nWDFLT	–0.3	5.75	V
High-side gate pin voltage	GH1, GH2	–0.3	V_{VM} + 12	V
Low-side gate pin voltage	GL1, GL2	–0.3	12	V
Continuous phase-node pin voltage	SH1, SH2	–1.2	V_{VM} + 1.2	V
Pulsed 10-µs phase-node pin voltage	SH1, SH2	–2	V_{VM} + 2	V
Continuous shunt amplifier input pin voltage	SP, SL2	–0.5	1.2	V
	SN	–0.3	0.3	V
Pulsed 10-µs shunt amplifier input pin voltage	SP, SL2	–1	1.2	V
Shunt amplifier output pin voltage	SO	–0.3	5.75	V
Shunt amplifier output pin current	SO	0	5	mA
Maximum current, limit current with external series resistor	VDRAIN	–2	2	mA
Open-drain output current	nFAULT, SDO, nWDFLT	0	10	mA
Gate pin source current	GH1, GL1, GH2, GL2	0	250	mA
Gate pin sink current	GH1, GL1, GH2, GL2	0	500	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins (1, 8, 9, 16, 17, 24, 25, and 32)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{VM}	Power supply voltage	VM	5.5	45	V
V_{CC}	Logic-level input voltage		0	5.25	V
V_{VREF}	Current Shunt Amplifier Reference Voltage	VREF	0.3(1)	3.6	V
$f_{(PWM)}$	Applied PWM signal (IN1/IN2)	IN1, IN2		100	kHz
I_{AVDD}	AVDD external load current			30(2)	mA
I_{DVDD}	DVDD external load current			30(2)	mA
I_{SO}	Shunt-amplifier output-current loading	SO		5	mA
T_A	Operating ambient temperature		–40	125	°C

(1) Operational at V_{VREF} = 0 to approximately 0.3 V, but accuracy is degraded.
(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV870x-Q1	UNIT
		RHB (VQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, AVDD, DVDD)						
V_{VM}	VM operating voltage	Gate drivers functional	5.5		45	V
		Logic functional	4.5		45	
I_{VM}	VM operating supply current	V_{VM} = 13.5 V; nSLEEP=1	5.5	7.5	12	mA
$I_{(SLEEP)}$	VM sleep mode supply current	nSLEEP = 0, V_{VM} = 13.5 V, T_A = 25°C			14	µA
		nSLEEP = 0, V_{VM} = 13.5 V, T_A = 125°C(1)			25	
V_{DVDD}	Internal logic regulator voltage	2-mA load	3	3.3	3.5	V
		30-mA load, V_{VM} = 13.5 V	2.9	3.2	3.5	
V_{AVDD}	Internal logic regulator voltage	2-mA load	4.7	5	5.3	V
		30-mA load, V_{VM} = 13.5 V	4.6	5	5.3	
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	V_{VM} = 13.5 V; I_{VCP} = 0 to 12 mA	22.5	23.5	24.5	V
		V_{VM} = 8 V; I_{VCP} = 0 to 10 mA	13.7	14	14.8	
		V_{VM} = 5.5 V; I_{VCP} = 0 to 8 mA	8.9	9.1	9.5	
I_{VCP}	Charge-pump current capacity	V_{VM} > 13.5 V	12			mA
		8 V < V_{VM} < 13.5 V	10			
		5.5 V < V_{VM} < 8 V	8			
CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP, MODE, nSCS, SCLK, SDI)						

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input logic-low voltage		0		0.8	V
V_{IH}	Input logic-high voltage		1.5		5.25	V
V_{hys}	Input logic hysteresis		100			mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–5		5	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			70	µA
R_{PD}	Pulldown resistance	IN1/PH, IN2/EN, nSLEEP, nSCS, SCLK, SDI	64	100	173	kΩ
R_{PD}	Pulldown resistance	MODE		65		kΩ
R_{PU}	Pullup Resistance	MODE		26		kΩ
CONTROL OUTPUTS (nFAULT, WDFAULT, SDO)						
V_{OL}	Output logic-low voltage	I_O = 2 mA			0.1	V
I_{OZ}	Output high-impedance leakage	5V pullup voltage	-2		2	µA
FET GATE DRIVERS (GH1, GH2, SH1, SH2, GL1, GL2)						
V_{GSH}	High-side V_{GS} gate drive (gate-to-source)	V_{VM} > 13.5 V; V_{GSH} with respect to SHx		10.5	11.5	V
		V_{VM} = 8 V; V_{GSH} with respect to SHx	5.7		6.8	
		V_{VM} = 5.5 V; V_{GSH} with respect to SHx	3.4		4	
V_{GSL}	Low-side V_{GS} gate drive (gate-to-source)	V_{VM} > 10.5 V		10.5		V
		V_{VM} < 10.5 V	V_{VM} – 2			
$I_{DRIVE(SRC\_HS)}$	High-side peak source current (V_{VM} = 5.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702) or IDRIVE = 3’b000 (DRV8703)		10		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DRV8702) or IDRIVE = 3’b001 (DRV8703)		20		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DRV8702) or IDRIVE = 3’b010 (DRV8703)		50		
		IDRIVE = 3’b011 (DRV8703)		70		
		IDRIVE = 3’b100 (DRV8703)		100		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DRV8702) or IDRIVE = 3’b101 (DRV8703)		145		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DRV8702) or IDRIVE = 3’b110 (DRV8703)		190		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DRV8702) or IDRIVE = 3’b111 (DRV8703)		240		
$I_{DRIVE(SNK\_HS)}$	High-side peak sink current (V_{VM} = 5.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702) or IDRIVE = 3’b000 (DRV8703)		20		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DRV8702) or IDRIVE = 3’b001 (DRV8703)		40		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DRV8702) or IDRIVE = 3’b010 (DRV8703)		90		
		IDRIVE = 3’b011 (DRV8703)		120		
		IDRIVE = 3’b100 (DRV8703)		170		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DRV8702) or IDRIVE = 3’b101 (DRV8703)		250		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DRV8702) or IDRIVE = 3’b110 (DRV8703)		330		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DRV8702) or IDRIVE = 3’b111 (DRV8703)		420		

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRIVE(SRC\_LS)}$	Low-side peak source current (V_{VM} = 5.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702) or IDRIVE = 3’b000 (DRV8703)		10		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DRV8702) or IDRIVE = 3’b001 (DRV8703)		20		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DRV8702) or IDRIVE = 3’b010 (DRV8703)		40		
		IDRIVE = 3’b011 (DRV8703)		55		
		IDRIVE = 3’b100 (DRV8703)		75		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DRV8702) or IDRIVE = 3’b101 (DRV8703)		115		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DRV8702) or IDRIVE = 3’b110 (DRV8703)		145		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DRV8702) or IDRIVE = 3’b111 (DRV8703)		190		
$I_{DRIVE(SNK\_LS)}$	Low-side peak sink current (V_{VM} = 5.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702) or IDRIVE = 3’b000 (DRV8703)		20		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DRV8702) or IDRIVE = 3’b001 (DRV8703)		40		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DRV8702) or IDRIVE = 3’b010 (DRV8703)		85		
		IDRIVE = 3’b011 (DRV8703)		115		
		IDRIVE = 3’b100 (DRV8703)		160		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DRV8702) or IDRIVE = 3’b101 (DRV8703)		235		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DRV8702) or IDRIVE = 3’b110 (DRV8703)		300		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DRV8702) or IDRIVE = 3’b111 (DRV8703)		360		
$I_{DRIVE(SRC\_HS)}$	High-side peak source current (V_{VM} = 13.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702) or IDRIVE = 3’b000 (DRV8703)		10		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DRV8702) or IDRIVE = 3’b001 (DRV8703)		20		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DRV8702) or IDRIVE = 3’b010 (DRV8703)		50		
		IDRIVE = 3’b011 (DRV8703)		70		
		IDRIVE = 3’b100 (DRV8703)		105		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DRV8702) or IDRIVE = 3’b101 (DRV8703)		155		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DRV8702) or IDRIVE = 3’b110 (DRV8703)		210		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DRV8702) or IDRIVE = 3’b111 (DRV8703)		260		

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRIVE(SNK\_HS)}$	High-side peak sink current (V_{VM} = 13.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702) or IDRIVE = 3'b000 (DRV8703)		20		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DRV8702) or IDRIVE = 3'b001 (DRV8703)		40		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DRV8702) or IDRIVE = 3'b010 (DRV8703)		95		
		IDRIVE = 3'b011 (DRV8703)		130		
		IDRIVE = 3'b100 (DRV8703)		185		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DRV8702) or IDRIVE = 3'b101 (DRV8703)		265		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DRV8702) or IDRIVE = 3'b110 (DRV8703)		350		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DRV8702) or IDRIVE = 3'b111 (DRV8703)		440		
$I_{DRIVE(SRC\_LS)}$	Low-side peak source current (V_{VM} = 13.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702) or IDRIVE = 3'b000 (DRV8703)		10		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DRV8702) or IDRIVE = 3'b001 (DRV8703)		20		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DRV8702) or IDRIVE = 3'b010 (DRV8703)		45		
		IDRIVE = 3'b011 (DRV8703)		60		
		IDRIVE = 3'b100 (DRV8703)		90		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DRV8702) or IDRIVE = 3'b101 (DRV8703)		130		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DRV8702) or IDRIVE = 3'b110 (DRV8703)		180		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DRV8702) or IDRIVE = 3'b111 (DRV8703)		225		
$I_{DRIVE(SNK\_LS)}$	Low-side peak sink current (V_{VM} = 13.5V)	$R_{(IDRIVE)}$ < 1kΩ to GND (DRV8702-Q1) or IDRIVE = 3'b000 (DRV8703-Q1)		20		mA
		$R_{(IDRIVE)}$ = 33 kΩ to GND (DRV8702-Q1) or IDRIVE = 3'b001 (DRV8703-Q1)		40		
		$R_{(IDRIVE)}$ = 200 kΩ to GND (DRV8702-Q1) or IDRIVE = 3'b010 (DRV8703-Q1)		95		
		IDRIVE = 3'b011 (DRV8703-Q1)		125		
		IDRIVE = 3'b100 (DRV8703-Q1)		180		
		$R_{(IDRIVE)}$ > 2 MΩ to GND (DRV8702-Q1) or IDRIVE = 3'b101 (DRV8703-Q1)		260		
		$R_{(IDRIVE)}$ = 68 kΩ to AVDD (DRV8702-Q1) or IDRIVE = 3'b110 (DRV8703-Q1)		350		
		$R_{(IDRIVE)}$ = 1 kΩ to AVDD (DRV8702-Q1) or IDRIVE = 3'b111 (DRV8703-Q1)		430		
I_{HOLD}	FET holding current	Source current after t_{DRIVE}		10		mA
		Sink current after t_{DRIVE}		40		
I_{STRONG}	FET holdoff strong pulldown	GHx		750		mA
		GLx		1000		
$R_{(OFF)}$	FET gate holdoff resistor	Pulldown GHx to SHx		150		kΩ
		Pulldown GLx to GND		150		
CURRENT SHUNT AMPLIFIER AND PWM CURRENT CONTROL (SP, SN, SO, VREF)						
V_{VREF}	VREF input rms voltage	For current internal chopping	0.3[2]		3.6	V

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{VREF}	VREF input impedance	DRV8702-Q1 and DRV8703-Q1 VREF_SCL = 00 (100%)	1			MΩ
		DRV8703-Q1 VREF_SCL = 2’b01, 2’b10 or 2’b11		175		kΩ
A_V	Amplifier gain (DRV8702-Q1)	60 < V_{SP} < 225 mV; V_{SN} = GND	19.3	19.8	20.3	V/V
A_V	Amplifier gain (DRV8703-Q1)	GAIN_CS = 00; 10 < V_{SP} < 450 mV; V_{SN} = GND	9.75	10	10.25	V/V
		GAIN_CS = 01; 60 < V_{SP} < 225 mV; V_{SN} = GND	19.3	19.8	20.3	
		GAIN_CS = 10; 10 < V_{SP} < 112 mV; V_{SN} = GND	38.4	39.4	40.4	
		GAIN_CS = 11; 10 < V_{SP} < 56 mV; V_{SN} = GND	73	78	81	
V_{IO}	Input-referred offset	V_{SP} = V_{SN} = GND		5	10	mV
$V_{IO(DRIFT)}$	Drift offset[2]	V_{SP} = V_{SN} = GND		10		μV/°C
I_{SP}	SP input current	V_{SP} = 100 mV; V_{SN} = GND		–20		μA
V_{SO}	SO pin output voltage range		A_V × Vio		4.5	V
$C_{(SO)}$	Allowable SO pin capacitance				1	nF
PROTECTION CIRCUITS						
$V_{(UVLO2)}$	VM undervoltage lockout	VM falling; UVLO2 report		5.25	5.45	V
		VM rising; UVLO2 recovery		5.4	5.65	
$V_{(UVLO1)}$	Logic undervoltage lockout				4.5	V
$V_{hys(UVLO)}$	VM undervoltage hysteresis	Rising to falling threshold	100			mV
$V_{(CP\_UV)}$	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 1.5		V
		VCP rising; CPUV recovery		V_{VM} + 1.55		
$V_{hys(CP\_UV)}$	CP undervoltage hysteresis	Rising to falling threshold		50		mV
$V_{DS(OCP)}$	Overcurrent protection trip level, V_{DS} of each external FET (DRV8702-Q1) High side FETs: VDRAIN – SHx Low side FETs: SHx – SP/SL2	$R_{(VDS)}$ < 1 kΩ to GND		0.06		V
		$R_{(VDS)}$ = 33 kΩ to GND		0.12		
		$R_{(VDS)}$ = 200 kΩ to GND		0.24		
		$R_{(VDS)}$ > 2 MΩ to GND		0.48		
		$R_{(VDS)}$ = 68 kΩ to AVDD		0.96		
		$R_{(VDS)}$ < 1 kΩ to AVDD		Disabled		
$V_{DS(OCP)}$	Overcurrent protection trip level, V_{DS} of each external FET (DRV8703-Q1) High-side FETs: VDRAIN – SHx Low-side FETs: SHx – SP/SL2	VDS_LEVEL = 3’b000		0.06		V
		VDS_LEVEL = 3’b001		0.145		
		VDS_LEVEL = 3’b010		0.17		
		VDS_LEVEL = 3’b011		0.2		
		VDS_LEVEL = 3’b100		0.12		
		VDS_LEVEL = 3’b101		0.24		
		VDS_LEVEL = 3’b110		0.48		
		VDS_LEVEL = 3’b111		0.96		
$V_{SP(OCP)}$	Overcurrent protection trip level, measured by sense amplifier	V_{SP} with respect to GND	0.8	1	1.2	V
$T_{(OTW)}$	Thermal warning temperature[1]	Die temperature T_J	120	135	145	°C
T_{SD}	Thermal shutdown temperature[1]	Die temperature T_J	150			°C
T_{hys}	Thermal shutdown hysteresis[1]	Die temperature T_J		20		°C

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{C(GS)}$	Gate-drive clamping voltage	Positive clamping voltage	16.3	17	17.8	V
		Negative clamping voltage	–1	–0.7	–0.5	

(1) Ensured by design and characterization data.
(2) Operational at V_{VREF} = 0 to approximately 0.3 V, but accuracy is degraded.

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{(CLK)}$	Minimum SPI clock period	100			ns
$t_{(CLKH)}$	Clock high time	50			ns
$t_{(CLKL)}$	Clock low time	50			ns
$t_{(SU\_SDI)}$	SDI input data setup time	20			ns
$t_{(HD\_SDI)}$	SDI input data hold time	30			ns
$t_{(HD\_SDO)}$	SDO output hold time	40			ns
$t_{(SU\_SCS)}$	SCS setup time	50			ns
$t_{(HD\_SCS)}$	SCS hold time	50			ns
$t_{(HI\_SCS)}$	SCS minimum high time before SCS active low	400			ns

6.7 Switching Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, AVDD, DVDD)						
$t_{(SLEEP)}$	Sleep time	nSLEEP = low to sleep mode			100	µs
$t_{(wu)}$	Wake-up time	nSLEEP = high to output change			1	ms
t_{on}	Turn on time	VM > UVLO2 to output transition			1	ms
CHARGE PUMP (VCP, CPH, CPL)						
$f_{S(VCP)}$	Charge-pump switching frequency	VM > UVLO2	200	400	700	kHz
CONTROL INPUTS (IN1, IN2, nSLEEP, MODE, nSCS, SCLK, SDI, PH, EN)						
t_{pd}	Propagation delay	IN1, IN2 to GHx or GLx		500		ns
FET GATE DRIVERS (GH1, GH2, SH1, SH2, GL1, GL2)						
$t_{(DEAD)}$	Output dead time (DRV8702-Q1)	Observed $t_{(DEAD)}$ depends on IDRIVE setting		240		ns
$t_{(DEAD)}$	Output dead time (DRV8703-Q1)	TDEAD = 2’b00; Observed $t_{(DEAD)}$ depends on IDRIVE setting		120		ns
		TDEAD = 2’b01; Observed $t_{(DEAD)}$ depends on IDRIVE setting		240		
		TDEAD = 2’b10; Observed $t_{(DEAD)}$ depends on IDRIVE setting		480		
		TDEAD = 2’b11; Observed $t_{(DEAD)}$ depends on IDRIVE setting		960		
$t_{(DRIVE)}$	Gate drive time			2.5		µs
CURRENT SHUNT AMPLIFIER AND PWM CURRENT CONTROL (SP, SN, SO, VREF)						

Over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_S	Settling time to ±1%[1]	V_{SP} = V_{SN} = GND to V_{SP} = 240 mV, V_{SN} = GND, A_V= 10; $C_{(SO)}$ = 200 pF			0.5	µs
		V_{SP} = V_{SN} = GND to V_{SP} = 120 mV, V_{SN} = GND, A_V= 20; $C_{(SO)}$ = 200 pF			1	
		V_{SP} = V_{SN} = GND to V_{SP} = 60 mV, V_{SN} = GND, A_V= 40; $C_{(SO)}$ = 200 pF			2	
		V_{SP} = V_{SN} = GND to V_{SP} = 30 mV, V_{SN} = GND, A_V= 80; $C_{(SO)}$ = 200 pF			4	
t_{off}	PWM off-time (DRV8702-Q1)			25		µs
t_{off}	PWM off-time (DRV8703-Q1)	TOFF = 00		25		µs
		TOFF = 01		50		
		TOFF = 10		100		
		TOFF = 11		200		
$t_{(BLANK)}$	PWM blanking time			2		µs
PROTECTION CIRCUITS						
$t_{(UVLO)}$	VM UVLO falling deglitch time	VM falling; UVLO report		10		µs
$t_{(OCP)}$	Overcurrent deglitch time		3.7	4	4.3	µs
$t_{(RETRY)}$	Overcurrent retry time		2.8	3	3.2	ms
$t_{(WD)}$	Watchdog time out (DRV8703-Q1)	WD_DLY = 2’b00		10		ms
		WD_DLY = 2’b01		20		
		WD_DLY = 2’b10		50		
		WD_DLY = 2’b11		100		
$t_{(RESET)}$	Watchdog timer reset period			64		µs
SPI						
$t_{(SPI\_READY)}$	SPI read after power on	VM > VUVLO1		5	10	ms
$t_{d(SDO)}$	SDO output data delay time, CLK high to SDO valid	C_L = 20 pF			30	ns
t_a	SCS access time, SCS low to SDO out of high impedance			10		ns
t_{dis}	SCS disable time, SCS high to SDO high impedance			10		ns

(1) Ensured by design

6.8 Typical Characteristics

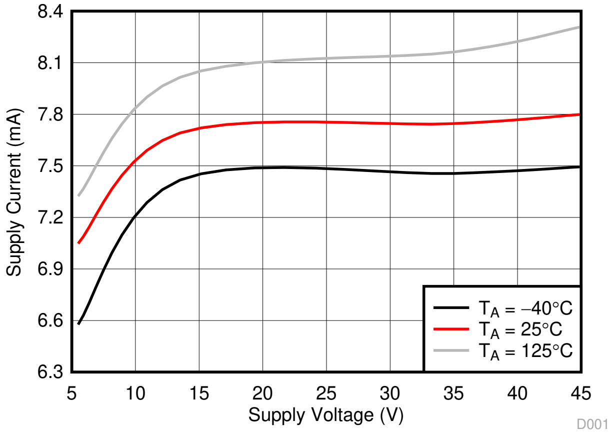


Figure 6-1. Supply Current vs Supply Voltage (VM)

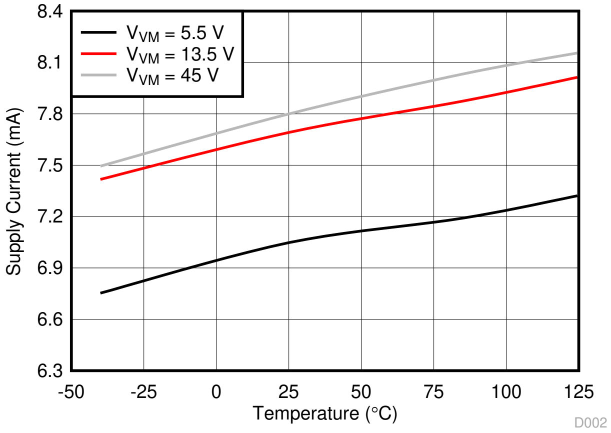


Figure 6-2. Supply Current vs Temperature

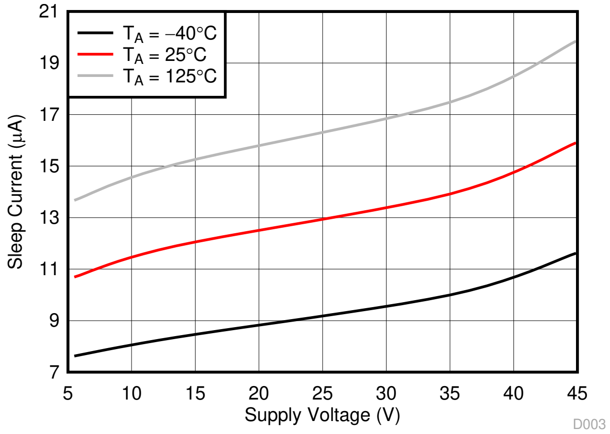


Figure 6-3. Sleep Current vs Supply Voltage (VM)

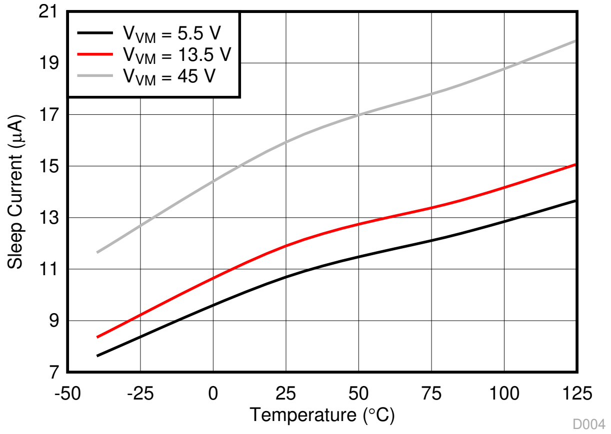
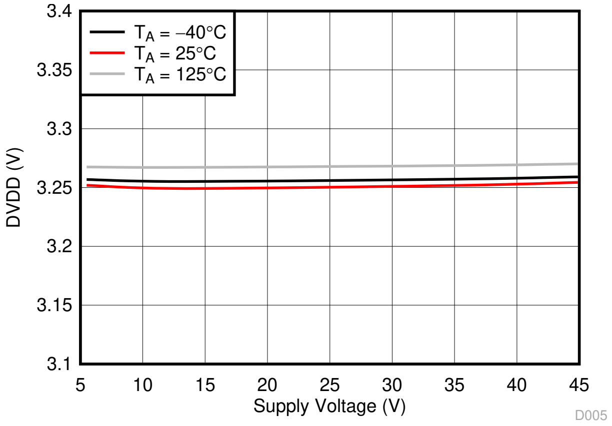
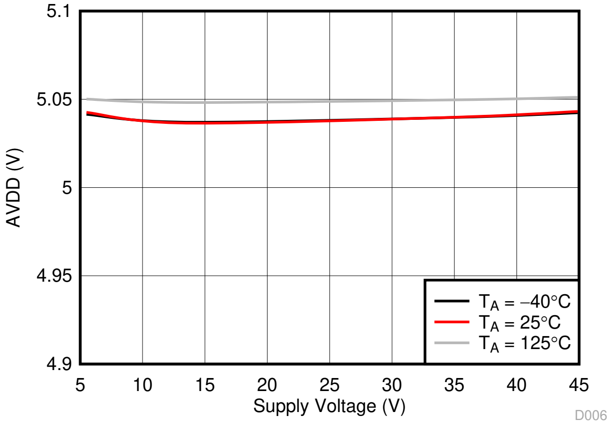


Figure 6-4. Sleep Current vs Temperature



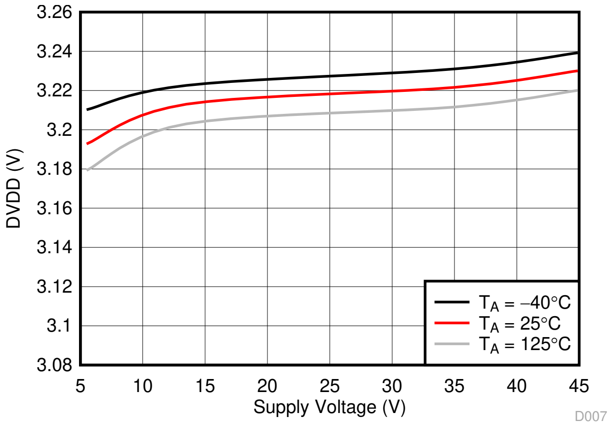
2-mA load

Figure 6-5. DVDD Regulator



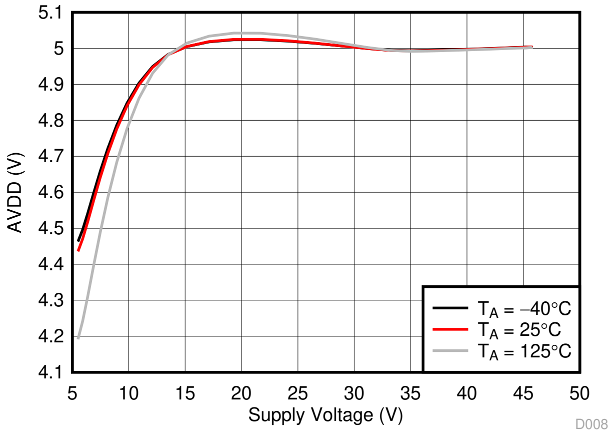
2-mA load

Figure 6-6. AVDD Regulator



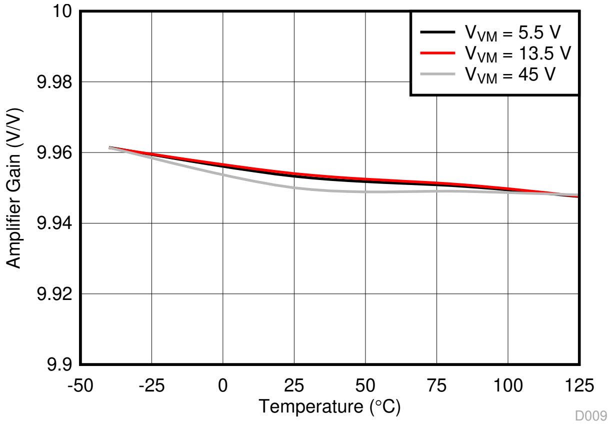
30-mA load

Figure 6-7. DVDD Regulator



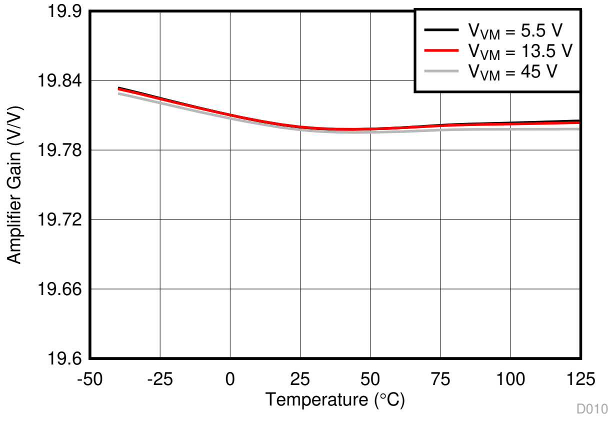
30-mA load

Figure 6-8. AVDD Regulator



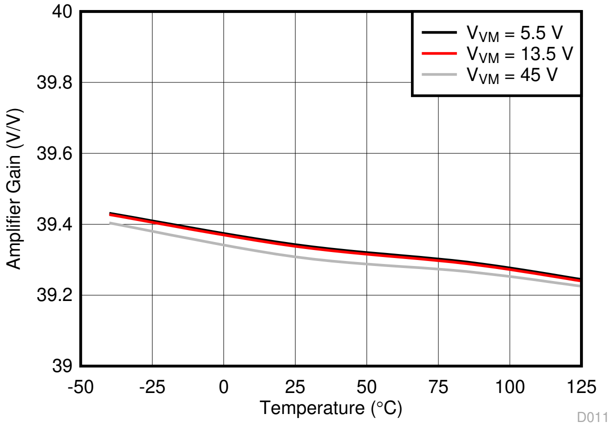
10-V/V gain

Figure 6-9. Amplifier Gain



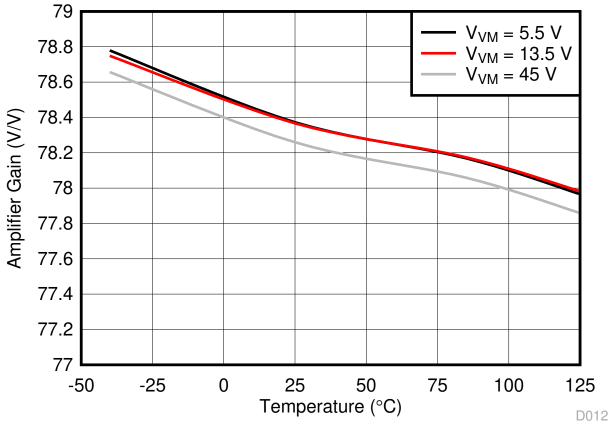
19.8-V/V gain

Figure 6-10. Amplifier Gain



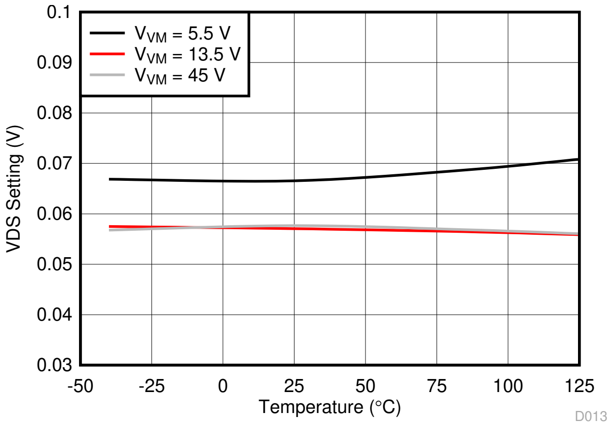
39.4-V/V gain

Figure 6-11. Amplifier Gain



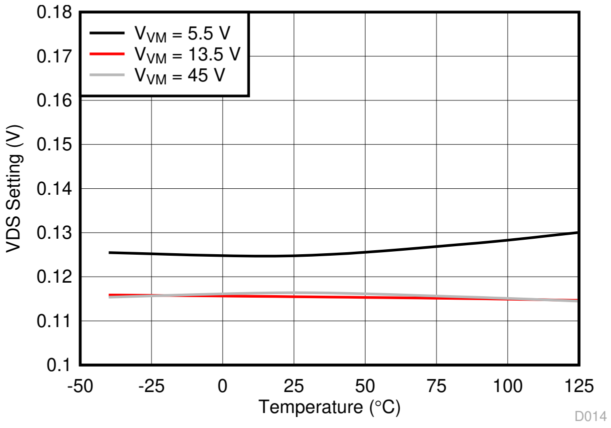
78-V/V gain

Figure 6-12. Amplifier Gain



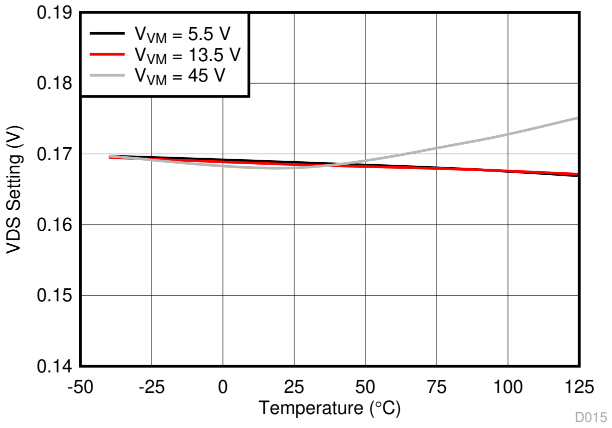
$V_{DS(OCP)}$ = 0.06 V

Figure 6-13. OCP Threshold Voltage



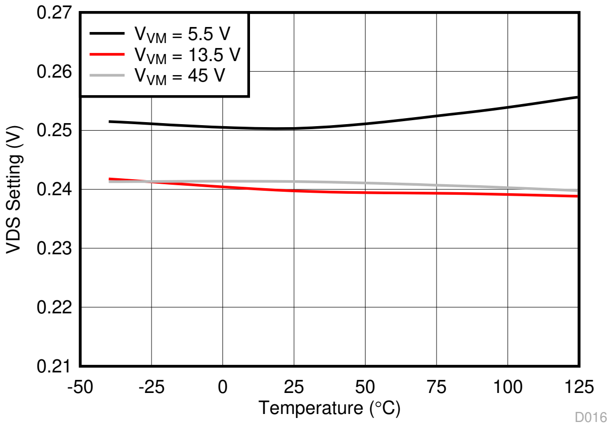
$V_{DS(OCP)}$ = 0.12 V

Figure 6-14. OCP Threshold Voltage



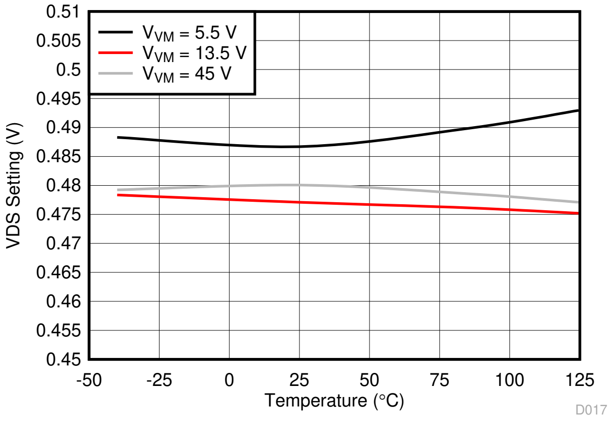
$V_{DS(OCP)}$ = 0.17 V

Figure 6-15. OCP Threshold Voltage



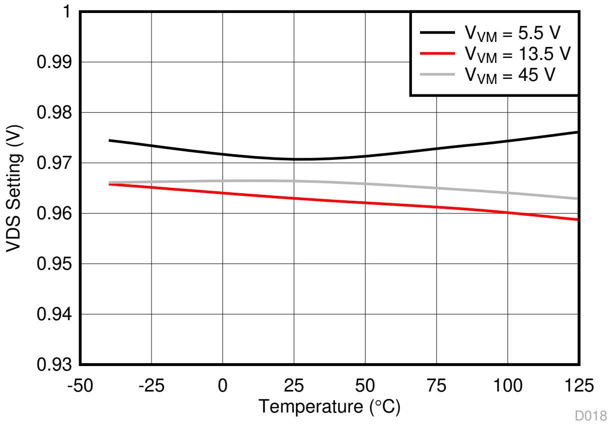
$V_{DS(OCP)}$ = 0.24 V

Figure 6-16. OCP Threshold Voltage



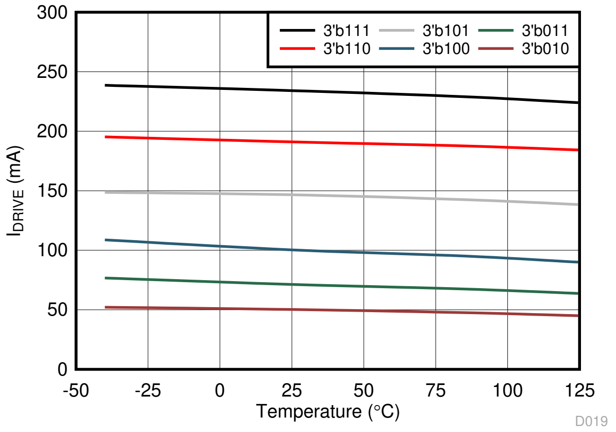
$V_{DS(OCP)}$ = 0.48 V

Figure 6-17. OCP Threshold Voltage



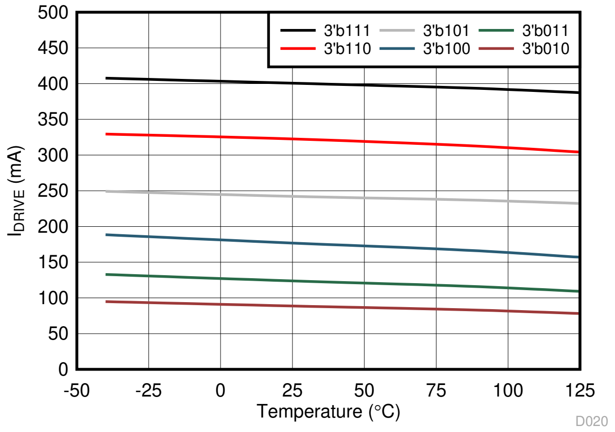
$V_{DS(OCP)}$ = 0.96 V

Figure 6-18. OCP Threshold Voltage



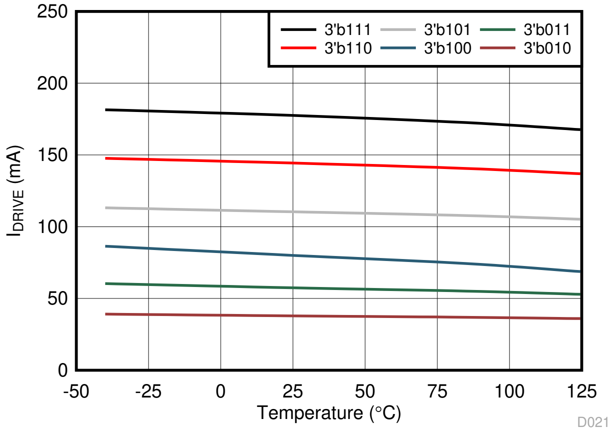
V_{VM} = 5.5 V

Figure 6-19. High-Side Source Current



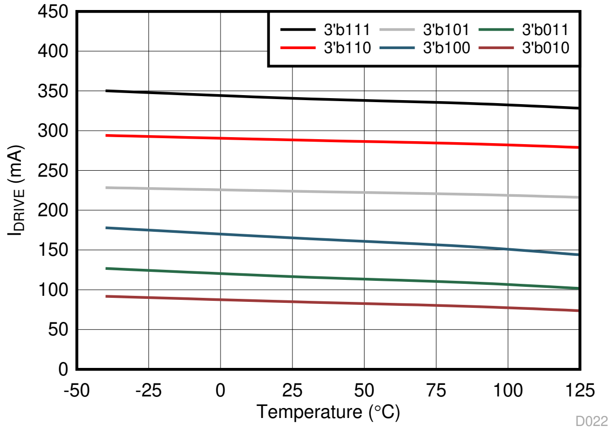
V_{VM} = 5.5 V

Figure 6-20. High-Side Sink Current



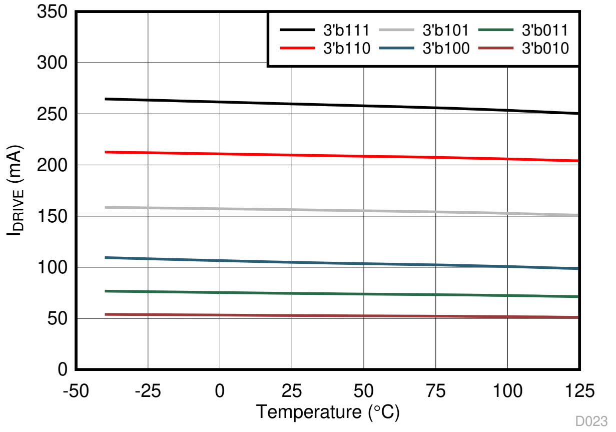
V_{VM} = 5.5 V

Figure 6-21. Low-Side Source Current



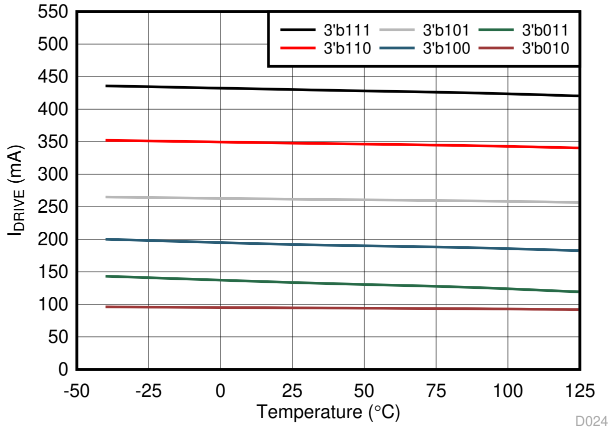
V_{VM} = 5.5 V

Figure 6-22. Low-Side Sink Current



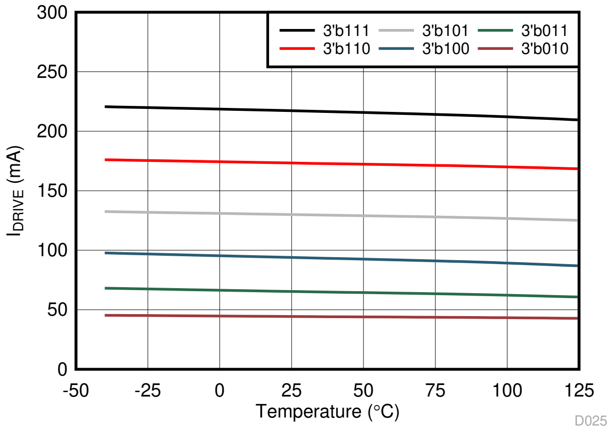
V_{VM} = 13.5 V

Figure 6-23. High-Side Source Current



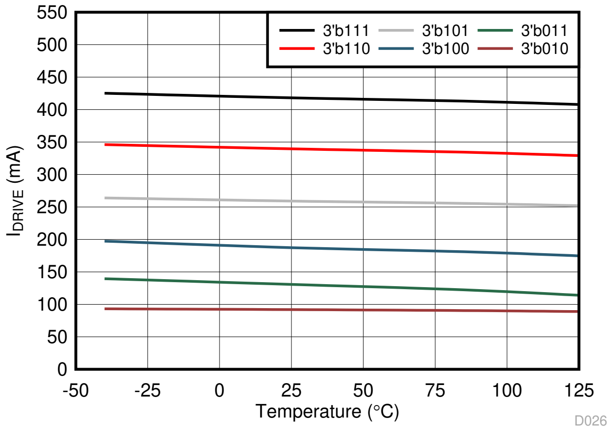
V_{VM} = 13.5 V

Figure 6-24. High-Side Sink Current



V_{VM} = 13.5 V

Figure 6-25. Low-Side Source Current



V_{VM} = 13.5 V

Figure 6-26. Low-Side Sink Current

7 Detailed Description

7.1 Overview

DRV87002-Q1 and DRV87003-Q1 are single H-bridge drivers, also referred to as gate controllers. The drivers control four external NMOS FETs used to drive a bi-directional brushed-DC motors. The devices can also operate in independent half bridge mode to drive two single directional brushed-DC motors.

The devices can support supply voltages from 5.5 V to 45 V and have a low power sleep mode enabled through the nSLEEP pin. There are three options for the interface modes including a configurable PH/EN, independent H-bridge control, or PWM interface. This allows easy interfacing to the controller circuit.

DRV87002-Q1 and DRV87003-Q1 include Smart Gate Drive technology which offers a combination of protection features and gate-drive configurability to improve design simplicity and bring a new level of intelligence to motor systems. The gate-drive strength, or gate-drive current can be adjusted through the driver itself to optimize for different FETs and applications without the need for external resistors. Smart Gate Drive significantly reduces the component count of discrete motor-driver systems by integrating the required FET drive circuitry into a single device. The peak current can be adjusted through the IDRIVE pin for DRV8702-Q1 and through SPI for DRV8703-Q1. Both the high-side and low-side FETs are driven with a gate source voltage (VGS) of 10.5 V (nominal) when the VM voltage is more than 13.5 V. At lower VM voltages, the VGS is reduced. The high-side gate drive voltage is generated using a doubler-architecture charge pump that regulates to the VM + 10.5 V.

The inrush or start up current and running current can be limited through a built in fixed time-off current chopping scheme. The chopping current level is set through the sense resistor by setting a voltage on the VREF pin. See the current regulation section for more information. A shunt-amplifier is also included in the devices to provide accurate current measurements to the system controller. The SO pin outputs a voltage that is approximately 20 times the voltage across the sense resistor on the DRV8702-Q1 device. For the DRV8703-Q1, this gain is configurable.

The DRV870x-Q1 device also has protection features beyond traditional discrete implementations including: undervoltage lockout (UVLO), overcurrent protection (OCP), gate driver faults, and thermal shutdown (TSD).

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature combined with output slew rate control minimizes the radiated emissions from the device.

7.2 Functional Block Diagram

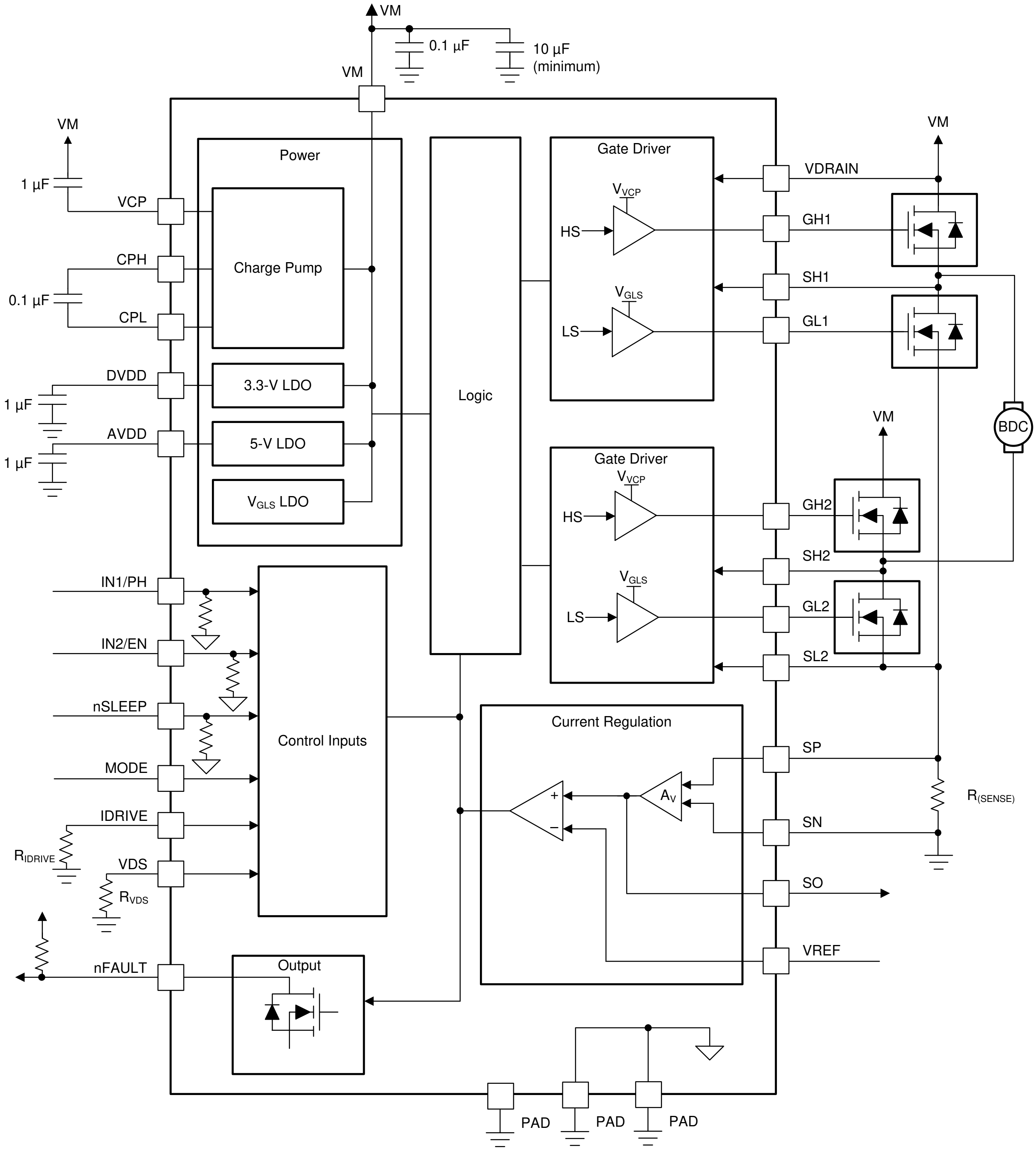


Figure 7-1. DRV8702-Q1 Functional Block Diagram

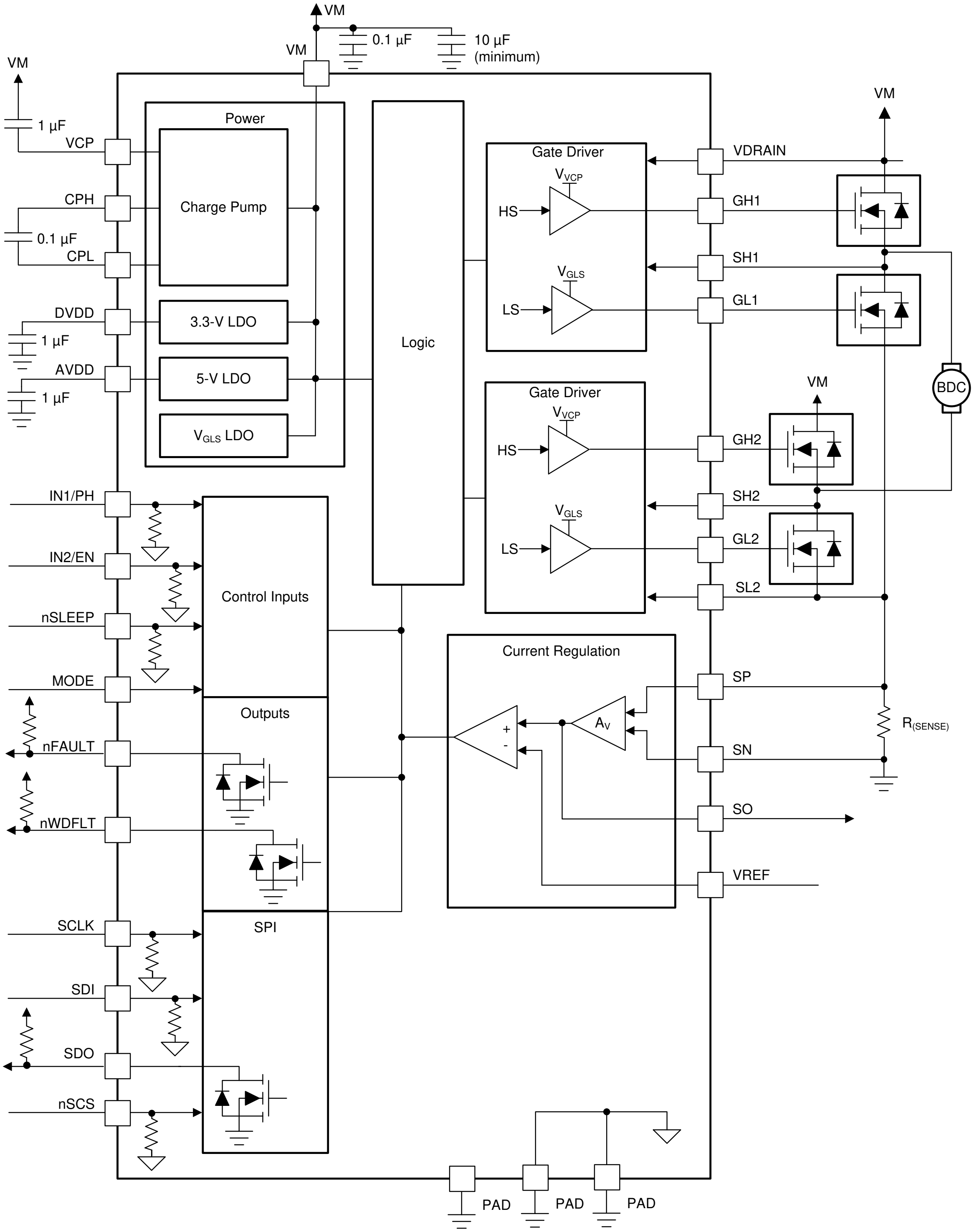


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Figure 7-2. DRV8703-Q1 Functional Block Diagram

7.3 Feature Description

Table 7-1 and Table 7-2 list the recommended external components for the device.

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
$C_{(VM1)}$	VM	GND	0.1-µF ceramic capacitor rated for VM
$C_{(VM2)}$	VM	GND	≥ 10-µF electrolytic capacitor rated for VM
$C_{(VCP)}$	VCP	VM	16-V, 1-µF ceramic capacitor
$C_{(SW)}$	CPH	CPL	0.1-µF X7R capacitor rated for VM
$C_{(DVDD)}$	DVDD	GND	6.3-V, 1-µF ceramic capacitor
$C_{(AVDD)}$	AVDD	GND	6.3-V, 1-µF ceramic capacitor
$R_{(IDRIVE)}$	IDRIVE	GND	For resistor sizing, see the *Section 8.2* section
$R_{(VDS)}$	VDS	GND	For resistor sizing, see the *Section 8.2* section
$R_{(nFAULT)}$	V_{CC} (1)	nFAULT	≥ 10 kΩ
$R_{(nWDFLT)}$	V_{CC} (1)	nWDFLT	≥ 10 kΩ
$R_{(SENSE)}$	SP	SN or GND	Optional low-side sense resistor
$R_{(VDRAIN)}$ (2)	VDRAIN	VM	100-Ω series resistor

(1) The V_{CC} pin is not a pin on the DRV870x-Q1, but a V_{CC} supply voltage pullup is required for open-drain outputs nFAULT. These pins can be pulled up to either AVDD or DVDD.

(2) The $R_{(VDRAIN)}$ resistor should be used between the VDRAIN and VM pins to minimize current to the VDRAIN pin if no external reverse battery protection is implemented on the VDRAIN pin.

Table 7-2. External Gates

COMPONENT	GATE	DRAIN	SOURCE	RECOMMENDED
$Q_{(HS1)}$	GH1	VM	SH1	Supports FETs up to 200 nC at 40 kHz PWM For more information, see *Section 8*
$Q_{(LS1)}$	GL1	SH1	SP or GND	
$Q_{(HS2)}$	GH2	VM	SH2	
$Q_{(LS2)}$	GL2	SH2	SP or GND	

7.3.1 Bridge Control

The DRV870x-Q1 device is controlled using a configurable input interface. The *Section 7.3.1.1* section provides the full H-bridge state . These tables do not consider the current control built into the DRV870x-Q1 device. Positive current is defined in the direction of SH1 → SH2. The logic operation set by the MODE pin is latched on power-up or when exiting sleep mode.

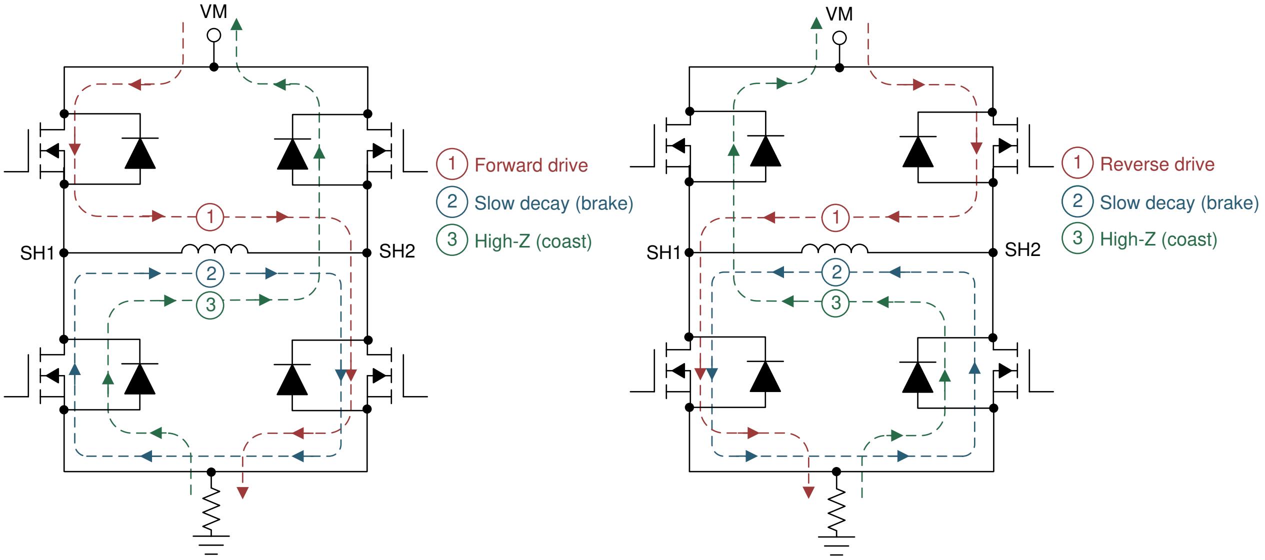


Figure 7-3. Bridge Control

7.3.1.1 Logic Tables

Table 7-3, Table 7-4, and Table 7-5 are the device logic tables. An *X* denotes a don't care input or output.

Table 7-3. DRV870x-Q1 PH and EN Control Interface (MODE = 0)

nSLEEP	IN1/PH	IN2/EN	GH1	GL1	SH1	GH2	GL2	SH2	AVDD/DVDD	DESCRIPTION
0	X	X	X	X	Hi-Z	X	X	Hi-Z	Disabled	Sleep mode H bridge disabled Hi-Z
1	X	0	0	1	L	0	1	L	Enabled	Brake low-side slow decay
1	0	1	0	1	L	1	0	H	Enabled	Reverse (Current SH2 → SH1)
1	1	1	1	0	H	0	1	L	Enabled	Forward (Current SH1 → SH2)

Table 7-4. DRV870x-Q1 Independent PWM Control Interface (MODE = 1)

nSLEEP	IN1/PH	IN2/EN	GH1	GL1	SH1	GH2	GL2	SH2	AVDD/DVDD	DESCRIPTION
0	X	X	X	X	Hi-Z	X	X	Hi-Z	Disabled	Sleep mode H bridge disabled Hi-Z
1	X	0	X	X	X	0	1	L	Enabled	Half-bridge 2 low side on
1	X	1	X	X	X	1	0	H	Enabled	Half-bridge 2 high side on
1	0	X	0	1	L	X	X	X	Enabled	Half-bridge 1 low side on
1	1	X	1	0	H	X	X	X	Enabled	Half-bridge 1 high side on

Table 7-5. DRV870x-Q1 Standard PWM Control Interface (MODE = Hi-Z)

nSLEEP	IN1/PH	IN2/EN	GH1	GL1	SH1	GH2	GL2	SH2	AVDD/DVDD	DESCRIPTION
0	X	X	X	X	Hi-Z	X	X	Hi-Z	Disabled	Sleep mode H bridge disabled Hi-Z
1	0	0	0	0	Hi-Z	0	0	Hi-Z	Enabled	Coast H bridge disabled Hi-Z
1	0	1	0	1	L	1	0	H	Enabled	Reverse (Current SH2 → SH1)
1	1	0	1	0	H	0	1	L	Enabled	Forward (Current SH1 → SH2)
1	1	1	0	1	L	0	1	L	Enabled	Brake low-side slow decay

7.3.2 MODE Pin

The MODE pin of the device determines the control interface and latches on power-up or when exiting sleep mode. Figure 7-4 shows an overview of the internal circuit of the MODE pin.

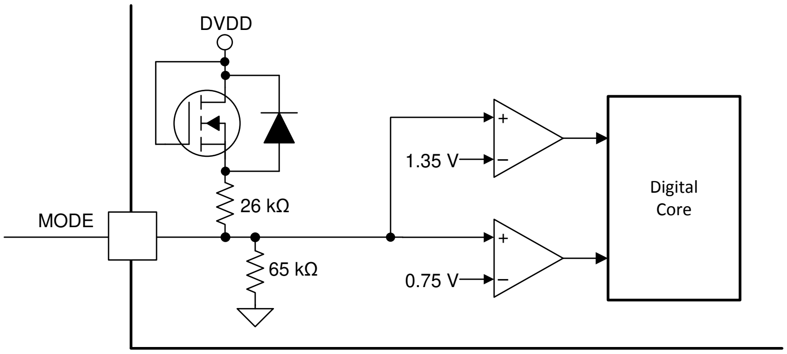


Figure 7-4. MODE Pin Block Diagram

Table 7-6 lists the different control interfaces that can be set via MODE pin at power-up or when exiting sleep mode.

Table 7-6. MODE Pin Configuration

MODE	CONTROL INTERFACE
0	PH or EN
1	Independent half-bridge
Hi-Z	PWM

During the device power-up sequence, the DVDD pin is enabled first. Then the MODE pin latches. Finally the AVDD pin is enabled. For setting PWM control interface, TI does not recommended connecting the MODE pin to the AVDD pin. Instead the MODE pin should be connected to an external 5-V or 3.3-V supply or to the DVDD pin if not driven by an external microcontroller (MCU).

7.3.3 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT line is logic low.

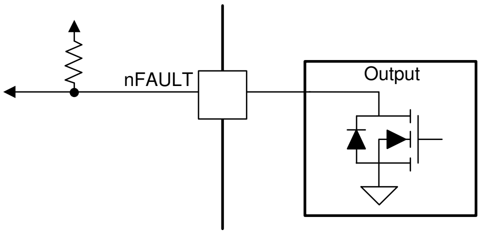


Figure 7-5. nFAULT Block Diagram

For a 3.3-V pullup the nFAULT pin can be tied to the DVDD pin with a resistor (refer to the *Section 8* section). For a 5-V pullup an external 5-V supply should be used. TI does not recommended connecting the nFAULT pin to the AVDD pin.

7.3.4 Current Regulation

The maximum current through the motor winding is regulated by a fixed off-time PWM current regulation or current chopping. When an H-bridge is enabled in forward or reverse drive, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. When the current hits the current chopping threshold, the bridge enters a brake (low-side slow decay) mode until the t_{off} time expires.

Note

Immediately after the current is enabled, the voltage on the SP pin is ignored for a period ($t_{(BLANK)}$) before enabling the current-sense circuitry.

The PWM chopping current is set by a comparator that compares the voltage across a current-sense resistor connected to the SP pin, multiplied by a factor of A_V, with a reference voltage from the VREF pin. The factor A_V is the shunt-amplifier gain, which is 19.8 V/V for the DRV8702-Q1 device or configurable to 10, 19.8, 39.4, or 78 V/V for the DRV8703-Q1 device.

Use Equation 1 to calculate the chopping current (I_{CHOP}).

$$I_{(CHOP)} \quad \frac{V_{VREF} - V_{IO} \times A_V}{A_V \times R_{(SENSE)}} \tag{1}$$

For example, if a 50-mΩ sense resistor and a VREF value of 3.3 V are selected, the full-scale chopping current is 3.28 A. The A_V is 19.8 V/V and V_{IO} is assumed to be 50 mV in this example.

For DC motors, current regulation is used to limit the start-up and stall current of the motor. If the current regulation feature is not needed, it can be disabled by tying the VREF pin directly to the AVDD pin. If the independent PWM control-interface mode (MODE pin is 1) is selected for operation, the device does not perform PWM current regulation or current chopping.

7.3.5 Amplifier Output (SO)

The SO pin on the DRV870x-Q1 device outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by A_V. The SO voltage is only valid for forward or reverse drive. Use Equation 2 to calculate the approximate current for the H-bridge.

$$I \quad \frac{V_{SO} - V_{IO} \times A_V}{A_V \times R_{(SENSE)}} \tag{2}$$

When the SP and SN voltages are 0 V, the SO pin outputs the amplifier offset voltage times the amplifier gain, $V_{io} \times Av$. When SP minus SN is greater than 0 V, the SO pin outputs the sum of the amplifier offset voltage and the sense resist or voltage, times the amplifier gain, $(V_{io} + V_{rsense}) \times Av$. No capacitor is required on the SO pin.

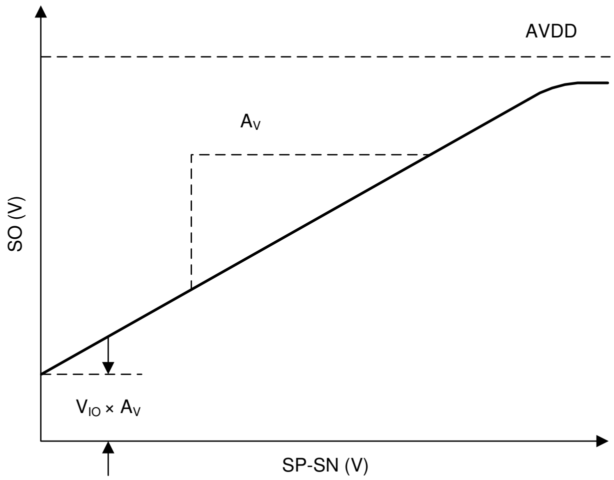


Figure 7-6. Current Sense Amplifier Output

If the voltage across the SP and SN pins exceeds 1 V, then the DRV870x-Q1 device flags an overcurrent condition.

The SO pin can source up to 5 mA of current. If the pin is shorted to ground, or if this pin drives a higher current load, the output functions as a constant-current source. The output voltage is not representative of the H-bridge current in this state.

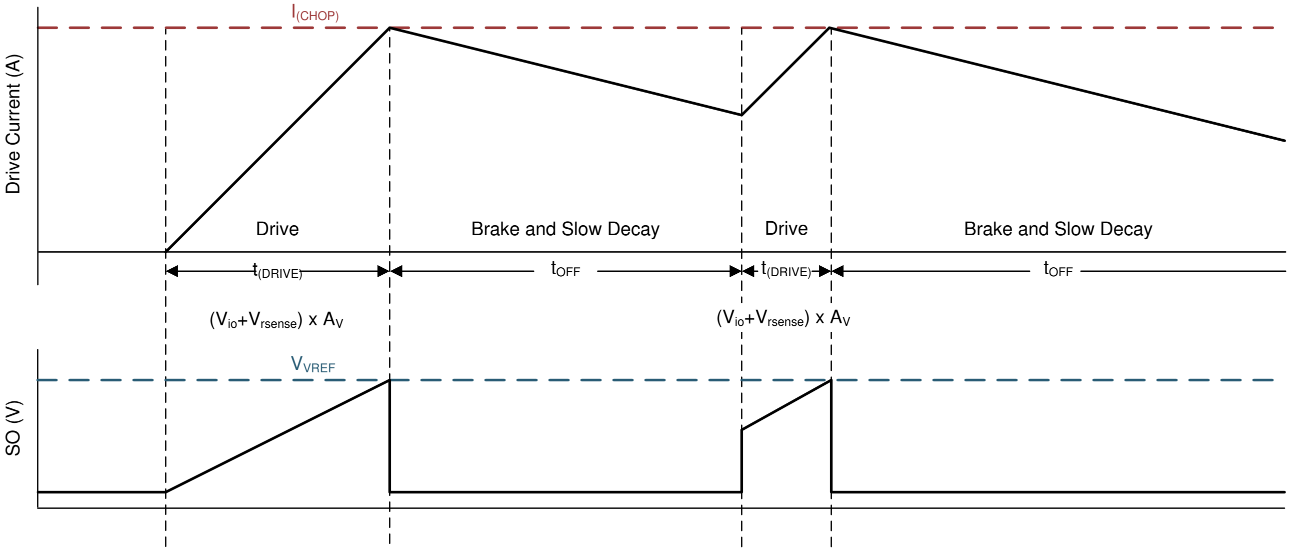


Figure 7-7. Current Sense Amplifier and Current Chopping Operation

During brake mode (slow decay), current is circulated through the low-side FETs. Because current is not flowing through the sense resistor, the SO pin does not represent the motor current.

7.3.5.1 SO Sample and Hold Operation

The DRV8703-Q1 device allows the shunt amplifier to operate in a sample and hold configuration. To enable this mode, set the SH_EN bit high through the SPI. In this mode, the shunt amplifier output is disabled to the Hi-Z state whenever the driver is in a brake mode. Place an external capacitor on this pin.

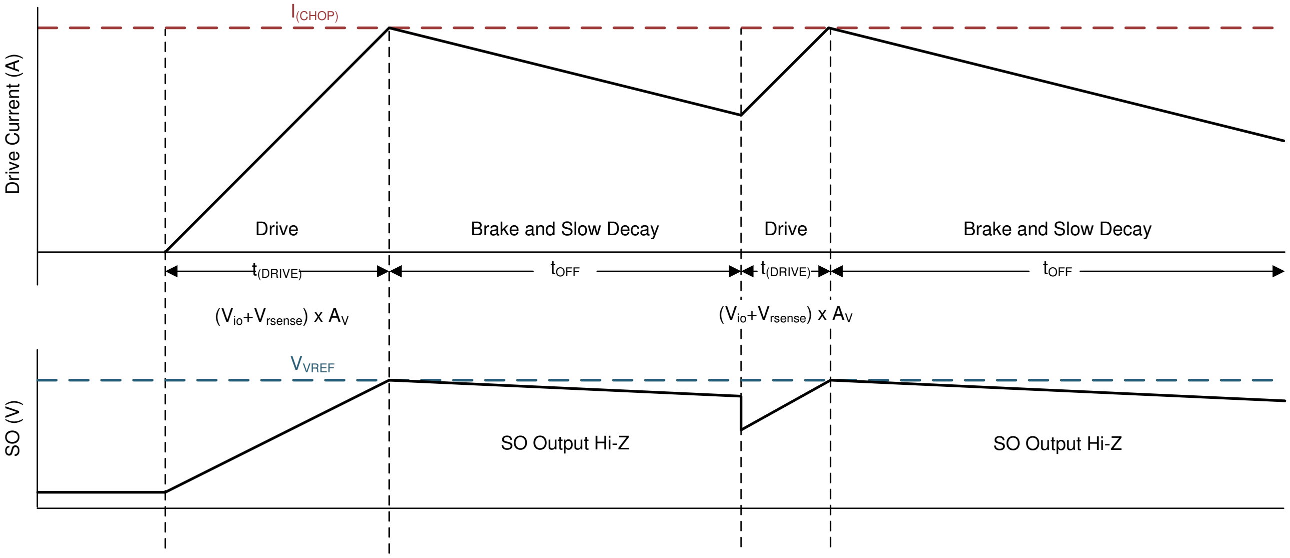


Figure 7-8. Sample and Hold Operation

7.3.6 PWM Motor Gate Drivers

The DRV870x-Q1 device has gate drivers for a single H-bridge with external NMOS FETs. Figure 7-9 shows a block diagram of the predrive circuitry.

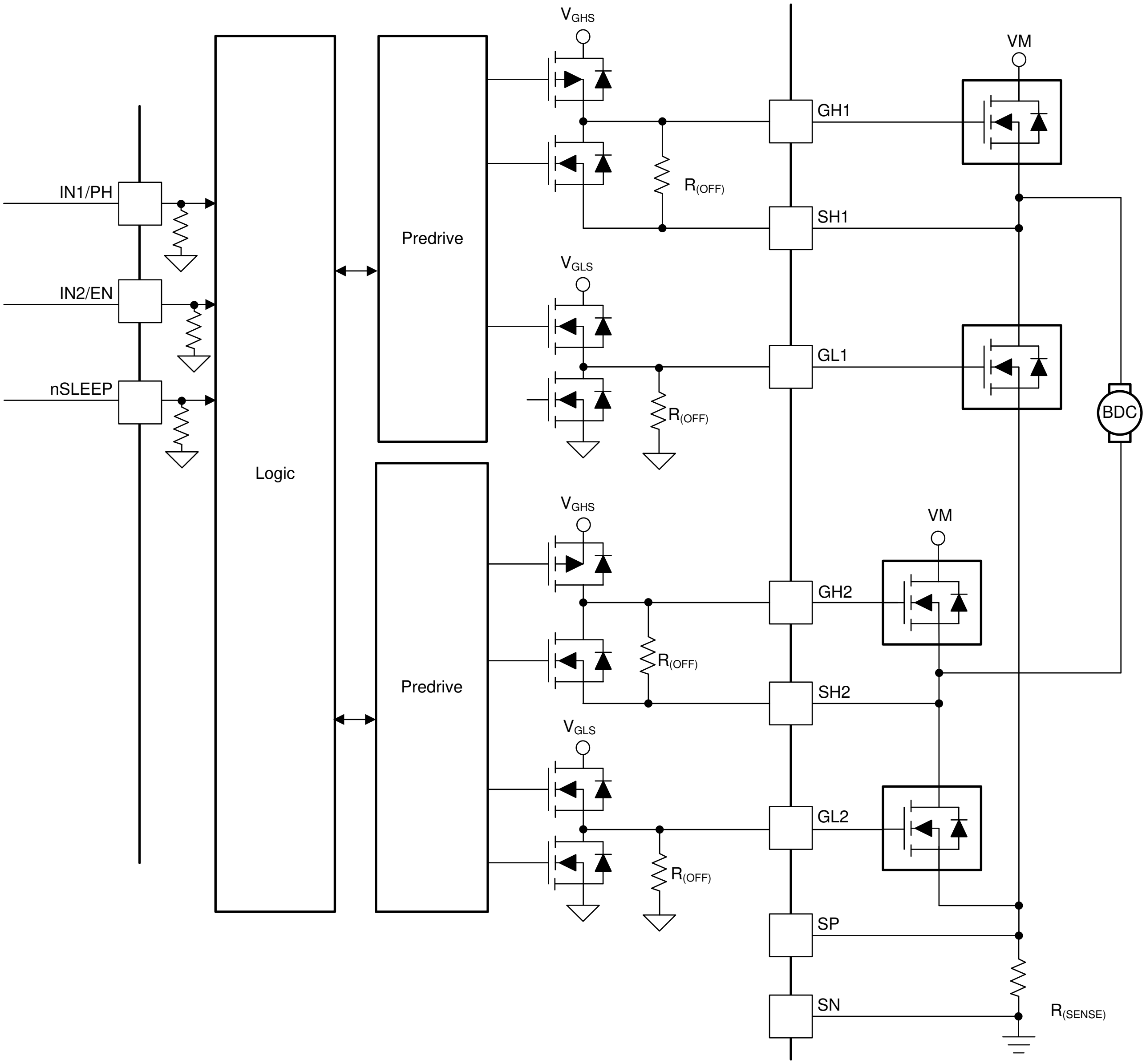


Figure 7-9. Predrive Block Diagram

Gate drivers inside the DRV870x-Q1 device directly drive N-Channel MOSFETs, which drive the motor current. The high-side gate drive is supplied by the charge pump, while an internal regulator generates the low-side gate drive.

The peak drive current of the gate drivers is adjustable through the IDRIVE pin for DRV8702-Q1 device or the IDRIVE register for the DRV8703-Q1 device. Peak source currents can be set to the values listed in the FET gate drivers section of the *Section 6.5* table. The peak sink current is approximately two times the peak source current. Adjusting the peak current changes the output slew rate, which also depends on the FET input capacitance and gate charge.

Fast switching times can cause extra noise on the VM and GND pins. This additional noise can occur specifically because of a relatively slow reverse-recovery time of the low-side body diode, when the body diode conducts reverse-bias momentarily, similar to shoot-through. Slow switching times can cause excessive power dissipation because the external FETs have a longer turn on and turn off time.

When changing the state of the output, the peak current (I_{DRIVE}) is applied for a short period ($t_{(DRIVE)}$), to charge the gate capacitance. After this time, a weak current source (I_{HOLD}) is used to keep the gate at the desired state. When selecting the gate drive strength for a given external FET, the selected current must be high enough to charge fully and discharge the gate during $t_{(DRIVE)}$, or excessive power is dissipated in the FET.

During high-side turn on, the low-side gate is pulled low with a strong pulldown (I_{STRONG}). This pulldown prevents the low-side FET Q_{GS} from charging and keeps the FET off, even when fast switching occurs at the outputs.

The gate-driver circuits include enforcement of a dead time in analog circuitry, which prevents the high-side and low-side FETs from conducting at the same time. When the switching FETs are on, this handshaking prevents the high-side or low-side FET from turning on until the opposite FET turns off.

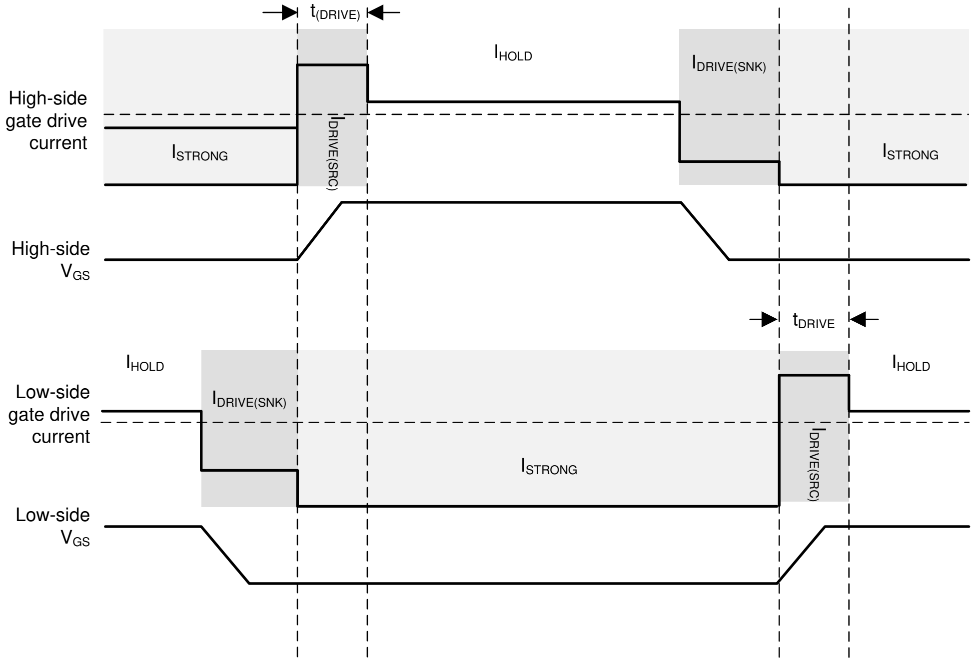


Figure 7-10. Gate Driver Output to Control External FETs

7.3.6.1 Miller Charge (Q_{GD})

When a FET gate turns on, the following capacitances must be charged:

- Gate-to-source charge, Q_{GS}
- Gate-to-drain charge, Q_{GD} (Miller charge)
- Remaining Q_G

The FET output is slewing primarily during the Q_{GD} charge.

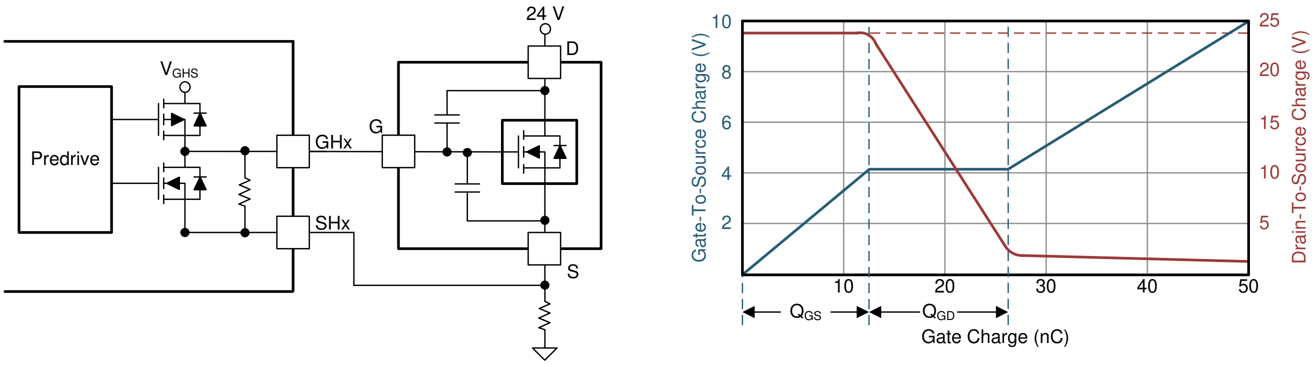


Figure 7-11. FET Gate Charging Profile

7.3.7 IDRIVE Pin (DRV8702-Q1 Only)

The rise and fall times of the H-bridge output (SHx pins) can be adjusted by setting the IDRIVE resistor value or forcing a voltage onto the IDRIVE pin. The FET gate voltage ramps faster if a higher IDRIVE setting is selected. The ramp of the FET gate directly affects the rise and fall times of the H-bridge output.

Tying the IDRIVE pin to ground selects the lowest drive setting of 10-mA source and 20-mA sink. Leaving this pin open selects the drive setting of 155-mA high side and 130-mA low side for source current, and 265-mA high side, 260-mA low side for sink current, at a VM voltage of 13.5 V. For a detailed list of IDRIVE configurations, see Table 7-7.

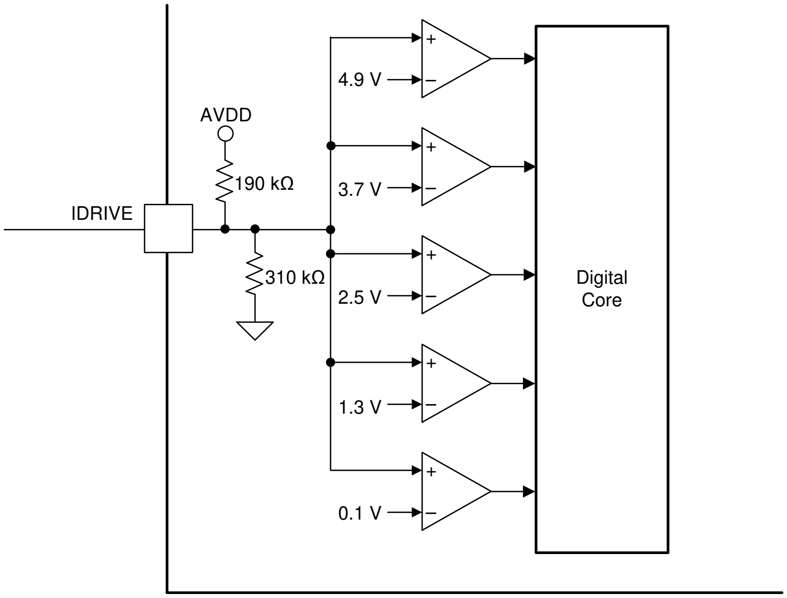
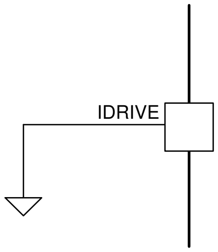
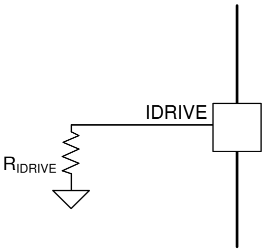
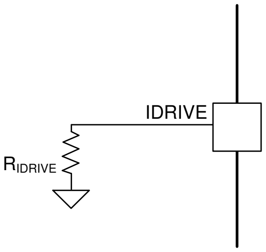
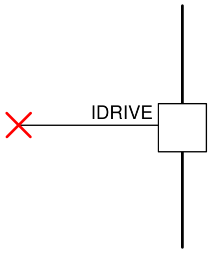
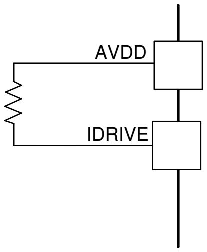
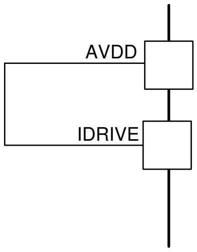


Figure 7-12. IDRIVE Pin Internal Circuitry

Table 7-7. DRV8702-Q1 IDRIVE Settings

IDRIVE RESISTANCE	IDRIVE VOLTAGE	SOURCE CURRENT		SINK CURRENT		CIRCUIT
		V_{VM} = 5.5 V	V_{VM} = 13.5 V	V_{VM} = 5.5 V	V_{VM} = 13.5 V	
< 1 kΩ to GND	GND	High-side: 10 mA Low-side: 10 mA	High-side: 10 mA Low-side: 10 mA	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA	
33 kΩ ± 5% to GND	0.7 V ± 5%	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA	High-side: 40 mA Low-side: 40 mA	High-side: 40 mA Low-side: 40 mA	
200 kΩ ± 5% to GND	2 V ± 5%	High-side: 50 mA Low-side: 40 mA	High-side: 50 mA Low-side: 45 mA	High-side: 90 mA Low-side: 85 mA	High-side: 95 mA Low-side: 95 mA	
> 2 MΩ to GND, Hi-Z	3 V ± 5%	High-side: 145 mA Low-side: 115 mA	High-side: 155 mA Low-side: 130 mA	High-side: 250 mA Low-side: 235 mA	High-side: 265 mA Low-side: 260 mA	
68 kΩ ± 5% to AVDD	4 V ± 5%	High-side: 190 mA Low-side: 145 mA	High-side: 210 mA Low-side: 180 mA	High-side: 330 mA Low-side: 300 mA	High-side: 350 mA Low-side: 350 mA	
< 1 kΩ to AVDD	AVDD	High-side: 240 mA Low-side: 190 mA	High-side: 260 mA Low-side: 225 mA	High-side: 420 mA Low-side: 360 mA	High-side: 440 mA Low-side:430 mA	

7.3.8 Dead Time

The dead time ($t_{(DEAD)}$) is measured as the time when the SHx pin is in the Hi-Z state between turning off one of the H-bridge FETs and turning on the other. For example, the output is Hi-Z between turning off the high-side FET and turning on the low-side FET.

The dead time consists of an inserted digital dead time and FET gate slewing. The DRV8702-Q1 device has a digital dead time of approximately 240 ns. The DRV8703-Q1 device has programmable dead-time options of 120, 240, 480, 960 ns. In addition to this digital dead time, the output is Hi-Z as long as the voltage across the GLx pin to ground or GHx pin to SHx pin is less than the FET threshold voltage.

The total dead time is dependent on the IDRIVE resistor setting because a portion of the FET gate ramp (GHx and GLx pins) includes the observable dead time.

7.3.9 Propagation Delay

The propagation delay time (t_{PD}) is measured as the time between an input edge to an output change. This time is composed of two parts: an input deglitcher and output slewing delay. The input deglitcher prevents noise on the input pins from affecting the output state.

The gate drive slew rate also contributes to the delay time. For the output to change state during normal operation, one FET must first be turned off. The FET gate is ramped down according to the IDRIVE resistor selection, and the observed propagation delay ends when the FET gate falls below the threshold voltage.

7.3.10 Overcurrent VDS Monitor

The gate-driver circuit monitors the VDS voltage of each external FET when it is driving current. When the voltage monitored is greater than the OCP threshold voltage ($V_{DS(OCP)}$) after the OCP deglitch time has expired, an OCP condition is detected. The $V_{DS(OCP)}$ voltage can be adjusted by changing the resistor (R_{VDS}) on the VDS pin of the DRV8702-Q1 device. The DRV8703-Q1 device provides $V_{DS(OCP)}$ voltage levels by setting the VDS register.

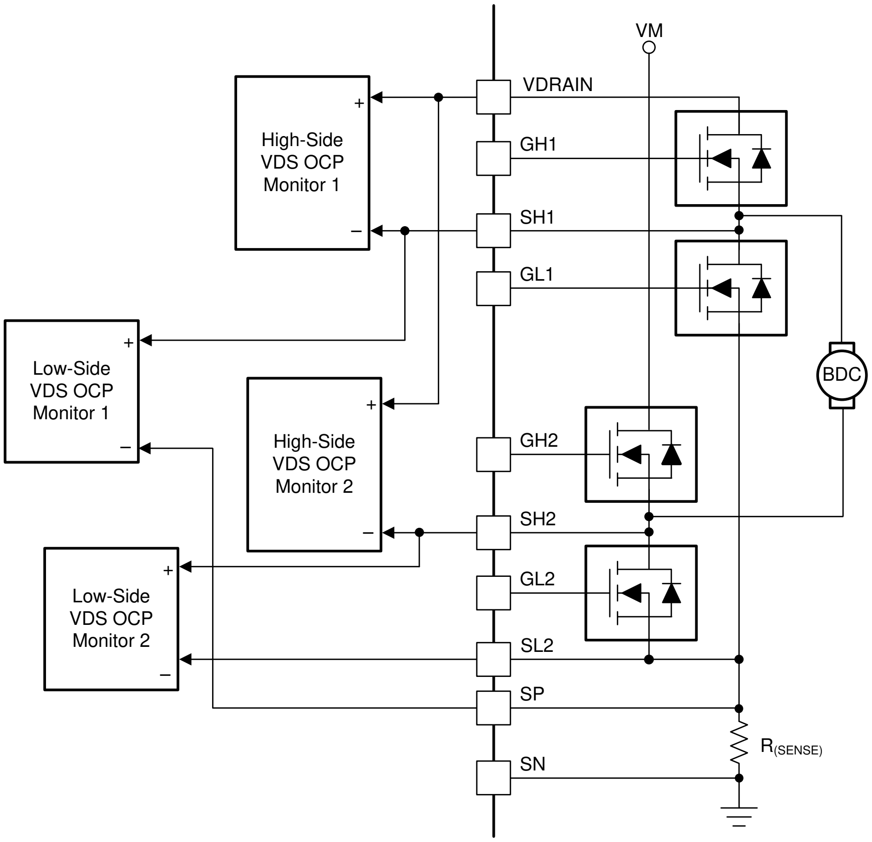


Figure 7-13. $V_{DS(OCP)}$ Block Diagram

The VDS voltage on the high-side FET is measured across the VDRAIN to SHx pins. The low-side VDS monitor on half-bridge 1 measures the VDS voltage across the SH1 to SP pins. The low-side VDS monitor on half-bridge 2 measures the VDS voltage across the SH2 to SL2 pins. Ensure that the SP pin is always connected to the source of the low-side FET of half-bridge 1, even when the sense amplifier is not used.

7.3.11 VDS Pin (DRV8702-Q1 Only)

The VDS pin on the DRV8702-Q1 device is used to select the VDS threshold voltage for overcurrent detection.

Tying the VDS pin to ground selects the lowest setting of 0.06 V. Leaving this pin open selects the setting of 0.48 V. Tying the VDS pin to the AVDD the pin disables the VDS monitor. For a detailed list of VDS configurations, see Table 7-8.

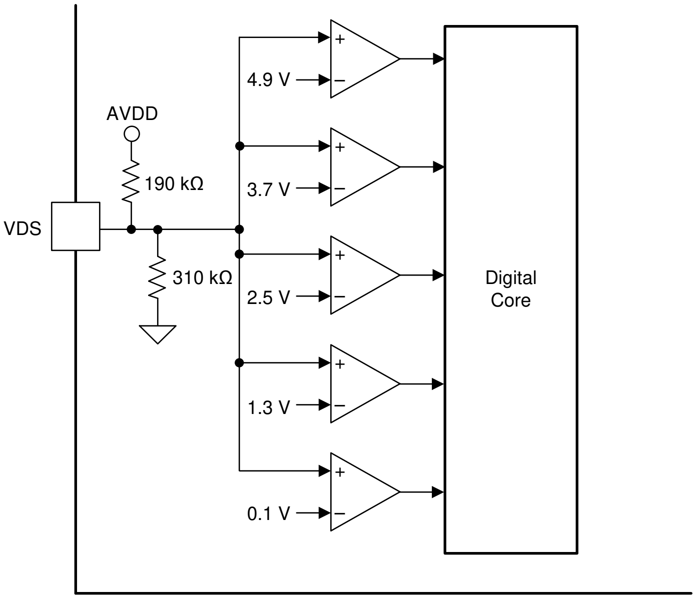
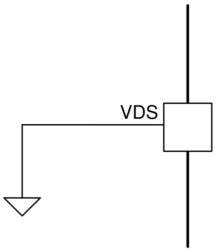
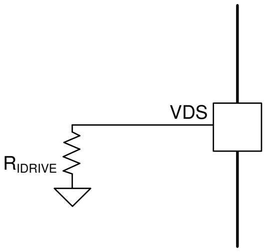
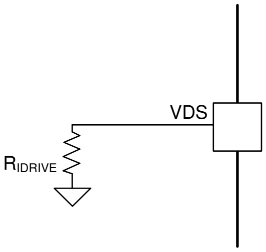
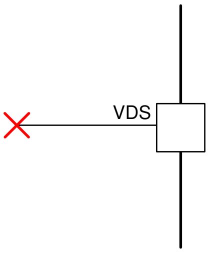
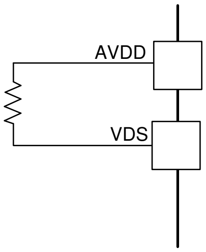
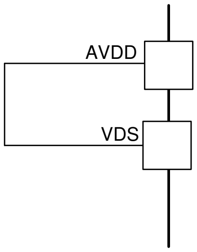


Figure 7-14. VDS Block Diagram

Table 7-8. VDS Pin Resistor Setting

VDS RESISTANCE	VDS VOLTAGE	OVERCURRENT TRIP LEVEL $(V_{DS(OCP)})$	CIRCUIT
< 1 kΩ to GND	GND	0.06 V	
33 kΩ ± 5% to GND	0.7 V ± 5%	0.12 V	
200 kΩ ± 5% to GND	2 V ± 5%	0.24 V	
> 2 MΩ to GND, Hi-Z	3 V ± 5%	0.48 V	
68 kΩ ± 5% to AVDD	4 V ± 5%	0.96 V	
< 1 kΩ to AVDD	AVDD	Disabled	

7.3.12 Charge Pump

A charge pump is integrated to supply the gate drive voltage of a high-side NMOS (V_{GSH}). The charge pump requires a capacitor between the VM and VCP pins. Additionally, a low-ESR ceramic capacitor is required between the CPH and CPL pins. When the VM voltage is below 13.5 V, this charge pump functions as a doubler and generates a V_{VCP} equal to 2 × V_{VM} – 1.5 V if unloaded. When the VM voltage is more than 13.5 V, the charge pump regulates V_{VCP} such that it is equal to V_{VM} + 10.5 V.

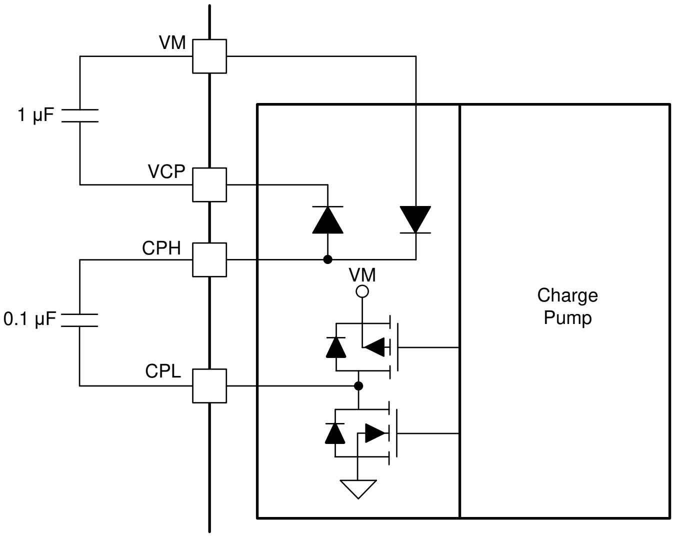


Figure 7-15. Charge Pump Block Diagram

7.3.13 Gate Drive Clamp

A clamping structure limits the gate-drive output voltage to the $V_{C(GS)}$ voltage to protect the power FETs from damage. The positive voltage clamp is realized using a series of diodes. The negative voltage clamp uses the body diodes of the internal predriver FET.

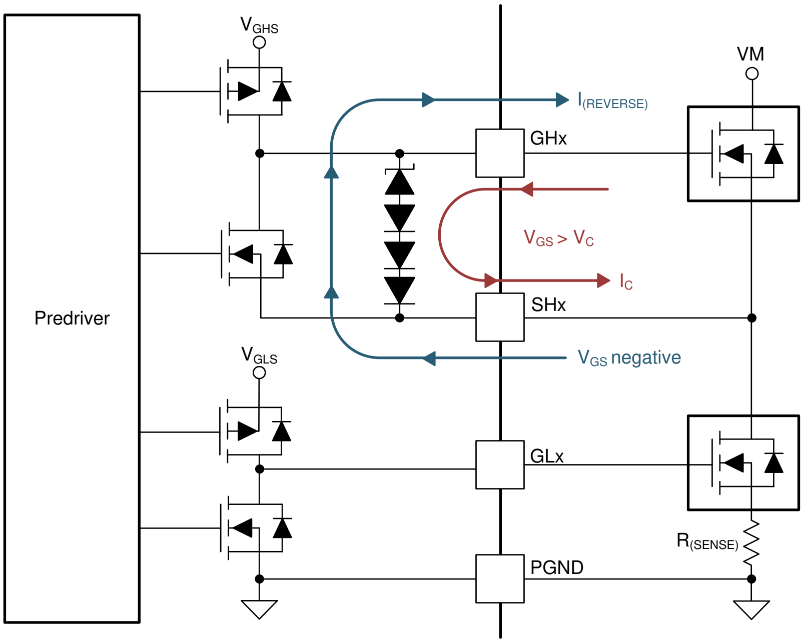


Figure 7-16. Gate Drive Clamp

7.3.14 Protection Circuits

The DRV870x-Q1 device is protected against VM undervoltage, charge-pump undervoltage, overcurrent, gate-driver shorts, and overtemperature events.

7.3.14.1 VM Undervoltage Lockout (UVLO2)

If the voltage on the VM pin falls below the VM undervoltage lockout threshold voltage (V_{UVLO2}), all FETs in the H-bridge are disabled, the charge pump is disabled, and the nFAULT pin is driven low. The VM_UVFL bit of the DRV8703-Q1 device is set. The operation resumes when the VM voltage rises above the UVLO2 threshold. The nFAULT pin is released after the operation resumes but the VM_UVFL bit on the DRV8703-Q1 device remains set until cleared by writing to the CLR_FLT bit.

The SPI settings on the DRV8703-Q1 device are not reset by this fault even though the output drivers are disabled. The settings are maintained and internal logic remains active until the VM voltage falls below the logic undervoltage threshold (VUVLO1).

7.3.14.2 Logic Undervoltage (UVLO1)

If the voltage on the VM pin falls below the logic undervoltage threshold voltage (V_{UVLO1}), the internal logic is reset. The operation resumes when the VM voltage rises above the UVLO1 threshold. The nFAULT pin is logic low during this state because it is pulled low when the VM undervoltage condition occurs. Decreasing the VM voltage below this undervoltage threshold resets the SPI settings.

7.3.14.3 VCP Undervoltage Lockout (CPUV)

If the voltage on the VCP pin falls below the threshold voltage of the charge-pump undervoltage (CPUV) lockout, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The DRV8703-Q1 the VCP_UVFL bit is set. The operation resumes when the VCP voltage rises above the CPUV threshold. The nFAULT pin is released after the operation resumes but the VCP_UVFL bit on the DRV8703-Q1 device remains set until cleared by writing to the CLR_FLT bit.

7.3.14.4 Overcurrent Protection (OCP)

Overcurrent is sensed by monitoring the VDS voltage drop across the external FETs. If the voltage across a driven FET exceeds the $V_{DS(OCP)}$ level for longer than the OCP deglitch time, an OCP event is recognized. All FETs in the H-bridge are disabled, and the nFAULT pin is driven low. The OCP bit of the DRV8703-Q1 device is set. The drive re-enables after the $t_{(RETRY)}$ time has passed. The nFAULT pin becomes high again after the retry time.

If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and the nFAULT pin goes high. The OCP bit on the DRV8703-Q1 remains set until cleared by writing to the CLR_FLT bit. In addition to this FET VDS monitor, an overcurrent condition is detected if the voltage at the SP pin exceeds $V_{SP(OCP)}$ and the nFAULT pin is driven low. The OCP bit in the DRV8703-Q1 device is set.

7.3.14.5 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external FET gate does not increase or decrease after the $t_{(DRIVE)}$ time, a gate driver fault is detected. This fault occurs if the GHx or GLx pins are shorted to the GND, SHx, or VM pin. Additionally, a gate-driver fault occurs if the selected IDRIVE setting is not sufficient to turn on the external FET. All FETs in the H-bridge are disabled, and the nFAULT pin is driven low. The GDF bit of the DRV8703-Q1 device is set. The driver re-enables after the OCP retry period ($t_{(RETRY)}$) has passed. The nFAULT pin is released after the operation has resumed but the GDF bit on the DRV8703-Q1 device remains set until cleared by writing to the CLR_FLT bit.

7.3.14.6 Thermal Shutdown (TSD)

If the die temperature exceeds the T_{SD} temperature, all FETs in the H-bridge are disabled, the charge pump shuts down, the AVDD regulator is disabled, and the nFAULT pin is driven low. The OTSD bit of the DRV8703-Q1 device is set as well. After the die temperature falls below T_{SD} – T_{hys} temperature, device operation automatically resumes. The nFAULT pin is released after the operation resumes, but the OTSD bit on the DRV8703-Q1 device remains set until cleared by writing to the CLR_FLT bit.

7.3.14.7 Watchdog Fault (WDFLT, DRV8703-Q1 Only)

An MCU watchdog function can be enabled to ensure that the external controller that is instructing the DRV8703-Q1 device is active and in a known state. The SPI watchdog must be enabled by writing a 1 to the WD_EN bit through the SPI (disabled by default, bit is 0). When the watchdog is enabled, an internal timer starts to count down to an interval set by the WD_DLY bits. The register address 0x00 must be read by the MCU within the interval set by the WD_DLY bit to reset the watchdog. If the timer is allowed to expire, the nWDFLT pin is enabled. When the nWDFLT pin is enabled the following occurs:

- The nWDFLT pin goes low for 64 µs.
- The nFAULT pin is asserted.
- The WD_EN bit is cleared.
- The drivers are disabled.

The WDFLT bit remains asserted, and operation is halted until the CLR_FLT bit has been written to 1.

Table 7-9 lists the fault responses of the device under the fault conditions.

Table 7-9. Fault Response

FAULT	CONDITION	H-BRIDGE	CHARGE PUMP	AVDD	DVDD	RECOVERY
VM undervoltage (UVLO)	$V_{VM} \leq V_{(UVLOx)}$ (5.45 V, max)	Disabled	Disabled	Disabled	Operating	$V_{VM} \geq V_{(UVLOx)}$ (5.65 V, max)
VCP undervoltage (CPUV)	$V_{VCP} \leq V_{(CP\_UV)}$ (V_{VM} + 1.5, typ)	Disabled	Operating	Operating	Operating	$V_{VCP} \geq V_{(CP\_UV)}$ (V_{VM} + 1.5, typ)
External FET overload (OCP)	$V_{DS} \geq V_{DS(OCP)}$ $V_{SP} - V_{SN} > 1$ V	Disabled	Operating	Operating	Operating	$t_{(RETRY)}$
Gate driver fault (GDF)	Gate voltage unchanged after $t_{(DRIVE)}$	Disabled	Operating	Operating	Operating	$t_{(RETRY)}$
Watchdog fault (WDFLT)	Watchdog timer expires	Disabled	Operating	Operating	Operating	CLR_FLT bit
Thermal shutdown (TSD)	$T_J \geq T_{SD}$ (150°C, min)	Disabled	Disabled	Disabled	Operating	$T_J \leq T_{SD} - T_{hys}$ (T_{hys} is typically 20°C)

7.3.14.8 Reverse Supply Protection

The circuit in Figure 7-17 can be implemented to help protect the system from reverse supply conditions. This circuit requires the following additional components:

- NMOS FET
- NPN BJT
- Diode
- 10-kΩ resistor
- 43-kΩ resistor

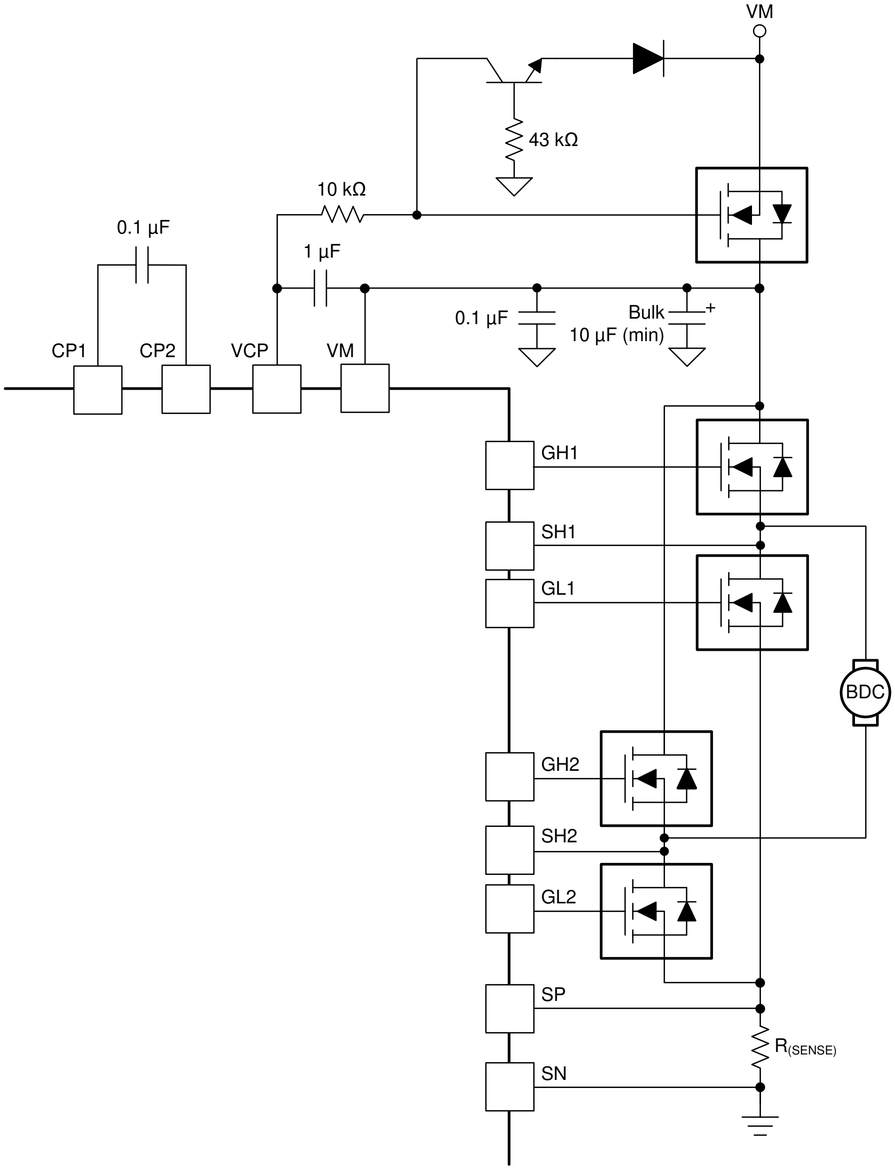


Figure 7-17. Reverse Supply Protection

7.3.15 Hardware Interface

The DRV8702-Q1 hardware interface allows the device to be configured without a SPI, however not all of the functionality is configurable like the DRV8703-Q1 device. The following configuration settings are fixed for the hardware-interface device option:

- The t_{off} value is set to 25 µs.
- Current regulation is enabled
- The VREF pin voltage is not scaled internally (100%).
- The shunt amplifier has a fixed gain of 19.8 V/V.

7.3.15.1 IDRIVE (6-level input)

The voltage or resistance on the IDRIVE pin sets the peak source and peak sink IDRIVE setting as listed in Table 7-10.

Table 7-10. DRV8702-Q1 IDRIVE Settings

IDRIVE RESISTANCE	IDRIVE VOLTAGE	SOURCE CURRENT		SINK CURRENT	
		V_{VM} = 5.5 V	V_{VM} = 13.5 V	V_{VM} = 5.5 V	V_{VM} = 13.5 V
< 1 kΩ to GND	GND	High-side: 10 mA Low-side: 10 mA	High-side: 10 mA Low-side: 10 mA	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA
33 kΩ ± 5% to GND	0.7 V ± 5%	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA	High-side: 40 mA Low-side: 40 mA	High-side: 40 mA Low-side: 40 mA
200 kΩ ± 5% to GND	2 V ± 5%	High-side: 50 mA Low-side: 40 mA	High-side: 50 mA Low-side: 45 mA	High-side: 90 mA Low-side: 85 mA	High-side: 95 mA Low-side: 95 mA
> 2 MΩ to GND, Hi-Z	3 V ± 5%	High-side: 145 mA Low-side: 115 mA	High-side: 155 mA Low-side: 130 mA	High-side: 250 mA Low-side: 235 mA	High-side: 265 mA Low-side: 260 mA
68 kΩ ± 5% to AVDD	4 V ± 5%	High-side: 190 mA Low-side: 145 mA	High-side: 210 mA Low-side: 180 mA	High-side: 330 mA Low-side: 300 mA	High-side: 350 mA Low-side: 350 mA
< 1 kΩ to AVDD	AVDD	High-side: 240 mA Low-side: 190 mA	High-side: 260 mA Low-side: 225 mA	High-side: 420 mA Low-side: 360 mA	High-side: 440 mA Low-side:430 mA

7.3.15.2 VDS (6-Level Input)

This input controls the VDS monitor trip voltage as listed in Table 7-11.

Table 7-11. DRV8702-Q1 VDS Settings

VDS RESISTANCE	VDS VOLTAGE	OVERCURRENT TRIP LEVEL ($V_{DS(OCP)}$)
< 1 kΩ to GND	GND	0.06 V
33 kΩ ± 5% to GND	0.7 V ± 5%	0.12 V
200 kΩ ± 5% to GND	2 V ± 5%	0.24 V
> 2 MΩ to GND, Hi-Z	3 V ± 5%	0.48 V
68 kΩ ± 5% to AVDD	4 V ± 5%	0.96 V
< 1 kΩ to AVDD	AVDD	Disabled

7.4 Device Functional Modes

The DRV870x-Q1 device is active unless the nSLEEP pin is brought low. In sleep mode, the charge pump is disabled, the H-bridge FETs are disabled to the Hi-Z state, and the AVDD and DVDD regulators are disabled.

Note

The $t_{(SLEEP)}$ time must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV870x-Q1 device is brought out of sleep mode automatically if the nSLEEP pin is brought high.

The $t_{(WAKE)}$ time must elapse before the outputs change state after wakeup.

On the DRV8703-Q1 device, the SPI settings are reset when coming out of UVLO or exiting sleep mode.

While the nSLEEP pin is brought low, all external H-bridge FETs are disabled. The high-side gate pins, GHx, are pulled to the output node, SHx, by an internal resistor and the low-side gate pins, GLx, are pulled to ground.

When the VM voltage is not applied and during the power-on time (t_{on}) the outputs are disabled using weak pulldown resistors between the GHx and SHx pins and the GLx and GND pins.

Note

The MODE pin controls the device-logic operation for phase and enable, independent half-bridge, or PWM input modes. This operation is latched on power up or when exiting sleep mode.

7.5 Programming

7.5.1 SPI Communication

7.5.1.1 Serial Peripheral Interface (SPI)

The SPI (DRV8703-Q1 only) is used to set device configurations, operating parameters, and read out diagnostic information. The DRV8703-Q1 SPI operates in slave mode. The SPI input data (SDI) word consists of a 16-bit word, with a 5-bit command, 3 don't care bits, and 8 bits of data. The SPI output data (SDO) word consists of 8-bit register data and the first 8 bits are don’t cares.

A valid frame has to meet following conditions:

- The clock polarity (CPOL) must be set to 0.
- The clock phase (CPHA) must be set to 0.
- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- No SCLK signal can occur when the nSCS signal is in transition.
- The SCLK pin must be low when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high impedance state.
- Full 16 SCLK cycles must occur.
- Data is captured on the falling edge of the clock and data is driven on the rising edge of the clock.
- The most-significant bit (MSB) is shifted in and out first
- For a write command, if the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 5-bit command data

7.5.1.2 SPI Format

The SDI input-data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit 15)
- 4 address bits, A (bits 14 through 11)
- 3 don't care bits, X (10 through 8)
- 8 data bits, D (7:0)

The SDO output-data word is 16 bits long and the first 8 bits are don’t care bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 7-12. SDI Input Data Word Format

R/W	ADDRESS				DON'T CARE			DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A3	A2	A1	A0	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

Table 7-13. SDO Output Data Word Format

DON'T CARE								DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

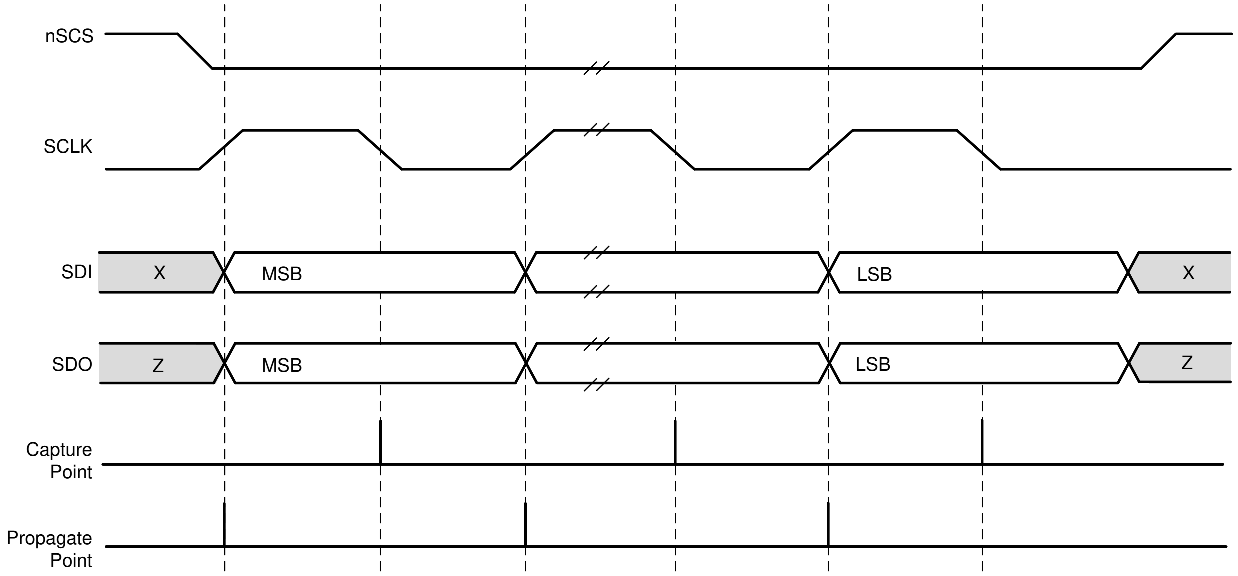


Figure 7-18. SPI Transaction

The SCLK pin should be low at power-up of the device for reliable SPI transaction. If the SCLK pin cannot be guaranteed to be low at power-up, TI recommends performing a dummy SPI-read transaction (of any register) after power-up to ensure reliable subsequent transactions. Data read from this dummy read transaction should be discarded.

7.6 Register Maps

Table 7-14. DRV8703-Q1 Memory Map

Register Name	7	6	5	4	3	2	1	0	Access Type	Address (Hex)
FAULT Status	FAULT	WDFLT	GDF	OCP	VM_UVFL	VCP_UVFL	OTSD	OTW	R	0
VDS and GDF	H2_GDF	L2_GDF	H1_GDF	L1_GDF	H2_VDS	L2_VDS	H1_VDS	L1_VDS	R	1
Main	RESERVED		LOCK			IN1/PH	IN2/EN	CLR_FLT	RW	2
IDRIVE and WD	TDEAD		WD_EN	WD_DLY		IDRIVE			RW	3
VDS	SO_LIM	VDS			DIS_H2_VDS	DIS_L2_VDS	DIS_H1_VDS	DIS_L1_VDS	RW	4
Config	TOFF		CHOP_IDS	VREF_SCL		SH_EN	GAIN_CS		RW	5

Table 7-15. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

7.6.1 Status Registers

The status registers are used to report warning and fault conditions. Status registers are read only registers.

Table 7-16 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 7-16 should be considered as reserved locations and the register contents should not be modified.

Table 7-16. Status Registers Summary Table

Address	Register Name	Section
0x00h	FAULT status	Go
0x01h	VDS and GDF status	Go

7.6.2 FAULT Status Register (address = 0x00h)

FAULT status is shown in Figure 7-19 and described in Table 7-17.

Return to Summary Table.

Read only

Figure 7-19. FAULT Status Register

7	6	5	4	3	2	1	0
FAULT	WDFLT	GDF	OCP	VM_UVFL	VCP_UVFL	OTSD	OTW
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-17. FAULT Status Field Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	Logic OR of the FAULT status register excluding the OTW bit
6	WDFLT	R	0b	Watchdog time-out fault
5	GDF	R	0b	Indicates gate drive fault condition
4	OCP	R	0b	Indicates VDS monitor overcurrent fault condition
3	VM_UVFL	R	0b	Indicates VM undervoltage lockout fault condition
2	VCP_UVFL	R	0b	Indicates charge-pump undervoltage fault condition
1	OTSD	R	0b	Indicates overtemperature shutdown
0	OTW	R	0b	Indicates overtemperature warning

7.6.3 VDS and GDF Status Register Name (address = 0x01h)

VDS and GDF status is shown in Figure 7-20 and described in Table 7-18.

Return to Summary Table.

Read only

Figure 7-20. VDS and GDF Status Register

7	6	5	4	3	2	1	0
H2_GDF	L2_GDF	H1_GDF	L1_GDF	H2_VDS	L2_VDS	H1_VDS	L1_VDS
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-18. VDS and GDF Status Field Descriptions

Bit	Field	Type	Default	Description
7	H2_GDF	R	0b	Indicates gate drive fault on the high-side FET of half-bridge 2
6	L2_GDF	R	0b	Indicates gate drive fault on the low-side FET of half-bridge 2
5	H1_GDF	R	0b	Indicates gate drive fault on the high-side FET of half-bridge 1
4	L1_GDF	R	0b	Indicates gate drive fault on the low-side FET of half-bridge 1
3	H2_VDS	R	0b	Indicates VDS monitor overcurrent fault on the high-side FET of half-bridge 2
2	L2_VDS	R	0b	Indicates VDS monitor overcurrent fault on the low-side FET of half-bridge 2
1	H1_VDS	R	0b	Indicates VDS monitor overcurrent fault on the high-side FET of half-bridge 1
0	L1_VDS	R	0b	Indicates VDS monitor overcurrent fault on the low-side FET of half-bridge 1

7.6.4 Control Registers

The control registers are used to configure the device. Control registers are read and write capable.

Table 7-19 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 7-19 should be considered as reserved locations and the register contents should not be modified.

Table 7-19. Status Registers Summary Table

Address	Register Name	Section
0x02h	Main control	Go
0x03h	IDRIVE and WD control	Go
0x04h	VDS control	Go
0x05h	Config control	Go

7.6.5 Main Control Register Name (address = 0x02h)

Main control is shown in Figure 7-21 and described in Table 7-20.

Return to Summary Table.

Read and write

Figure 7-21. Main Control Register

7	6	5	4	3	2	1	0
RESERVED		LOCK			IN1/PH	IN2/EN	CLR_FLT
R/W-00b		R/W-011b			R/W-0b	R/W-0b	R/W-0b

Table 7-20. Main Control Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	00b	Reserved
5-3	LOCK	R/W	011b	Write 110b to lock the settings by ignoring further register changes except to address 0x02h. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
2	IN1/PH	R/W	0b	This bit is ORed with the IN1/PH pin
1	IN2/EN	R/W	0b	This bit is ORed with the IN2/EN pin
0	CLR_FLT	R/W	0b	Write a 1 to this bit to clear the fault bits

7.6.6 IDRIVE and WD Control Register Name (address = 0x03h)

IDRIVE and WD control is shown in Figure 7-22 and described in Table 7-21.

Return to Summary Table.

Read and write

Figure 7-22. IDRIVE and WD Register

7	6	5	4	3	2	1	0
TDEAD		WD_EN	WD_DLY		IDRIVE		
R/W-00b		R/W-0b	R/W-00b		R/W-111b		

Table 7-21. IDRIVE and WD Field Descriptions

Bit	Field	Type	Default	Description
7-6	TDEAD	R/W	00b	Dead time 00b = 120 ns 01b = 240 ns 10b = 480 ns 11b = 960 ns
5	WD_EN	R/W	0b	Enables or disables the watchdog time (disabled by default)
4-3	WD_DLY	R/W	00b	Watchdog timeout delay (if WD_EN = 1) 00b = 10 ms 01b = 20 ms 10b = 50 ms 11b = 100 ms
2-0	IDRIVE	R/W	111b	Sets the peak source current and peak sink current of the gate drive. Table 7-22 lists the bit settings.

Table 7-22. IDRIVE Bit Settings

Bit Value	Source Current		Sink Current	
	V_{VM} = 5.5 V	V_{VM} = 13.5 V	V_{VM} = 5.5 V	V_{VM} = 13.5 V
000b	High-side: 10 mA Low-side: 10 mA	High-side: 10 mA Low-side: 10 mA	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA
001b	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA	High-side: 40 mA Low-side: 40 mA	High-side: 40 mA Low-side: 40 mA
010b	High-side: 50 mA Low-side: 40 mA	High-side: 50 mA Low-side: 45 mA	High-side: 90 mA Low-side: 85 mA	High-side: 95 mA Low-side: 95 mA
011b	High-side: 70 mA Low-side: 55 mA	High-side: 70 mA Low-side: 60 mA	High-side: 120 mA Low-side: 115 mA	High-side: 130 mA Low-side: 125 mA
100b	High-side: 100 mA Low-side: 75 mA	High-side: 105 mA Low-side: 90 mA	High-side: 170 mA Low-side: 160 mA	High-side: 185 mA Low-side: 180 mA
101b	High-side: 145 mA Low-side: 115 mA	High-side: 155 mA Low-side: 130 mA	High-side: 250 mA Low-side: 235 mA	High-side: 265 mA Low-side: 260 mA
110b	High-side: 190 mA Low-side: 145 mA	High-side: 210 mA Low-side: 180 mA	High-side: 330 mA Low-side: 300 mA	High-side: 350 mA Low-side: 350 mA
111b	High-side: 240 mA Low-side: 190 mA	High-side: 260 mA Low-side: 225 mA	High-side: 420 mA Low-side: 360 mA	High-side: 440 mA Low-side: 430 mA

7.6.7 VDS Control Register Name (address = 0x04h)

VDS control is shown in Figure 7-23 and described in Table 7-23.

Return to Summary Table.

Read and write

Figure 7-23. VDS Control Register

7	6	5	4	3	2	1	0
SO_LIM	VDS			DIS_H2_VDS	DIS_L2_VDS	DIS_H1_VDS	DIS_L1_VDS
R/W-0b	R/W-111b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-23. VDS Control Field Descriptions

Bit	Field	Type	Default	Description
7	SO_LIM	R/W	0b	0b = Default operation 1b = SO output is voltage-limited to 3.6 V
6-4	VDS	R/W	111b	Sets the $V_{DS(OCP)}$ monitor for each FET 000b = 0.06 V 001b = 0.145 V 010b = 0.17 V 011b = 0.2 V 100b = 0.12 V 101b = 0.24 V 110b = 0.48 V 111b = 0.96 V
3	DIS_H2_VDS	R/W	0b	Disables the VDS monitor on the high-side FET of half-bridge 2 (enabled by default)
2	DIS_L2_VDS	R/W	0b	Disables the VDS monitor on the low-side FET of half-bridge 2 (enabled by default)
1	DIS_H1_VDS	R/W	0b	Disables the VDS monitor on the high-side FET of half-bridge 1 (enabled by default)
0	DIS_L1_VDS	R/W	0b	Disables the VDS monitor on the low-side FET of half-bridge 1 (enabled by default)

7.6.8 Config Control Register Name (address = 0x05h)

Config control is shown in Figure 7-24 and described in Table 7-24.

Return to Summary Table.

Read and write

Figure 7-24. Config Control Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="2">TOFF</td><td>CHOP_IDS</td><td colspan="2">VREF_SCL</td><td>SH_EN</td><td colspan="2">GAIN_CS</td></tr>
<tr><td colspan="2">R/W-00b</td><td>R/W-0b</td><td colspan="2">R/W-00b</td><td>R/W-0b</td><td colspan="2">R/W-01b</td></tr>
</table>

Table 7-24. Config Control Field Descriptions

Bit	Field	Type	Default	Description
7-6	TOFF	R/W	00b	Off time for PWM current chopping 00b = 25 µs 01b = 50 µs 10b = 100 µs 11b = 200 µs
5	CHOP_IDS	R/W	0b	Disables current regulation (enabled by default)
4-3	VREF_SCL	R/W	00b	Scale factor for the VREF input 00b = 100% 01b = 75% 10b = 50% 11b = 25%
2	SH_EN	R/W	0b	Enables sample and hold operation of the shunt amplifier (disabled by default)
1-0	GAIN_CS	R/W	01b	Shunt amplifier gain setting 00b = 10 V/V 01b = 19.8 V/V 10b = 39.4 V/V 11b = 78 V/V

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV870x-Q1 device is used in brushed-DC, solenoid, or relay-control applications. The following typical application can be used to configure the DRV870x-Q1 device.

8.2 Typical Application

This application features the DRV8702-Q1 device.

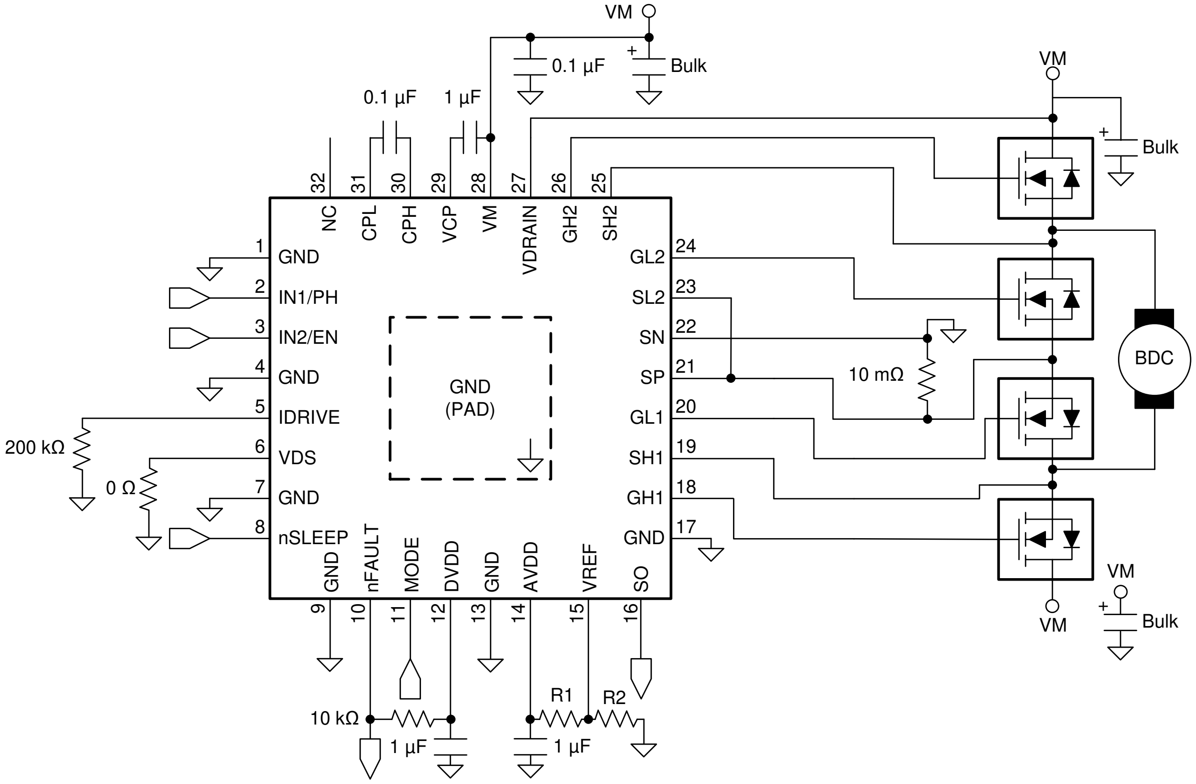


Figure 8-1. DRV8702-Q1 Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	VM	14 V
Supply voltage range		7 V to 35 V
FET part number		CSD18502Q5B
FET total gate charge	Q_g	52 nC (typical)
FET gate-to-drain charge	Q_{gd}	8.4 nC (typical)
Target FET gate rise time	t_r	100 to 300 ns
Motor current chopping level	$I_{(CHOP)}$	15 A

8.2.2 Detailed Design Procedure

8.2.2.1 External FET Selection

The DRV8702-Q1 FET support is based on the charge-pump capacity and PWM-output frequency. For a quick calculation of FET driving capacity, use Equation 3 when drive and brake (slow decay) are the primary modes of operation.

$$Q_g < \frac{I_{VCP}}{f_{(PWM)}} \tag{3}$$

where

- f_{PWM} is the maximum desired PWM frequency to be applied to the DRV8702-Q1 inputs or the current chopping frequency, whichever is larger.
- I_{VCP} is the charge-pump capacity, which depends on the VM voltage.

The internal current chopping frequency is at most equal to the PWM frequency as shown in Equation 4.

$$f_{(PWM)} < \frac{1}{t_{off} + t_{(BLANK)}} \tag{4}$$

For example, if the VM voltage of a system is 7 V (I_{VCP} = 8 mA) and uses a maximum PWM frequency of 40 kHz, then the DRV8702-Q1 device will support FETs with a Q_g up to 200 nC.

If the application requires a forced fast decay (or alternating between drive and reverse drive), use Equation 5 to calculate the maximum FET driving capacity.

$$Q_g < \frac{I_{VCP}}{2 \times f_{(PWM)}} \tag{5}$$

8.2.2.2 IDRIVE Configuration

The IDRIVE current is selected based on the gate charge of the FETs. The IDRIVE pin must be configured so that the FET gates are charged entirely during the $t_{(DRIVE)}$ time. If the selected IDRIVE current is too low for a given FET, then the FET may not turn on completely. TI recommends adjusting these values in-system with the required external FETs and motor to determine the best possible setting for any application.

For FETs with a known gate-to-drain charge (Q_{gd}) and desired rise time (t_r), the IDRIVE current can be selected based on the Equation 6.

$$I_{DRIVE} > \frac{Q_{gd}}{t_r} \tag{6}$$

If the gate-to-drain charge is 2.3 nC and the desired rise time is around 100 to 300 ns, use Equation 7 to calculate the minimum IDRIVE (I_{DRIVE1}) and Equation 8 to calculate the maximum IDRIVE (I_{DRIVE2}).

$$I_{DRIVE1} = 8.4\ \text{nC} / 100\ \text{ns} = 84\ \text{mA} \tag{7}$$

$$I_{DRIVE2} = 8.4\ \text{nC} / 300\ \text{ns} = 28\ \text{mA} \tag{8}$$

Select a value for IDRIVE between 28 and 84 mA. An IDRIVE value of approximately 50 mA for the source (approximately 100 mA sink) was selected for this application. This value requires a 200-kΩ resistor from the IDRIVE pin to ground.

8.2.2.3 VDS Configuration

The VDS monitor threshold voltage, $V_{DS(OCP)}$, is configured based on the maximum current, I_{VDS}, and $R_{DS(on)}$ of the FETs. The drain to source voltage, V_{DSFET}, is the maximum current, I_{VDS}, multiplied by the $R_{DS(on)}$ of the FET.

The VDS pin of the DRV8702-Q1 selects the VDS monitor trip threshold, $V_{DS(OCP)}$. The VDS bits in the VDS register of the DRV8703-Q1 selects the $V_{DS(OCP)}$ voltage. Use Equation 9 to calculate the trip current.

$$I_{VDS} > \frac{V_{DSFET}}{R_{DS(on)}} \tag{9}$$

If the $R_{DS(on)}$ of the FET is 1.8 mΩ and the desired maximum current is less than 100 A, the V_{DSFET} voltage is equal to 180 mV as shown in Equation 10.

For this example, select a value for the $V_{DS(OCP)}$ that is less than 180 mV. A $V_{DS(OCP)}$ value of 0.12 V was selected for this application.

To set the $V_{DS(OCP)}$ to 0.12 V, use the SPI (DRV8703-Q1 Only) or place a 33k resistor at the VDS pin to ground (DRV8702-Q1 Only).

The VDS pin can configured to select other $V_{DS(OCP)}$ threshold voltages. See the Section 7.3.11 section for more information on VDS operation.

$$V_{DSFET} = I_{VDS} \times R_{DS(on)} = 100\ \text{A} \times 1.8\ \text{m}\Omega = 180\ \text{mV} \tag{10}$$

8.2.2.4 Current Chopping Configuration

The chopping current is set based on the sense resistor value and the analog voltage at the VREF pin. Use Equation 11 to calculate the current ($I_{(CHOP)}$). The amplifier gain, A_V, is 19.8 V/V for the DRV8702-Q1 and V_{IO} is typically 5 mV (input referred).

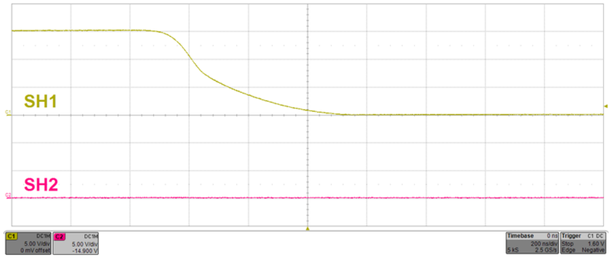
$$I_{(CHOP)} \quad \frac{V_{VREF} - V_{IO} \times A_V}{A_V \times R_{(SENSE)}} \tag{11}$$

For example, if the desired chopping current is 15 A, select a value of 10 mΩ for $R_{(SENSE)}$. The value of V_{VREF} must therefore be 2.975 V. Add a resistor divider from the AVDD (5 V) pin to set the V_{VREF} at approximately 2.975 V. Select a value of 13 kΩ for R2 and 19.1 kΩ for R1 (the VREF resistor).

If current chopping is not required, the sense resistor can be removed and the source of the low side FET can be connected to ground.

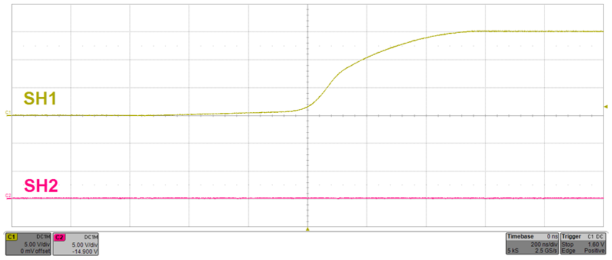
SN and SP should be connected to the source of the low side FET and VREF should be connected to AVDD

8.2.3 Application Curves



10-mA source 20-mA sink

Figure 8-2. SH1 Fall Time



10-mA source 20-mA sink

Figure 8-3. SH1 Rise Time

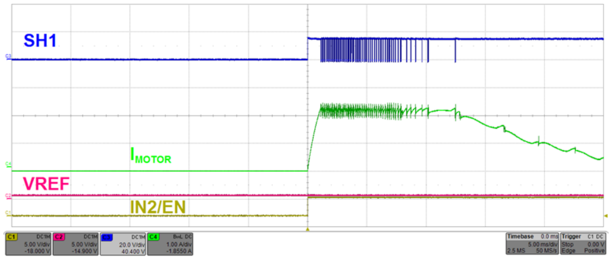


Figure 8-4. Current Profile on Motor Startup With Regulation

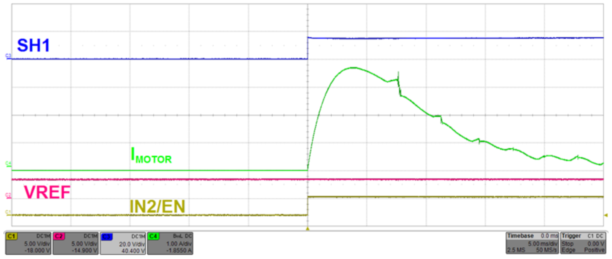


Figure 8-5. Current Profile on Motor Startup Without Regulation

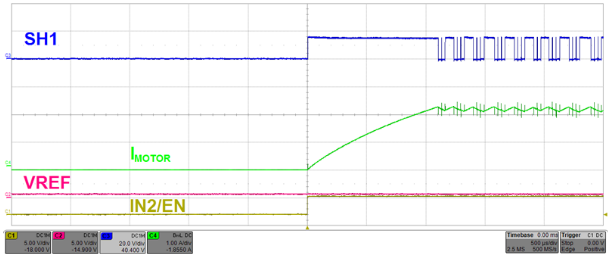


Figure 8-6. Current Regulating at 2.25 A on Motor Startup

9 Power Supply Recommendations

The DRV8702-Q1 device is designed to operate with an input voltage supply (VM) rangefrom 5.5 V to 45 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the DRV8702-Q1 device as possible. Also, a bulk capacitor valued at least 10 µF must be placed on the VM pin.

Additional bulk capacitance is required to bypass the external H-bridge FETs.

9.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It is beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors including:

- The highest current required by the motor system.
- The capacitance of the power supply and the ability of the power supply to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (brushed DC, brushless DC, and stepper).
- The motor braking method.

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When sufficient bulk capacitance is used, the motor voltage remains stable, and high current can be quickly supplied.

The data sheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

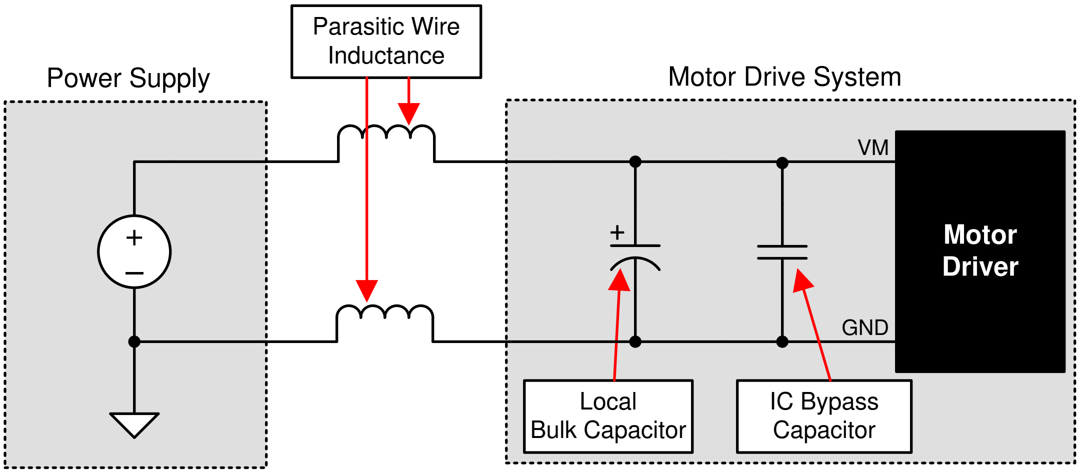


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage to provide a margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to ground using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground-plane connection to the GND pin of the device. The VM pin must also be bypassed to ground using a bulk capacitor rated for VM. This capacitor can be electrolytic and must be at least 10 µF.

A low-ESR ceramic capacitor must be placed between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this capacitor as close to the pins as possible. A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the AVDD and DVDD pins to ground with ceramic capacitors rated for 6.3 V. Place these bypassing capacitors as close to the pins as possible.

Use separate traces to connect the SP and SN pins to the $R_{(SENSE)}$ resistor.

10.2 Layout Example

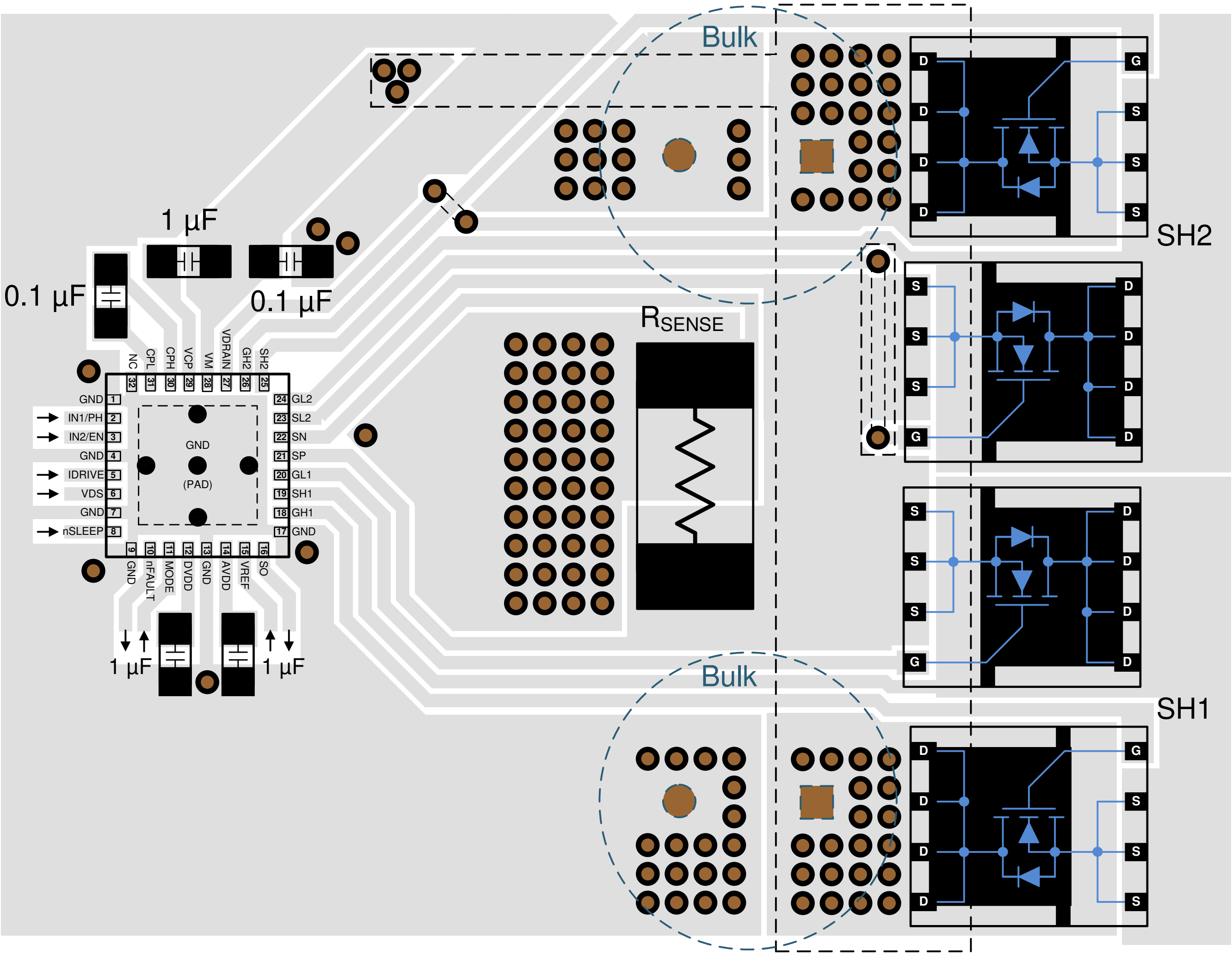


Figure 10-1. DRV8702-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Automotive Relay Replacement Application Note*
- Texas Instruments, *DRV8702-Q1 EVM User's Guide*
- Texas Instruments, *DRV8703-Q1 EVM User's Guide*
- Texas Instruments, *Small Footprint Motor Driver Sunroof Module Design Guide*
- Texas Instruments, *Relay Replacement for Brushed DC Motor Drive in Automotive Applications* application report
- Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Smart Gate Drivers*

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8702-Q1	Click here	Click here	Click here	Click here	Click here
DRV8703-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

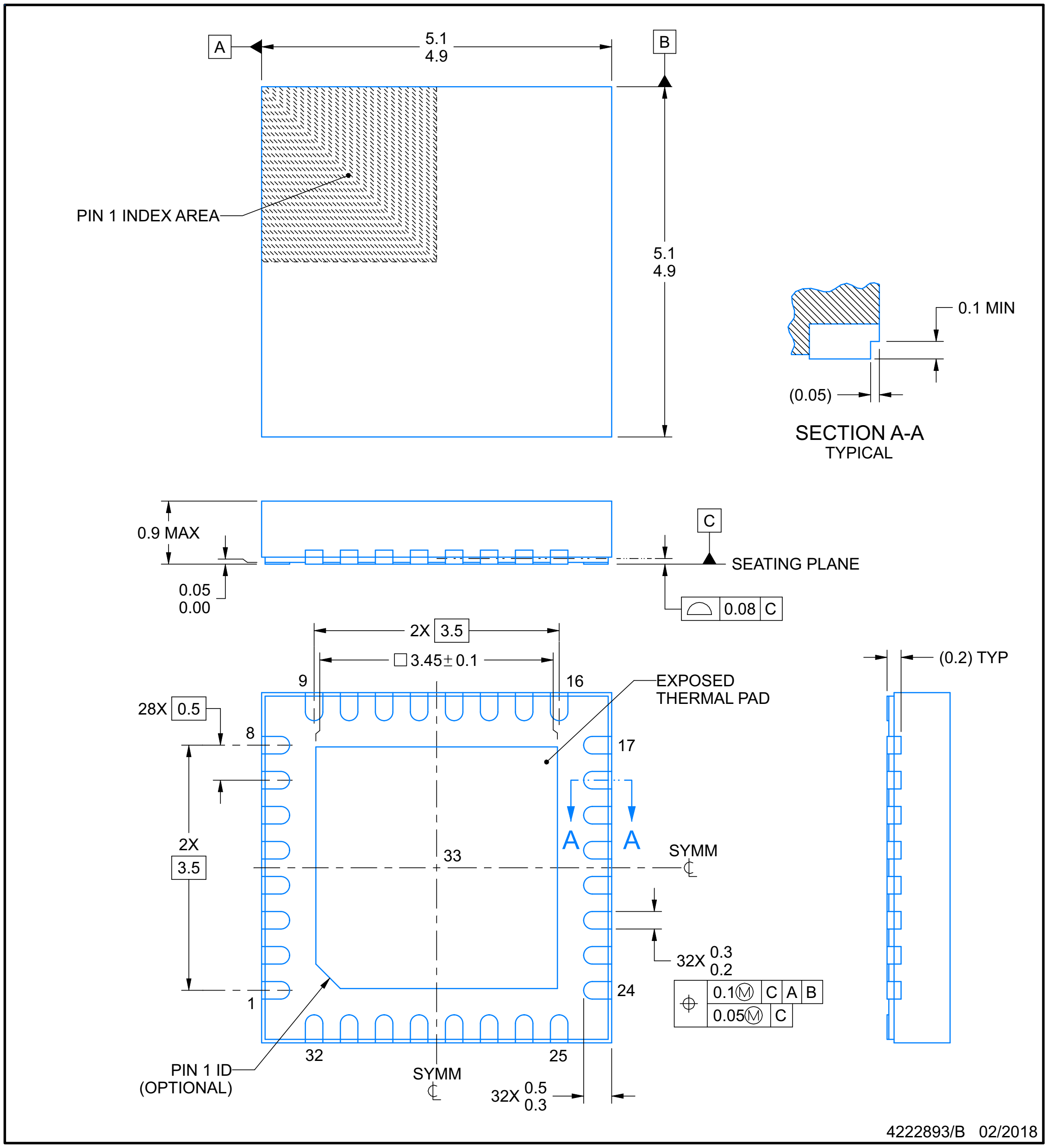
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RHB0032N

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

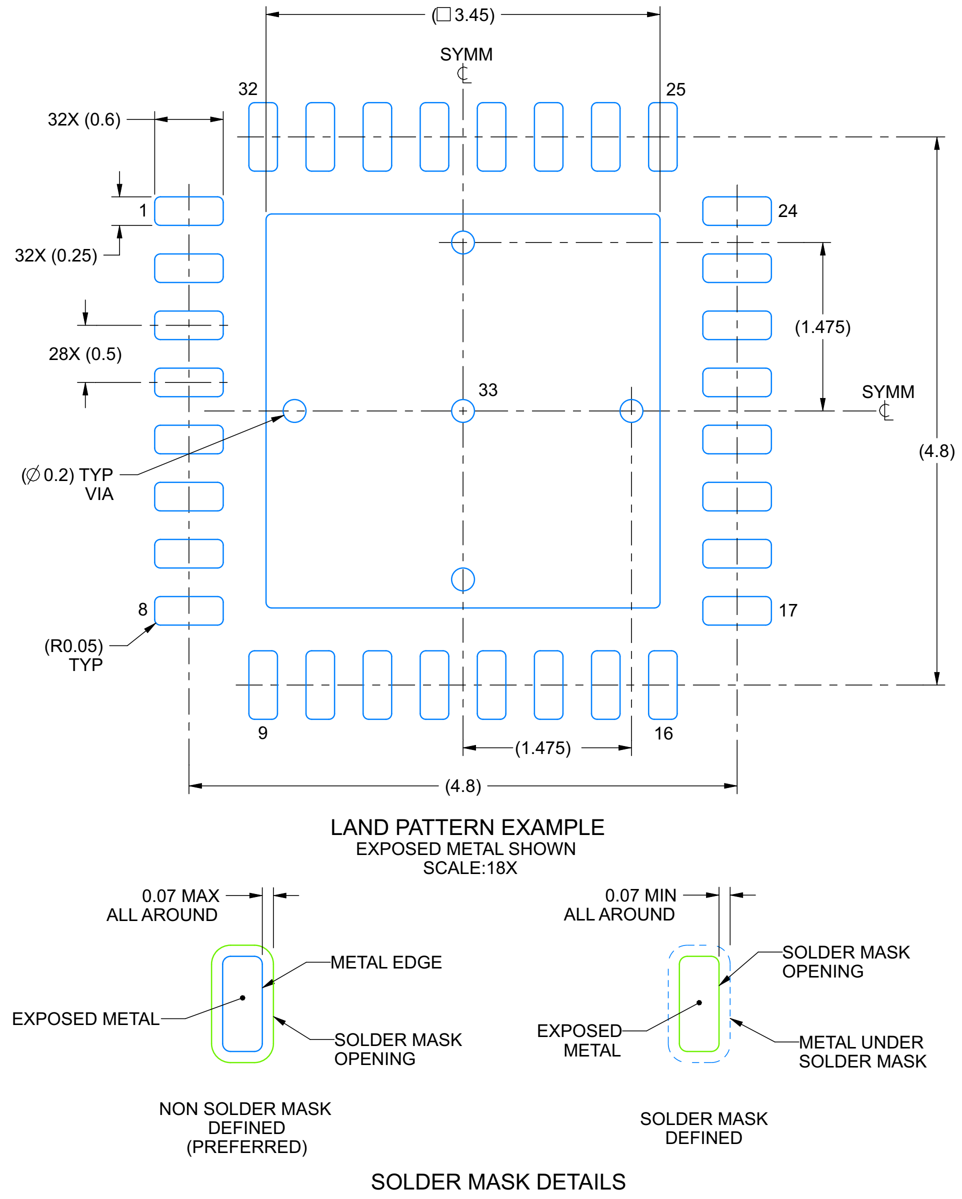
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032N

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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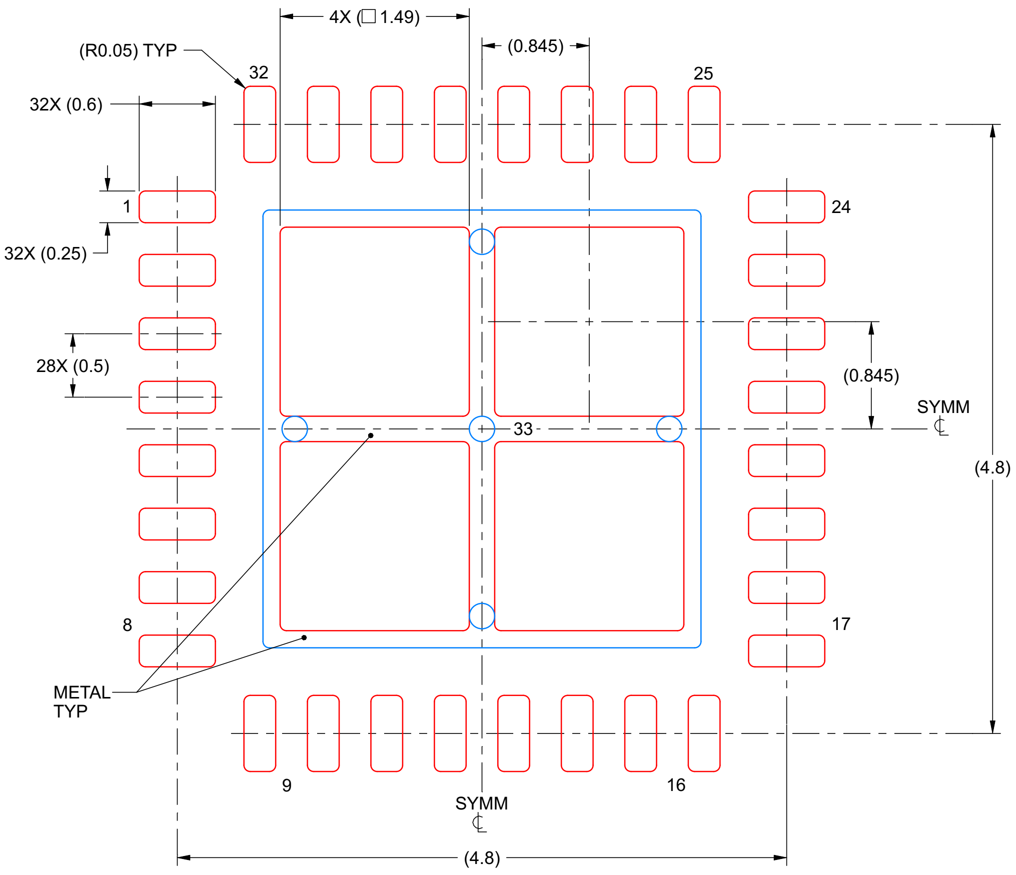
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032N **VQFN - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8702QRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	DRV8702
DRV8702QRHBTQ1	Obsolete	Production	VQFN (RHB) | 32	-	-	Call TI	Call TI	-40 to 125	DRV8702
DRV8703QRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	DRV8703
DRV8703QRHBTQ1	Obsolete	Production	VQFN (RHB) | 32	-	-	Call TI	Call TI	-40 to 125	DRV8703

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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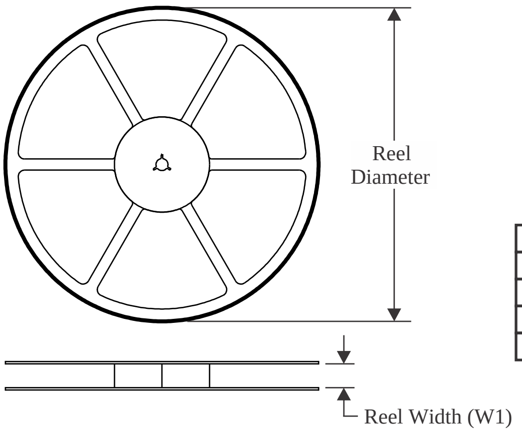
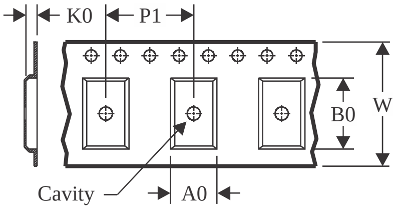
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

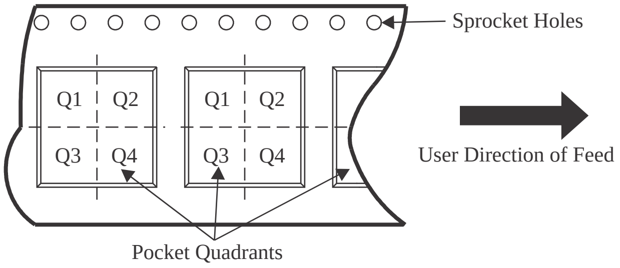


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

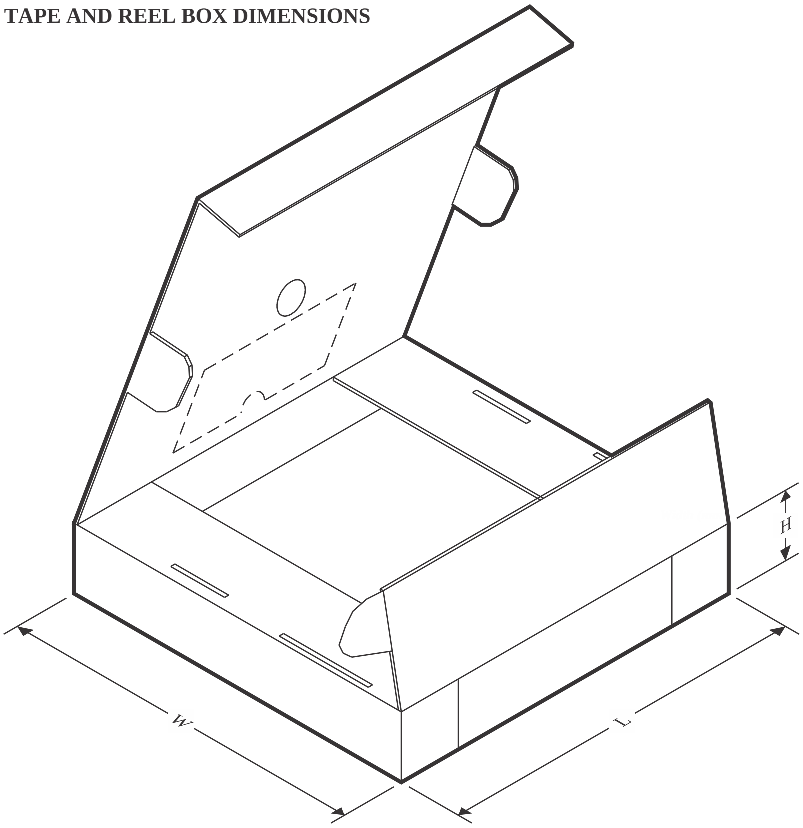
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8702QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8703QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8702QRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
DRV8703QRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0