TMS8609F 2x15W Analog Class-D AUDIO PA with EMI Suppression & Power-Limiting

Features

- 15W/CH BTL Mode into an 8Ω Load @10% THD+N with 15V Supply
- Supply Voltage Ranges from 8.0V to 15.5V
- Filter-Free Operation
- Programmable Soft-Clipping Power Limit
- 4 Gain Selections: 20dB/26dB/32dB/36dB;
- Internal feedback control with high PSRR
- 90% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Thermal and Short-Circuit Protection as well as Over-Current -Protection with Auto Recovery
- Comprehensive Click and Pop Suppression
- EMI/EMC Suppression with SSM
- Output Parallel as Mono as to Drive Low Impedance Speaker
- Space-Saving Surface Mount 28-Pin HTSSOP Package with Thermal Pad

Application

- Flat Panel Display TVs
- Powered Speakers
- Music Instruments
- Consumer Audio Application

Description

The TMS8609F is a class-D audio power amplifier with analog input and high-power efficiency for driving two bridged-tied stereo speakers with up to 15W/8Ω (per channel). Higher than 90% efficiency making the TMS8609F eliminate the need for an external heat sink when playing music.

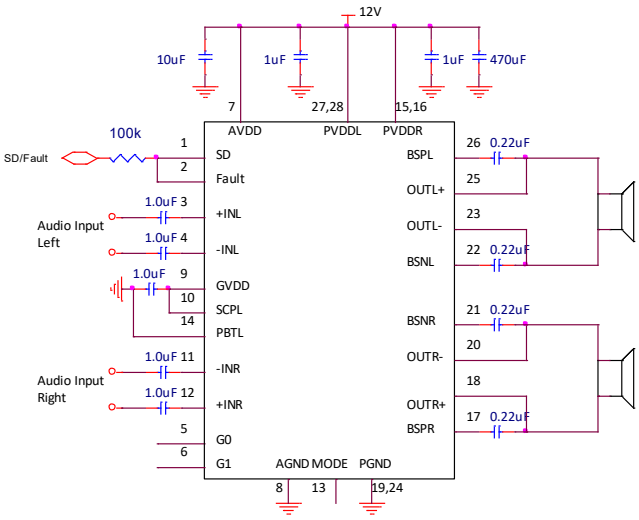
The TMS8609F integrated spread spectrum modulation (SSM) to avoid EMI/EMC interference which will eliminate to use huge and expensive LPF (Low Pass Filter) to save the PCB area and BOM cost.

The programmable soft clipping power limit (SCPL) limits the maximum output voltage to allows adjustment of the maximum output power without signal clipping for enhanced speaker protection and audio quality.

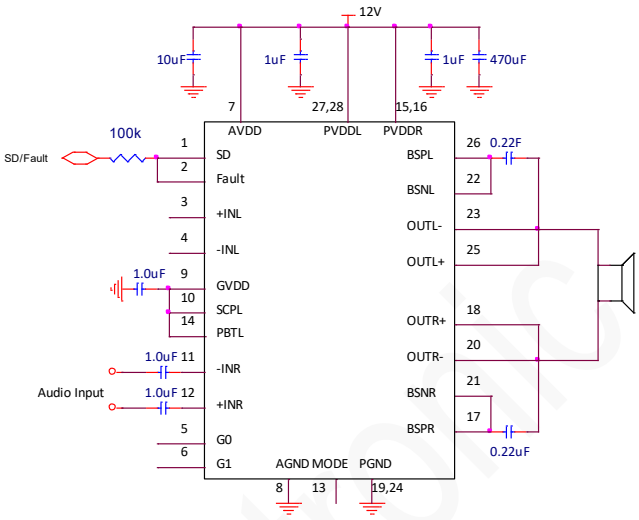
The TMS8609F features over current protection, short circuit protection and over temperature protection to fully protect the chip to be damaged.

The TMS8609F is available in HTSSOP28 package with exposed thermal pad.

Typical Application

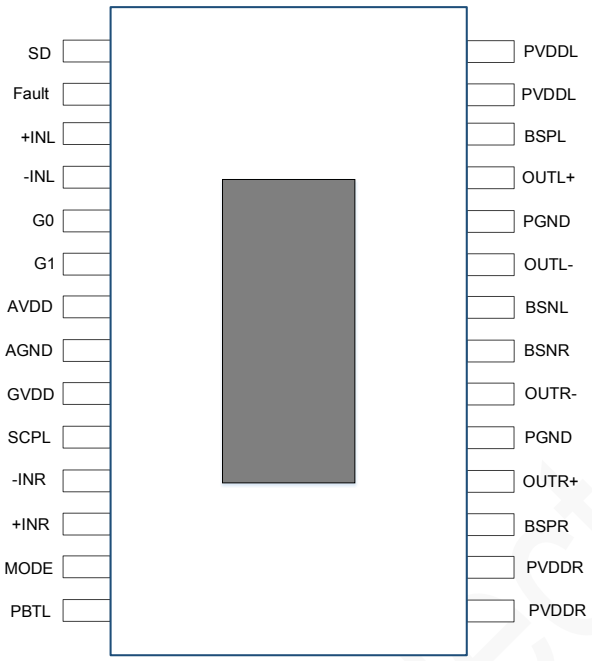


BTL Application Circuit



PBTL Application Circuit

Package



HTSSOP28 (Top View)

Order Information

Part Number	Package	Top Marking	Quantity/ Reel
TMS8609FTF-TR	HTSSOP28	T8609FTF XXXXX	4500

TMS8609F devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	I/O	Description
1	SD	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVDD.
2	Fault	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVDD. Short circuit faults can be set to auto-recovery by connecting FAULT pin to SD pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVDD.
3	+INL	I	Positive audio input for left channel. Biased at 3V.
4	-INL	I	Negative audio input for left channel. Biased at 3V.
5	G0	I	Gain selects least significant bit 0. TTL logic levels with compliance to AVDD.
6	G1	I	Gain selects least significant bit 1. TTL logic levels with compliance to AVDD.
7	AVDD	P	Analog supply
8	AGND	P	Analog signal ground. Connect to the thermal pad.
9	GVDD	O	High-side FET gate drive supply. Nominal voltage is 5V. Should be used as supply for SCPL function.
10	SCPL	I	Soft Clipping Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit
11	+INR	I	Negative audio input for right channel. Biased at 3V.
12	-INR	I	Positive audio input for right channel. Biased at 3V.
13	MODE	I	SSM Control Pin, connect directly to GVDD turn off SSM
14	PBTL	I	Parallel BTL mode switch
15	PVDDR	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally.
16	PVDDR	P	
17	BSPR	P	Bootstrap I/O for right channel, positive high-side FET.
18	OUTR+	O	Class-D H-bridge positive output for right channel.
19	PGND	P	Power ground for the H-bridges.
20	OUTR-	O	Class-D H-bridge negative output for right channel.
21	BSNR	P	Bootstrap I/O for right channel, negative high-side FET.
22	BSNL	P	Bootstrap I/O for left channel, negative high-side FET.
23	OUTL-	O	Class-D H-bridge negative output for left channel.
24	PGND	P	Power ground for the H-bridges.
25	OUTL+	O	Class-D H-bridge positive output for left channel.
26	BSPL	P	Bootstrap I/O for left channel, positive high-side FET.
27	PVDDL	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.
28	PVDDL	P	

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
PVDD_x, AVDD	Power Supply Voltage	-0.5 to + 18.5	V
GVDD	Supply Voltage	-0.5 to + 6.5	V
VI	Digital Input	–0.5 to GVDD + 0.5	V
T_J	Junction Temperature	–55 to +150	°C
T_{STG}	Storage Temperature	–65 to +165	°C

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
PVDD_x, AVDD	Power Supply Voltage	+8.5 to +15.5	V
$VIH_{\_MIN}$	Input High	2	V
$VIL_{\_MAX}$	Input Low	0.8	V
T_A	Operating free-air temperature	–40 to +85	°C
T_J	Junction Temperature	–40 to +125	°C
RL	Loading Impedance	4	Ω

ESD Rating

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model	±4000	V
V_{ESD_CDM}	Charge Device Model	±1000	V

THERMAL INFOAMATION

Symbol	Parameter	Value	Unit
θ_{JA}	Junction to ambient resistance	37	°C/W
θ_{JC}	Junction to case resistance	19	°C/W

DC Electrical Characteristics

T_A=25°C, PV_{DD}=12V, Gain=20dB, R_L=L(33μH) + R+L(33μH), unless otherwise noted.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_Q	Quiescent Current	PV_{DD}=12V	No Load		8.5	20	mA
		PV_{DD}=8.5V	No Load		8.0	15	mA
I_{SD}	Shutdown Current	PV_{DD}=8.5V to 15.5V	SD=0V		6	20	μA
R_{SDON}	Static Drain-to Source On-state Resistor	High Side MOS, I=500mA	PVDD=12V		230		mΩ
		Low Side MOS, I=500mA	PVDD=12V		230		mΩ
V_{OS}	Output Offset Voltage	Input ac-ground, PVDD=12V			1.5	30	mV
t_{ON}	Turn On Time	SD from 0V to 2V			24		ms
t_{OFF}	Turn Off Time	SD from 2V to 0V			2		μs
f_{OSC}	Switching Frequency	PV_{DD}=8.5V to 15.5V			300		kHz

AC Electrical Characteristics

T_A=25°C, PV_{DD}=12V, Gain=20dB, R_L=L(33μH) + R+L(33μH), unless otherwise noted.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Po	Output Power	f=1kHz, R=8Ω, PV_{DD}=12V	THD+N=10%		9.5		W
			THD+N=1%		7.8		
		f=1kHz, R=6Ω, PV_{DD}=12V	THD+N=10%		12.5		W
			THD+N=1%		10		
		f=1kHz, R=8Ω, PV_{DD}=15V	THD+N=10%		15		W
			THD+N=1%		12		
THD+N	Total Hormonic Distortion Plus Noise	PV_{DD}=12V, RL=8Ω, f=1kHz	Po=0.5W		0.010		%
			Po=2.5W		0.011		
			Po=5.0W		0.016		
PSRR	Power Supply Ripple Rejection	Inputs ac-grounded with C=1μF	f=1kHz		-65		dB
SNR	Signal to Noise Ratio	THD=1%, R=8Ω	f=1kHz		100		dB
CS	Cross Talk	V_O=1Vrms	f=1kHz		-96		dB
Vn	Output Noise	Inputs ac-grounded	A weighting		80		μV
Gv	Closed-loop Gain	G0=0; G1=0			20		dB
		G0=1; G1=0			26		
		G0=0; G1=1			32		
		G0=1; G1=1			36		
UVLO	Under Voltage Lock-out	PV_{DD} Rising			8.5		V
		PV_{DD} Falling			8.0		
OTP	Over Temperature Protection	OTP Threshold			165		°C
HYS		Hysterisis			20		°C

Performance Characteristics

T_A=25°C, PV_{DD}=12V, Gain=26dB, R_L=L(33μH) + R+L(33μH), SSM off, unless otherwise noted.

Fig 1-THD+N Vs. Output Power(R_L=8Ω)

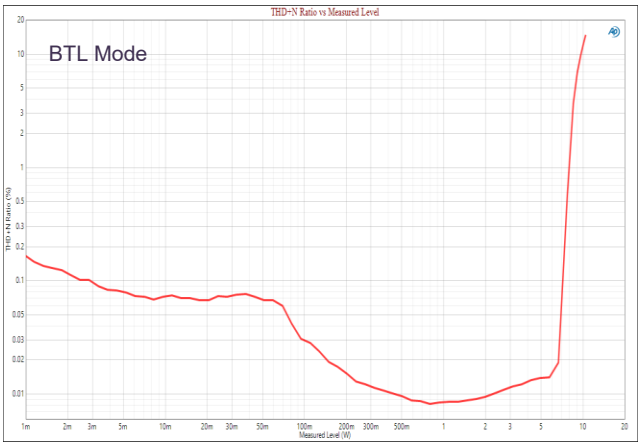


Fig 2-THD+N Vs. Frequency(R_L=8Ω)

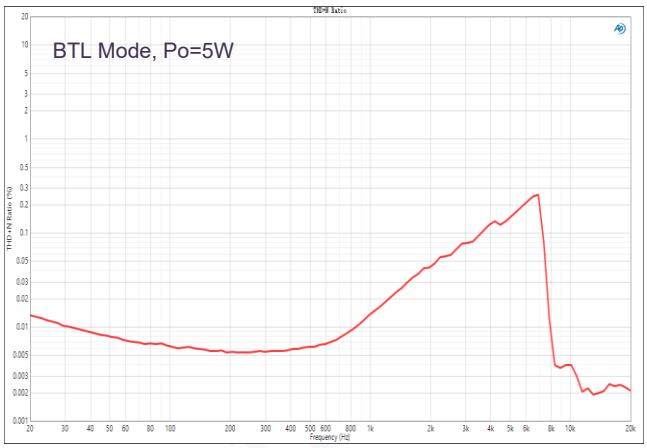


Fig 3-THD+N Vs. Output Power (R_L=6Ω)

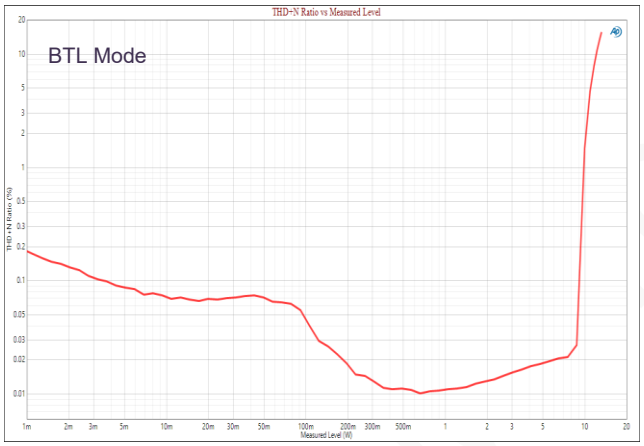


Fig 3-THD+N Vs. Frequency (R_L=6Ω)

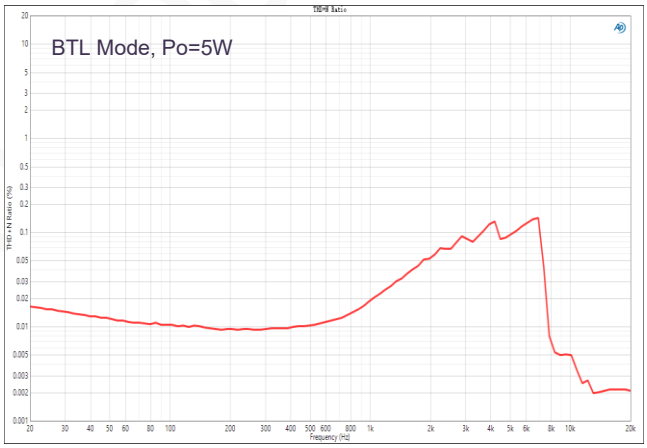


Fig 5-THD+N Vs. Output Power (R_L=4Ω)(1)

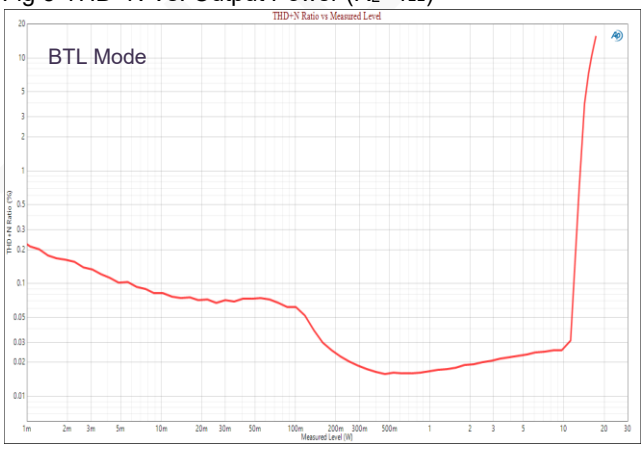
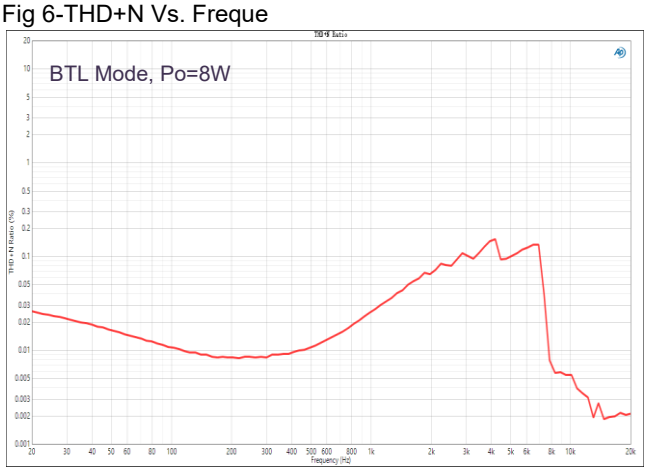


Fig 6-THD+N Vs. Freque



Performance Characteristics

T_A=25°C, PV_{DD}=12V, Gain=26dB, R_L=L(33μH) + R+L(33μH), SSM off, unless otherwise noted.

Fig 7-THD+N Vs. Output Power(R_L=8Ω)

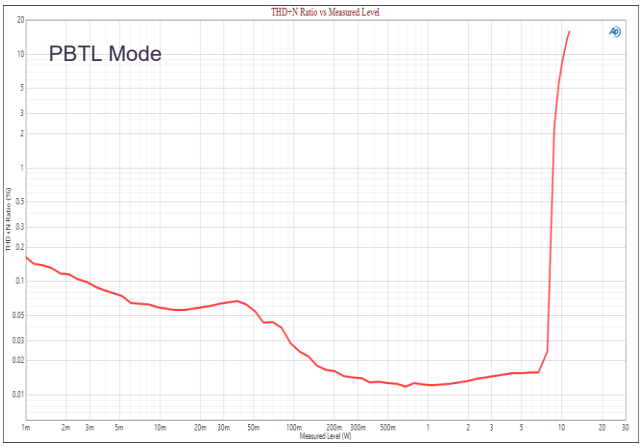


Fig 8-THD+N Vs. Frequency(R_L=8Ω)

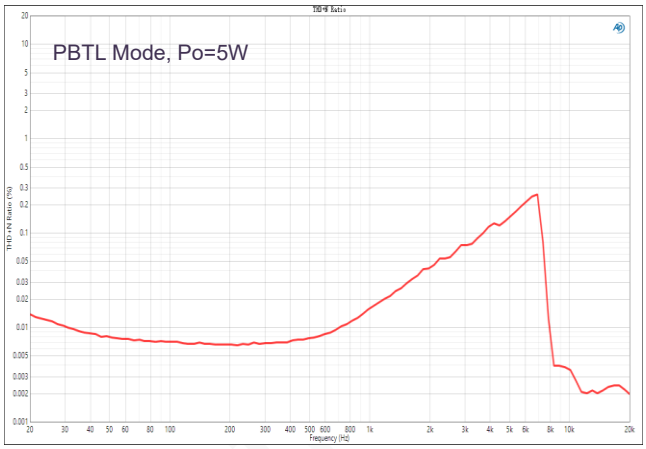


Fig 9-THD+N Vs. Output Power (R_L=6Ω)

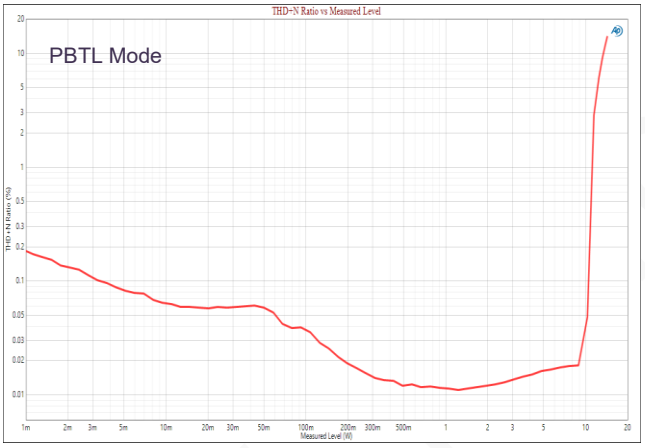


Fig 10-THD+N Vs. Frequency (R_L=6Ω)

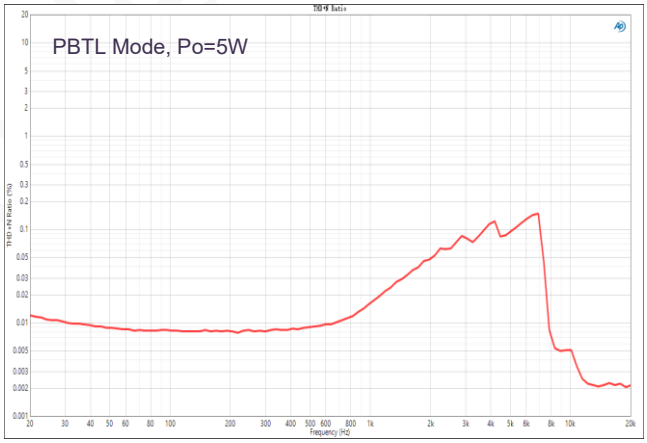


Fig 11-THD+N Vs. Output Power (R_L=4Ω) (1)

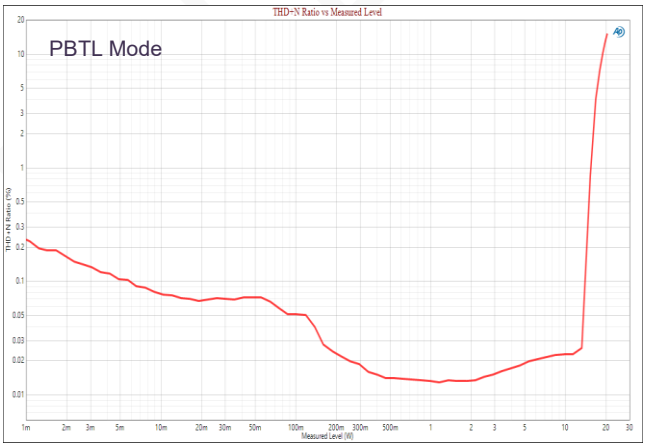
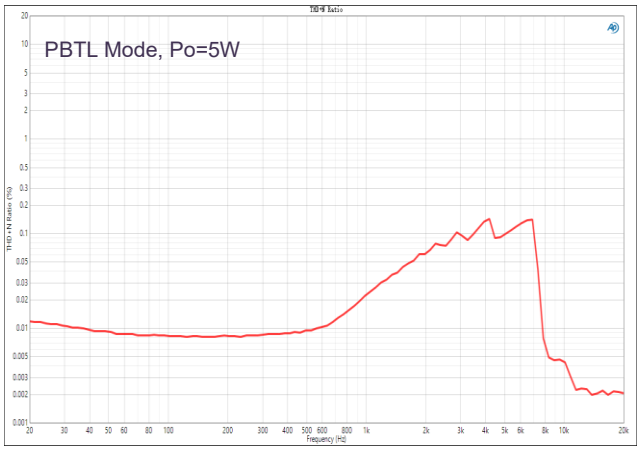


Fig 12-THD+N Vs. Frequency (R_L=4Ω)



Note: (1) The maximum output power is limited at THD+N < 1% with 4Ω load;

Performance Characteristics

T_A=25°C, PV_{DD}=12V, Gain=26dB, R_L=L(33μH) + R+L(33μH), SSM off, unless otherwise noted.

Fig 13-Frequency Response

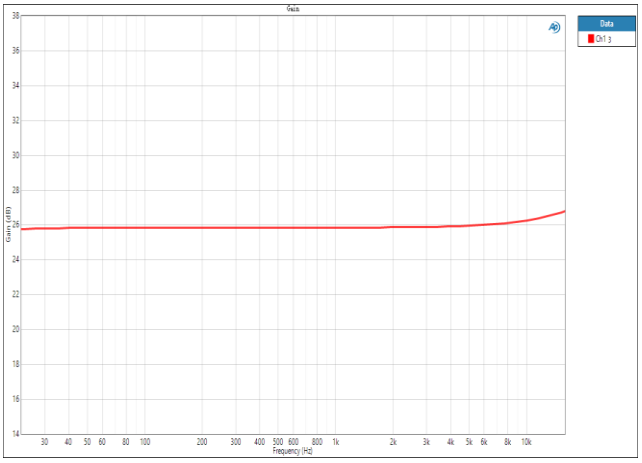


Fig 14-Noise Floor (R_L=8Ω)

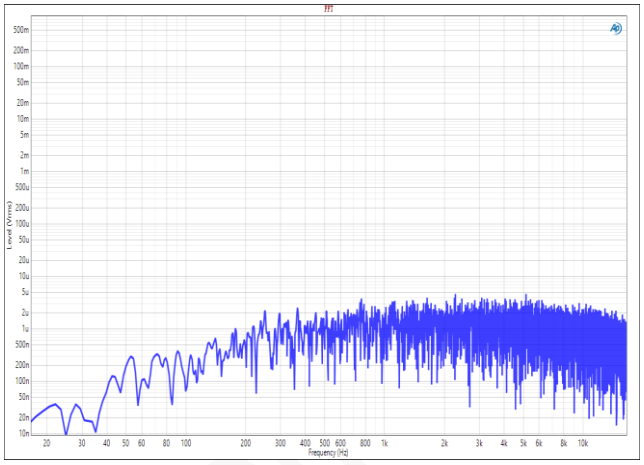


Fig 15-PSRR (Vripp=200mVpp)

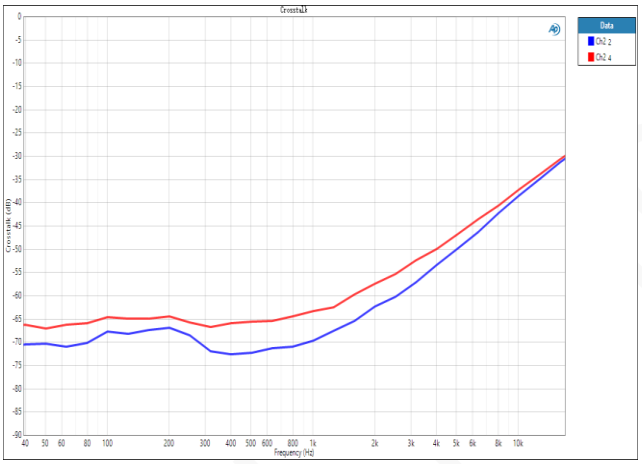


Fig 16-Crosstalk(Vo=1Vrms)

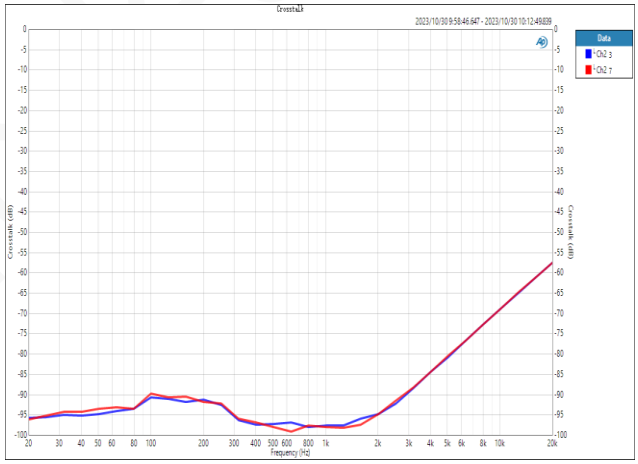


Fig 17-Efficiency

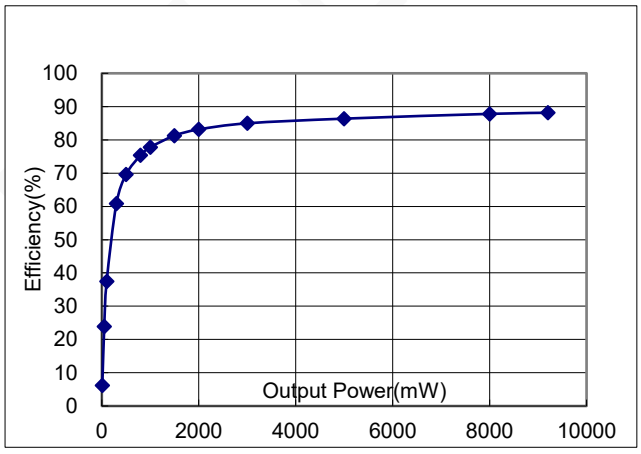
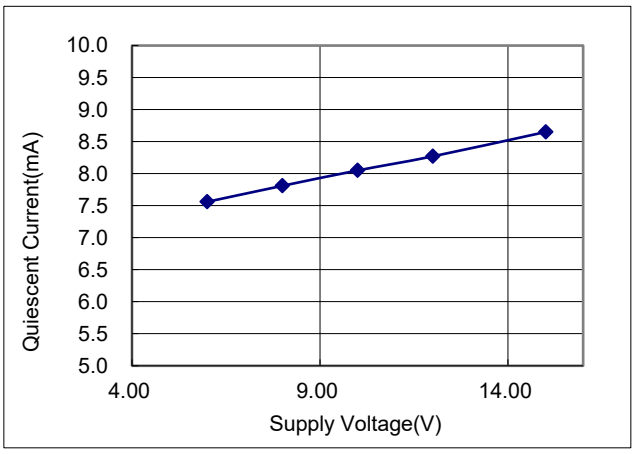


Fig 18-Quiescent Current



Application Information

Gain Setting

The gain of the TMS8609F is set to one of four options by the state of the G0 and G1 pins. Changing the gain setting also changes the input impedance of the TMS8609F. Refer to below table for a list of the gain settings.

G1	G0	Gain	Input Impedance
		(dB)	（kΩ）
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

Input Capacitors (Ci)

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form is a high-pass filter with the corner frequency determined in the follow equation:

$$f_C = \frac{1}{(2\pi RiCi)}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example, when Ri is 20kΩ and the specification calls for a flat bass response are down to 100Hz. Equation is reconfigured as followed:

$$Ci = \frac{1}{(2\pi Rif_c)}$$

When input resistance variation is considered, the Ci is 84nF, so one would likely choose a value of 100nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at 3.0V, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

PBTL Select

Use the PBTL pin to select between PBTL mode when held high or BTL mode when held low. Connect the speaker between the right and left outputs, with the positive and negative output from each channel tied together.

Application Information

Decoupling Capacitor (CS)

The TMS8609F is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low Equivalent-Series-Resistance (ESR) ceramic capacitor, typically 1μF, is placed as close as possible to the device PVDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure 19-1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies. A snubber circuit at output nodes as shown at Figure 19-2 will diminish the spiking caused by the Class D switching that make the radiation reduction more. The snubber circuit should be place as closed as to TMS8609F.

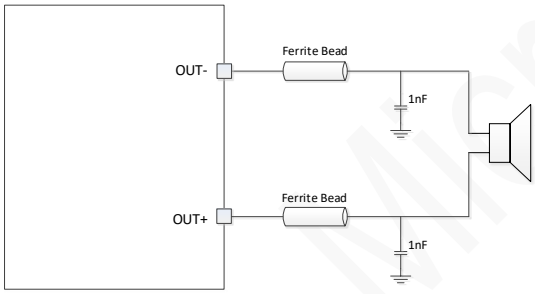


Fig 19-1: Ferrite Bead Filter to Reduce EMI

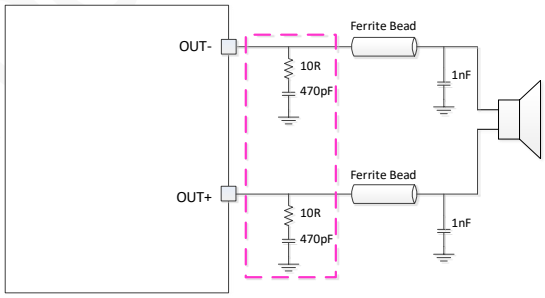


Fig 19-2: Snubber Circuit for EMI Suppression

Under Voltage Lock-out (UVLO)

The TMS8609F incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 8.0V or below, the TMS8609F goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when PVDD higher than 8.5V.

Over Current Protection (OCP)

The TMS8609F has protection from overcurrent conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the Fault pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SD pin through the low state. If automatic recovery from the short circuit protection latch is desired, connect the Fault pin directly to the SD pin. This allows the Fault pin function to automatically drive the SD pin low which clears the short-circuit protection latch.

Application Information

Soft-Clipping Power Limiting (SCPL)

The TMS8609F has a built-in Soft-Clipping Power Limiting to limit excessive output voltage to a preset output signal. When an excessive level input signal is sent to TMS8609F, the SCPL will active immediately to preserve high audio quality and to protect the attached speaker from excessive power without any delay.

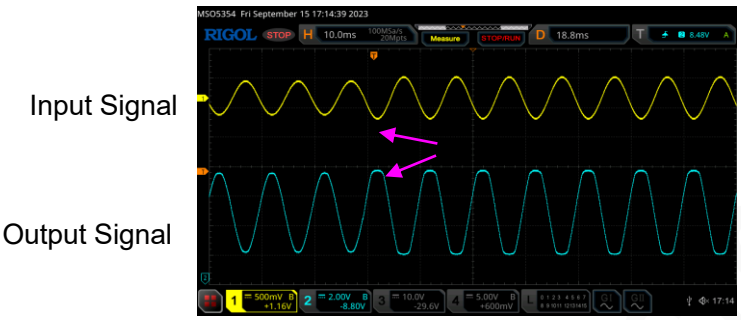


Fig 20-SCPL Operation

The SCPL pin limits the output peak-to-peak voltage based on the voltage supplied to this pin. The peak output voltage is limited to four times the voltage at the SCPL pin. Pull SCPL pin to a high (GVDD) turn off the Soft-Clipping Power Limiting.

DC Detect Protection

The TMS8609F has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the Fault pin as a low state. A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, +57%, -43%) for more than 850 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults. If automatic recovery from the DC protection latch is desired, connect the Fault pin directly to the SD pin. This allows the Fault pin function to automatically drive the SD pin low which clears the DC protection latch.

Over Temperature Protection (OTP)

Thermal protection on the TMS8609F prevents damage to the device when the internal die temperature exceeds 165°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault. Thermal protection faults are reported on the Fault pin. If automatic recovery from the thermal protection latch is desired, connect the Fault pin directly to the SD pin. This allows the Fault pin function to automatically drive the SD pin low which clears the thermal protection latch.

Application Information

SSM

The TMS8609F has built-in spread spectrum control of the oscillator frequency to improve EMI performance. Spread Spectrum Mode can be turned off by applied a high level to MODE pin.

POP and Click Circuitry

The TMS8609F contains circuitry to minimize turn-on and turn-off transients or “click and pops”, where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage, 1/2 GVDD. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Application Information

Layout Guide

The TMS8609F can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVDD and AVDD pins as possible. Large (220μF or greater) bulk power supply decoupling capacitors should be placed near the TMS8609F on the PVDDL and PVDDR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVDD pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220pF and 1000pF and a larger mid-frequency cap of value between 0.1μF and 1μF also of good quality to the PVDD connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVDD (pin 7) decoupling capacitor should be connected to analog ground. The PVDD decoupling capacitors should connect to power ground. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TMS8609F.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. For an example layout as below.

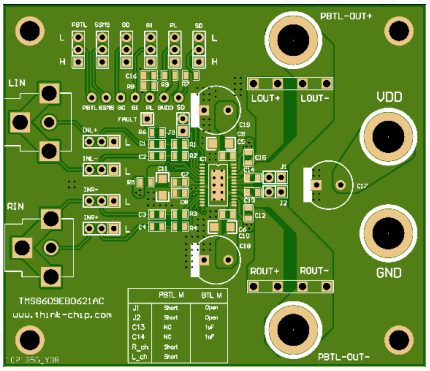


Fig 21-PCB Top Layer

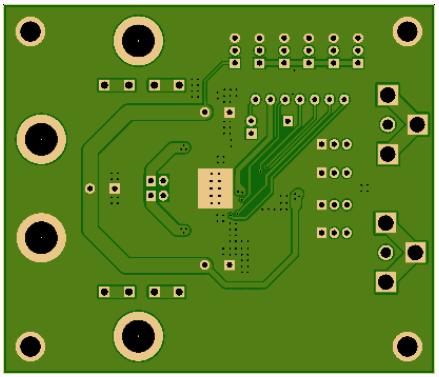
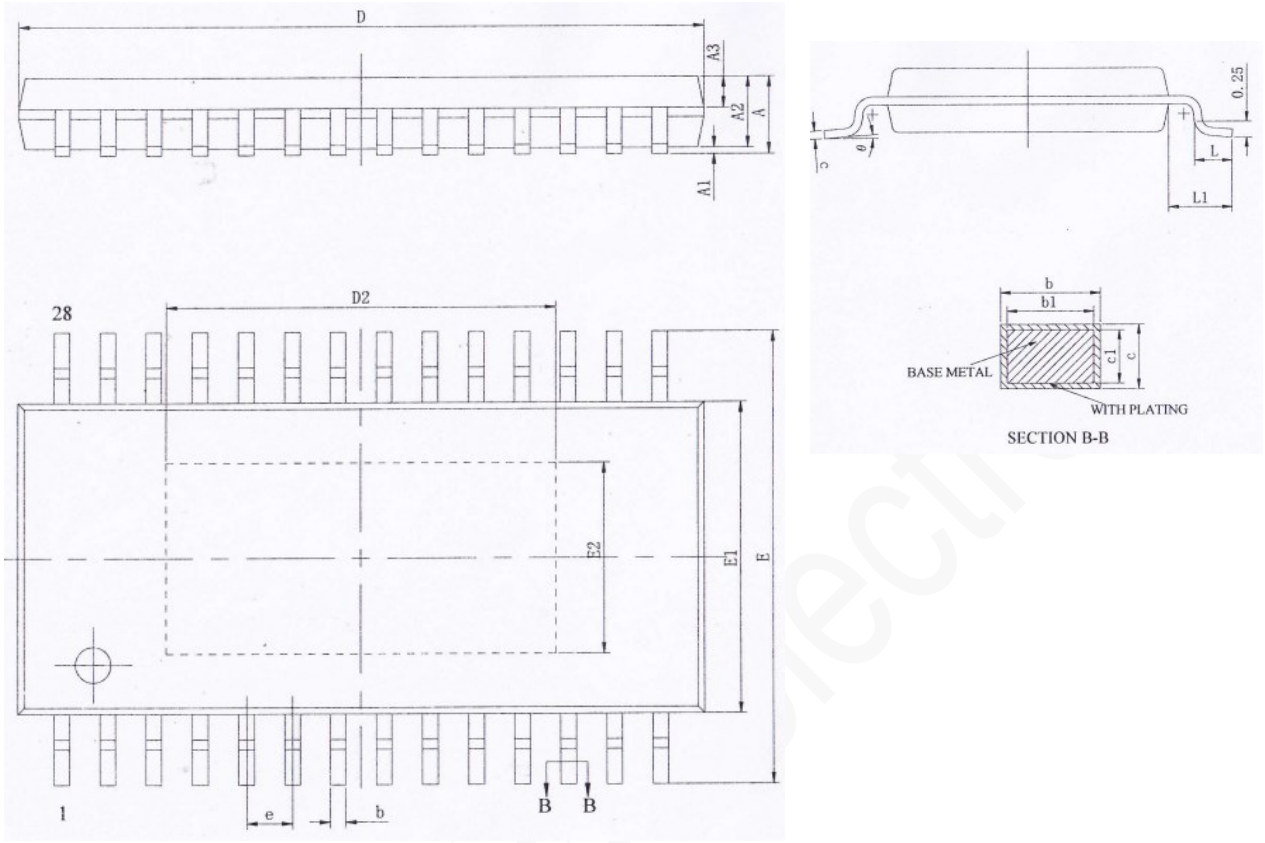


Fig 22-PCB Bottom Layer

Package Information

Package: HTSSOP28



Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Typ.	Max		Min	Typ.	Max
A	-	-	1.20	c1	0.12	0.13	0.15
A1	0.05	-	0.15	D	9.60	9.70	9.80
A2	0.80	-	1.00	E	6.20	6.40	6.60
A3	0.39	0.44	0.49	E1	4.30	4.40	4.50
b	0.20	-	0.29	e	0.65 BSC		
b1	0.19	0.22	0.25	L	0.45	0.60	0.75
c	0.13	-	0.18	L1	1.00 BSC		
D2	5.50 REF			θ	0	-	8°
E2	2.70 REF						

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