# SGM2065
# 1A, Low Noise, Ultra-Low Dropout Bias Rail CMOS Voltage Regulator

## GENERAL DESCRIPTION

The SGM2065 is a low noise, low dropout voltage linear regulator which is designed using CMOS technology. It provides 1A output current capability. The operating input voltage range is from 0.8V to 5.5V and bias supply voltage range is from 2.8V to 5.5V. The output voltage range is from 0.8V to 3.5V.

Other features include logic-controlled shutdown mode, short-circuit current limit and thermal shutdown protection. The SGM2065 has automatic discharge function to quickly discharge $V_{OUT}$ in the disabled status.

The SGM2065 is available in a Green XTDFN-1.2×1.2-6L package. It operates over an operating temperature range of -40℃ to +125℃.

## FEATURES

- **1A Nominal Output Current**
- **Input Voltage Range: 0.8V to 5.5V**
- **Bias Voltage Range: 2.8V to 5.5V**
- **Adjustable Output Voltage Range: 0.8V to 3.5V**
- **Low Dropout Voltage: 240mV (TYP) at 1A**
- **Low Bias Input Current: 37μA (TYP)**
- **Very Low Bias Input Current in Shutdown: 0.01μA (TYP)**
- **Low Noise: 25μ$V_{RMS}$ (TYP)**
- **Output Current Limit**
- **Thermal Shutdown Protection**
- **Fast Load Transient Response**
- **Logic Level Enable Input for ON/OFF Control**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green XTDFN-1.2×1.2-6L Package**

## APPLICATIONS

Portable Equipment
Smartphone
Industrial and medical Equipment

## TYPICAL APPLICATION

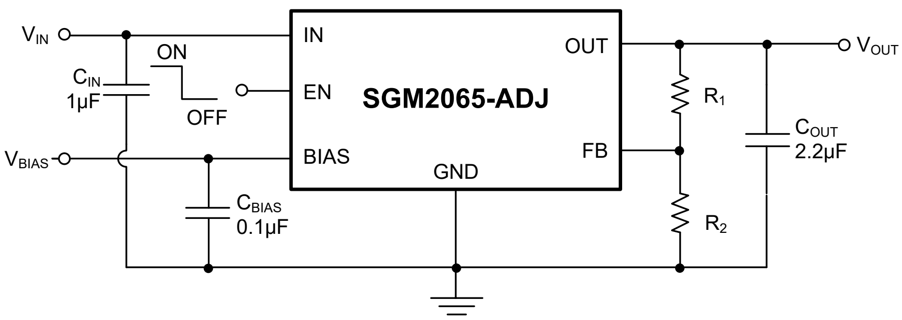



**Figure 1. Typical Application Circuit**

## PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM2065-ADJ | XTDFN-1.2×1.2-6L | -40℃ to +125℃ | SGM2065-ADJXXED6G/TR | 3H<br>XX | Tape and Reel, 5000 |

### MARKING INFORMATION

NOTE: XX = Date Code.

YY — Serial Number
XX
Date Code - Week
Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

### ABSOLUTE MAXIMUM RATINGS

IN, BIAS, EN to GND .......................................... -0.3V to 6V
OUT, FB to GND ....................... -0.3V to Min($V_{IN}$ + 0.3V, 6V)
Package Thermal Resistance
XTDFN-1.2×1.2-6L, $\theta_{JA}$........................................... 195℃/W
Junction Temperature .................................................+150℃
Storage Temperature Range........................-65℃ to +150℃
Lead Temperature (Soldering, 10s).............................+260℃
ESD Susceptibility
HBM.............................................................................8000V
CDM ............................................................................1000V

### RECOMMENDED OPERATING CONDITIONS

Operating Input Voltage Range, $V_{IN}$....................0.8V to 5.5V
Operating Bias Voltage Range, $V_{BIAS}$..................2.8V to 5.5V
BIAS Effective Capacitance, $C_{BIAS}$ ...................... 0.1μF (MIN)
Input Effective Capacitance, $C_{IN}$ ......................... 0.5μF (MIN)
Output Effective Capacitance, $C_{OUT}$ .................... 1μF to 10μF
Operating Junction Temperature Range .......-40℃ to +125℃

### OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

### ESD SENSITIVITY CAUTION

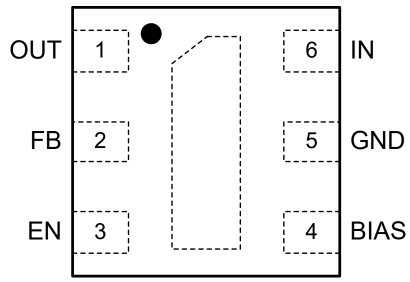
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

### DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




XTDFN-1.2×1.2-6L

## PIN DESCRIPTION

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | OUT | Regulated Output Voltage Pin. It is recommended to use output capacitor with effective capacitance in the range of 1μF to 10μF. |
| 2 | FB | Feedback Pin. Connect this pin to the external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin. |
| 3 | EN | Enable Pin. Driving EN high to turn on the regulator. Driving EN low to turn off the regulator. The EN pin has an internal pull-down resistance which ensures that the device is turned off when the EN pin is floated. |
| 4 | BIAS | Bias Voltage Supply Pin for Internal Control Circuits. This pin is monitored by internal under-voltage lockout circuit. |
| 5 | GND | Ground. |
| 6 | IN | Input Voltage Supply Pin. |
| Exposed Pad | – | Exposed Pad. Exposed pad is internally connected to GND. Connect it to a large ground plane to maximize thermal performance; not intended as an electrical connection point. |

# ELECTRICAL CHARACTERISTICS

($V_{BIAS}$ = 2.8V or ($V_{OUT(NOM)}$ + 2V) (whichever is greater), $V_{EN}$ = $V_{BIAS}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V, $I_{OUT}$ = 1mA, $C_{IN}$ = 1μF, $C_{BIAS}$ = 0.1μF, $C_{OUT}$ = 2.2μF, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Input Voltage Range | $V_{IN}$ | | $V_{OUT(NOM)}$ + $V_{DROP\_IN}$ | | 5.5 | V |
| Operating Bias Voltage Range | $V_{BIAS}$ | | 2.8 | | 5.5 | V |
| Under-Voltage Lockout Thresholds | $V_{UVLO}$ | $V_{BIAS}$ rising | | 1.6 | | V |
| | | Hysteresis | | 0.2 | | |
| Feedback Voltage | $V_{FB}$ | $V_{OUT}$ = $V_{FB}$, $I_{OUT}$ = 1mA to 1000mA | | 0.8 | | V |
| $V_{IN}$ Line Regulation | $\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$ | $V_{IN}$ = ($V_{OUT(NOM)}$ + 0.5V) to 5.5V | | 0.002 | | %/V |
| $V_{BIAS}$ Line Regulation | $\frac{\Delta V_{OUT}}{\Delta V_{BIAS} \times V_{OUT}}$ | $V_{BIAS}$ = 2.8V to 5.5V, $V_{OUT(NOM)}$ = 0.8V | | 0.002 | | %/V |
| Load Regulation | $\Delta V_{OUT}$ | $I_{OUT}$ = 1mA to 1000mA, $V_{OUT(NOM)}$ = 0.8V | | 0.5 | | mV |
| $V_{IN}$ Dropout Voltage (1) | $V_{DROP\_IN}$ | $I_{OUT}$ = 150mA | | 35 | | mV |
| | | $I_{OUT}$ = 500mA | | 120 | | |
| | | $I_{OUT}$ = 1000mA | | 240 | | |
| $V_{BIAS}$ Dropout Voltage (1, 2) | $V_{DROP\_BIAS}$ | $I_{OUT}$ = 500mA | | 1.2 | | V |
| | | $I_{OUT}$ = 1000mA | | 1.5 | | |
| Output Current Limit | $I_{LIM}$ | | | 1.3 | | A |
| Short-Circuit Current Limit | $I_{SHORT}$ | $V_{OUT}$ = 0V | | 0.4 | | A |
| FB Pin Input Current | $I_{FB}$ | | -100 | | 100 | nA |
| BIAS Pin Operating Current | $I_{BIAS}$ | $V_{BIAS}$ = 5.5V | | 37 | 58 | μA |
| IN Pin Disable Current | $I_{DIS\_IN}$ | $V_{EN}$ = 0V, $T_J$ = +25℃ | | 0.1 | 1.2 | μA |
| | | $V_{EN}$ = 0V, $T_J$ = -40℃ to +125℃ | | | 2 | |
| BIAS Pin Disable Current | $I_{DIS\_BIAS}$ | $V_{EN}$ = 0V, $T_J$ = +25℃ | | 0.01 | 1 | μA |
| | | $V_{EN}$ = 0V, $T_J$ = -40℃ to +125℃ | | | 2.8 | |
| EN Pin Threshold Voltage | $V_{IH}$ | EN input voltage high | 1.2 | | | V |
| | $V_{IL}$ | EN input voltage low | | | 0.25 | V |
| EN Pin Pull-Down Resistance | $R_{EN}$ | | 270 | 580 | 880 | kΩ |
| Turn-On Time | $t_{ON}$ | From assertion of $V_{EN}$ to $V_{OUT}$ = 90%$V_{OUT(NOM)}$ | | 100 | | μs |
| $V_{IN}$ Power Supply Rejection Ratio | PSRR | $V_{IN}$ to $V_{OUT}$, f = 1kHz, $V_{OUT(NOM)}$ = 1.0V, $I_{OUT}$ = 150mA, $V_{IN}$ ≥ 1.5V | | 71 | | dB |
| $V_{BIAS}$ Power Supply Rejection Ratio | | $V_{BIAS}$ to $V_{OUT}$, f = 1kHz, $V_{OUT(NOM)}$ = 1.0V, $I_{OUT}$ = 150mA, $V_{IN}$ ≥ 1.5V | | 76 | | |
| Output Voltage Noise | $e_n$ | $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5V, $V_{OUT(NOM)}$ = 1.0V, f = 10Hz to 100kHz | | 25 | | $μV_{RMS}$ |
| Output Discharge Resistance | $R_{DIS}$ | $V_{EN}$ = 0V, $V_{OUT}$ = 0.5V | 50 | 120 | 220 | Ω |
| Thermal Shutdown Temperature | $T_{SHDN}$ | | | 160 | | ℃ |
| Thermal Shutdown Hysteresis | $\Delta T_{SHDN}$ | | | 20 | | ℃ |

NOTES:

1. Dropout voltage is characterized when $V_{OUT}$ falls 5% below $V_{OUT(NOM)}$.
2. For output voltages below 1.3V, $V_{BIAS}$ dropout voltage does not apply due to a minimum bias operating voltage of 2.8V.

## FUNCTIONAL BLOCK DIAGRAM

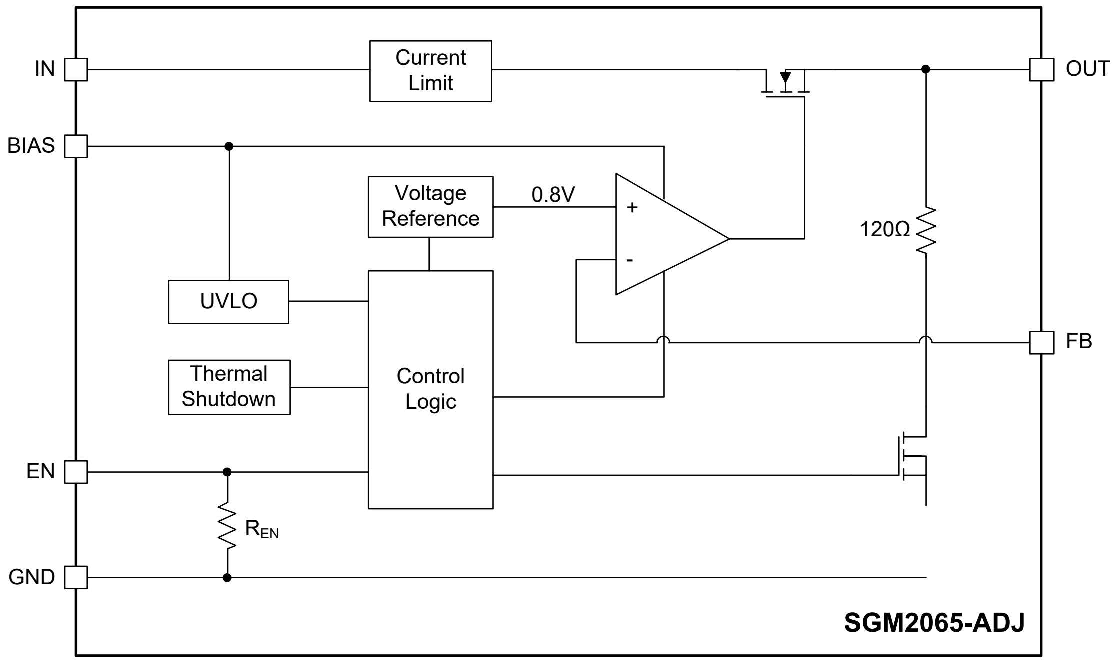



**Figure 2. Block Diagram**

# APPLICATION INFORMATION

The SGM2065 is a low noise, fast transient response high performance LDO, it consumes only 37μA (TYP) quiescent current and provides 1A output current. The SGM2065 provides the protection function for output overload, output short-circuit condition and overheating.

The SGM2065 is suitable for application which has noise sensitive circuit such as battery-powered equipment and smartphones.

## Input Capacitor Selection ($C_{IN}$)

The input decoupling capacitor is necessary to be connected as close as possible to the IN pin for ensuring the device stability. 1μF or greater X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When $V_{IN}$ is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

## Output Capacitor Selection ($C_{OUT}$)

The output decoupling capacitor should be located as close as possible to the OUT pin. 2.2μF or greater X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of $C_{OUT}$ that SGM2065 can remain stable is 1μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of $C_{OUT}$ must be considered in design. Larger capacitance and lower ESR $C_{OUT}$ will help improve the load transient response and increase the high frequency PSRR.

## Enable Operation

The SGM2065 uses the EN pin to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.25V, the device is in shutdown state, there is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 120Ω (TYP) resistor.

When the EN pin voltage is higher than 1.2V, the device is in active state, the input voltage is regulated to the output voltage and the automatic discharge transistor is turned off.

## Adjustable Regulator

The output voltage of the SGM2065 can be adjusted from 0.8V to 3.5V. The FB pin will be connected with two external resistors as shown in Figure 3, the output voltage is determined by the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

$V_{OUT}$ is output voltage and $V_{FB}$ is the internal voltage reference, $V_{FB}$ = 0.8V. Choose $R_2$ = 40kΩ to maintain a 20μA minimum load.

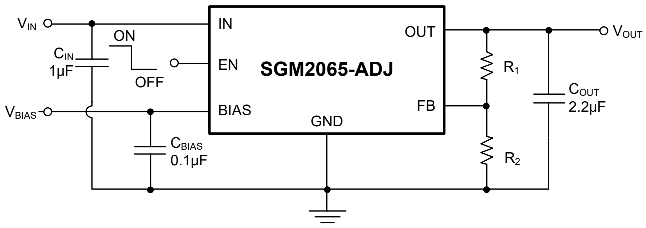



**Figure 3. Adjustable Output Voltage Application**

## Dropout Voltage

The SGM2065 specifies two dropout voltages because there are two power supplies $V_{IN}$ and $V_{BIAS}$ and one $V_{OUT}$ regulator output. $V_{IN}$ dropout voltage is defined as the difference between $V_{IN}$ and $V_{OUT}$ when $V_{OUT}$ falls 5% below $V_{OUT(NOM)}$. When the output voltage is lower than 1.3V, $V_{BIAS}$ dropout voltage does is not applicable because the minimum bias operating voltage is 2.8V.

When $V_{OUT}$ begins to decrease and $V_{BIAS}$ is high enough, the $V_{IN}$ dropout voltage equals to $V_{IN}$ - $V_{OUT}$. $V_{BIAS}$ dropout voltage refers to $V_{BIAS}$ - $V_{OUT}$ when the IN and BIAS pins are connected together and $V_{OUT}$ begins to decrease.

## Output Current Limit and Short-Circuit Protection

When overload events happen, the output current is internally limited to 1.3A (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 0.4A (TYP).

# APPLICATION INFORMATION (continued)

## Thermal Shutdown

The SGM2065 can detect the temperature of die. When the die temperature exceeds the threshold value of thermal shutdown, the SGM2065 will be in shutdown state and it will remain in this state until the die temperature decreases to +140℃.

## Power Dissipation ($P_D$)

Thermal protection limits power dissipation in the SGM2065. When power dissipation on pass element ($P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$) is too much that raise the operation junction temperature exceeds +160℃, the OTP circuit starts the thermal shutdown function and turns the pass element off. The power dissipation needs to be less than 1.5W when thermal protection occurs.

Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. To guarantee reliable operation, the junction temperature of the SGM2065 must not exceed 125℃.

The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be approximated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (2)$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction -to-ambient thermal resistance.

## Negatively Biased Output

When the output is negative voltage, the chip may not start-up due to parasitic effects. Ensure that the output is greater than -0.3V under all conditions. The load is too high can make $V_{OUT}$ < -0.3V, a Schottky diode can be added between the OUT pin and GND pin.

## Reverse Current Protection

The NMOS power transistor has an inherent body diode, this body diode will be forward biased when $V_{OUT} > V_{IN}$. When $V_{OUT} > V_{IN}$, the reverse current flowing from the OUT pin to the IN pin will damage the SGM2065. If $V_{OUT} > (V_{IN} + 0.3V)$ is expected in the application, one external Schottky diode will be added between the OUT pin and IN pin to protect the SGM2065.

## TYPICAL APPLICATION CIRCUIT

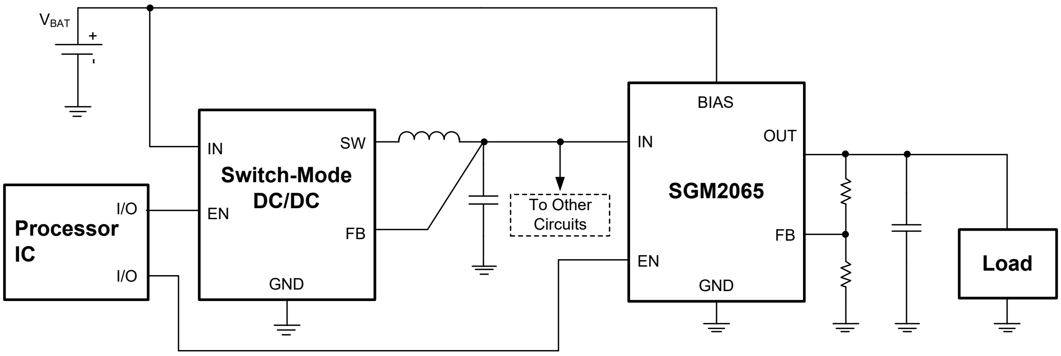
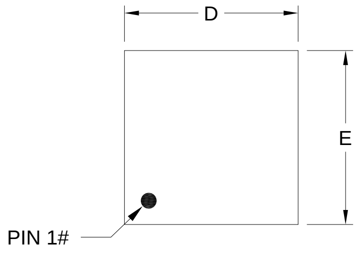


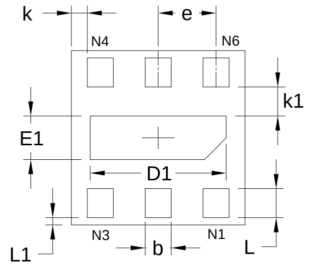

Figure 4. Used as DC/DC Post Regulator

# PACKAGE OUTLINE DIMENSIONS

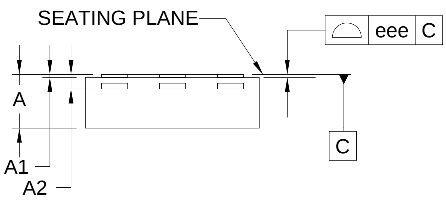
## XTDFN-1.2×1.2-6L



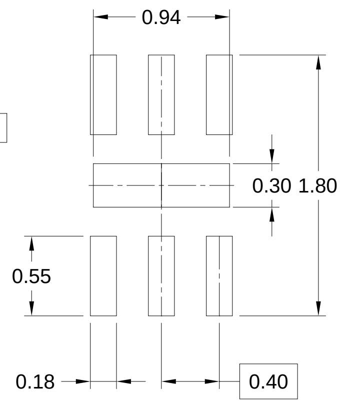

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**



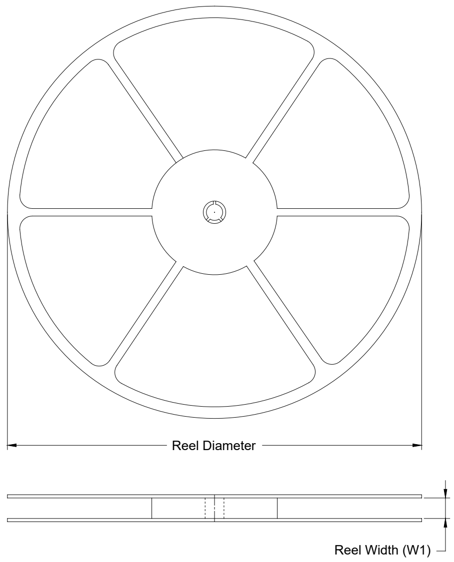

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | 0.340 | 0.370 | 0.400 |
| A1 | 0.000 | - | 0.050 |
| A2 | 0.100 REF | | |
| b | 0.130 | 0.180 | 0.230 |
| D | 1.100 | 1.200 | 1.300 |
| E | 1.100 | 1.200 | 1.300 |
| D1 | 0.890 | 0.940 | 0.990 |
| E1 | 0.250 | 0.300 | 0.350 |
| e | 0.300 | 0.400 | 0.500 |
| k | 0.110 REF | | |
| k1 | 0.150 | 0.200 | 0.250 |
| L | 0.150 | 0.200 | 0.250 |
| L1 | 0.000 | 0.050 | 0.100 |
| eee | 0.080 | | |

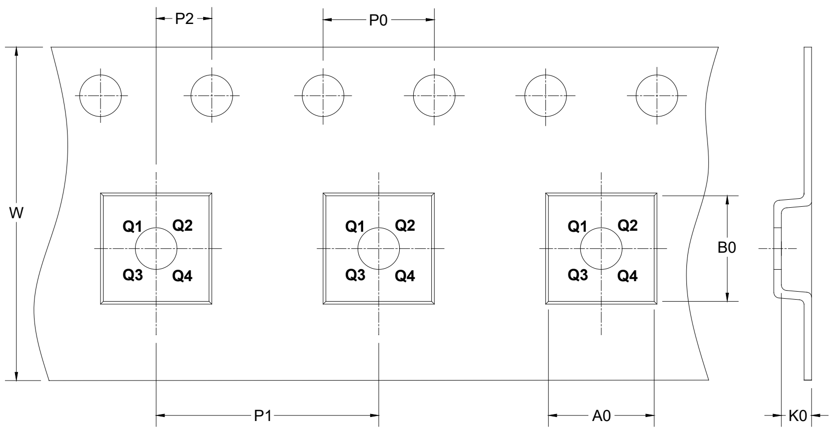
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS



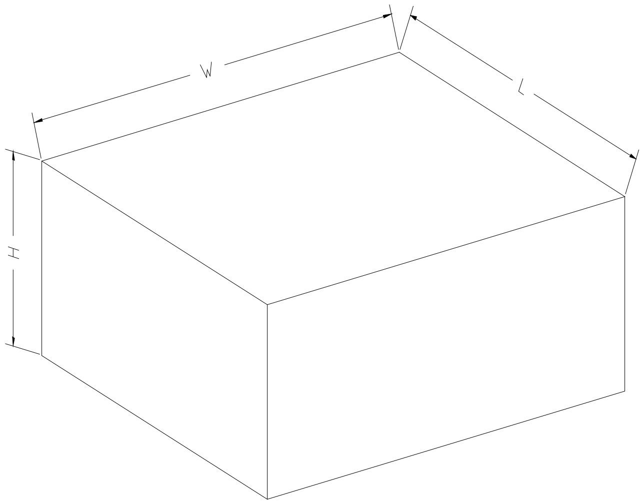

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| XTDFN-1.2×1.2-6L | 7″ | 9.5 | 1.37 | 1.37 | 0.55 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002