

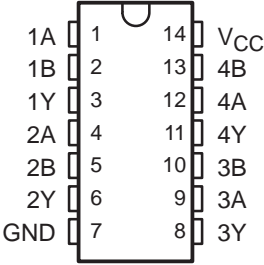
SN54ACT08, SN74ACT08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

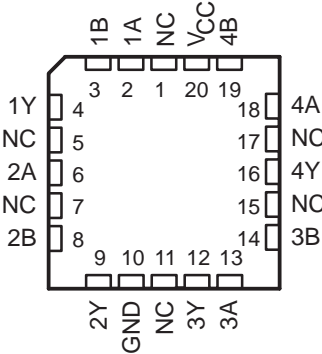
SCAS535C – SEPTEMBER 1995 – REVISED OCTOBER 2003

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 10 ns at 5 V
- Inputs Are TTL-Voltage Compatible

SN54ACT08 . . . J OR W PACKAGE
SN74ACT08 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT08 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The 'ACT08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74ACT08N	ACT08
	SOIC – D	Tube	SN74ACT08D	
		Tape and reel	SN74ACT08DR	
	SOP – NS	Tape and reel	SN74ACT08NSR	ACT08
	SSOP – DB	Tape and reel	SN74ACT08DBR	AD08
	TSSOP – PW	Tube	SN74ACT08PW	AD08
		Tape and reel	SN74ACT08PWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54ACT08J	SNJ54ACT08J
	CFP – W	Tube	SNJ54ACT08W	SNJ54ACT08W
	LCCC – FK	Tube	SNJ54ACT08FK	SNJ54ACT08FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

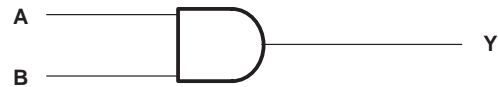
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

SN54ACT08, SN74ACT08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

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logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Table with 2 columns: Parameter and Rating. Parameters include Supply voltage range, Input voltage range, Output voltage range, Input clamp current, Output clamp current, Continuous output current, Continuous current through VCC or GND, Package thermal impedance for various packages, and Storage temperature range.

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

Table with 6 columns: Parameter, Symbol, and values for SN54ACT08 (MIN, MAX), SN74ACT08 (MIN, MAX), and UNIT. Parameters include Supply voltage, High-level input voltage, Low-level input voltage, Input voltage, Output voltage, High-level output current, Low-level output current, Input transition rise or fall rate, and Operating free-air temperature.

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54ACT08, SN74ACT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT08		SN74ACT08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I _{OH} = -50 mA†	5.5 V				3.85				
	I _{OH} = -75 mA†	5.5 V						3.85		
V _{OL}	I _{OL} = 50 µA	4.5 V		0.001	0.1		0.1		0.1	V
		5.5 V		0.001	0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA†	5.5 V					1.65			
	I _{OL} = 75 mA†	5.5 V							1.65	
I _I	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		80		20	µA
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.6			1.6		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		4.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54ACT08		SN74ACT08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	1	6.5	9	1	10	1	10	ns
t _{PHL}			1	6.5	9	1	10	1	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

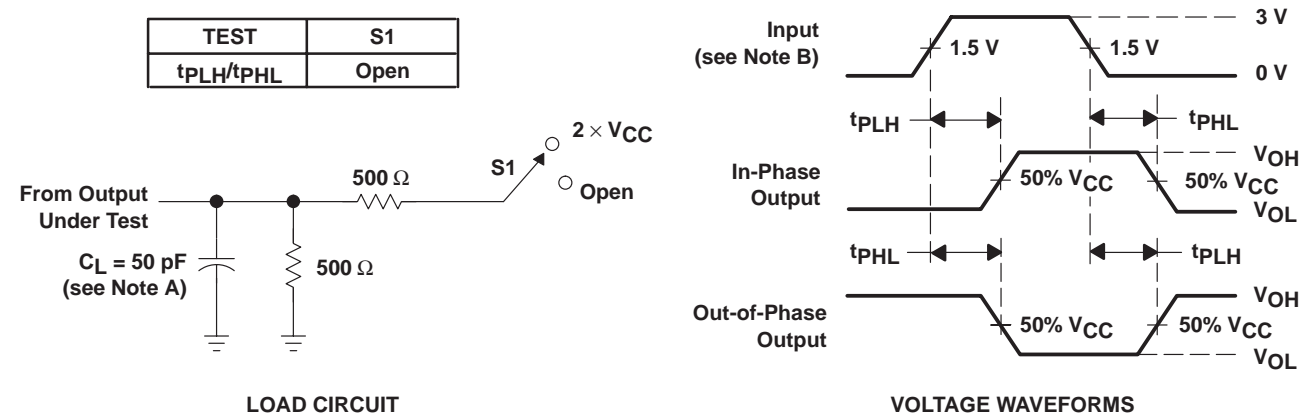
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	20	pF

SN54ACT08, SN74ACT08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \text{ }\Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

9-Mar-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89547022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 89547022A SNJ54ACT 08FK	Samples
5962-8954702CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702CA SNJ54ACT08J	Samples
5962-8954702DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702DA SNJ54ACT08W	Samples
SN74ACT08D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD08	Samples
SN74ACT08DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT08N	Samples
SN74ACT08NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD08	Samples
SN74ACT08PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	AD08	Samples
SN74ACT08PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD08	Samples
SNJ54ACT08FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 89547022A SNJ54ACT 08FK	Samples

PACKAGE OPTION ADDENDUM

9-Mar-2021

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54ACT08J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702CA SNJ54ACT08J	Samples
SNJ54ACT08W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702DA SNJ54ACT08W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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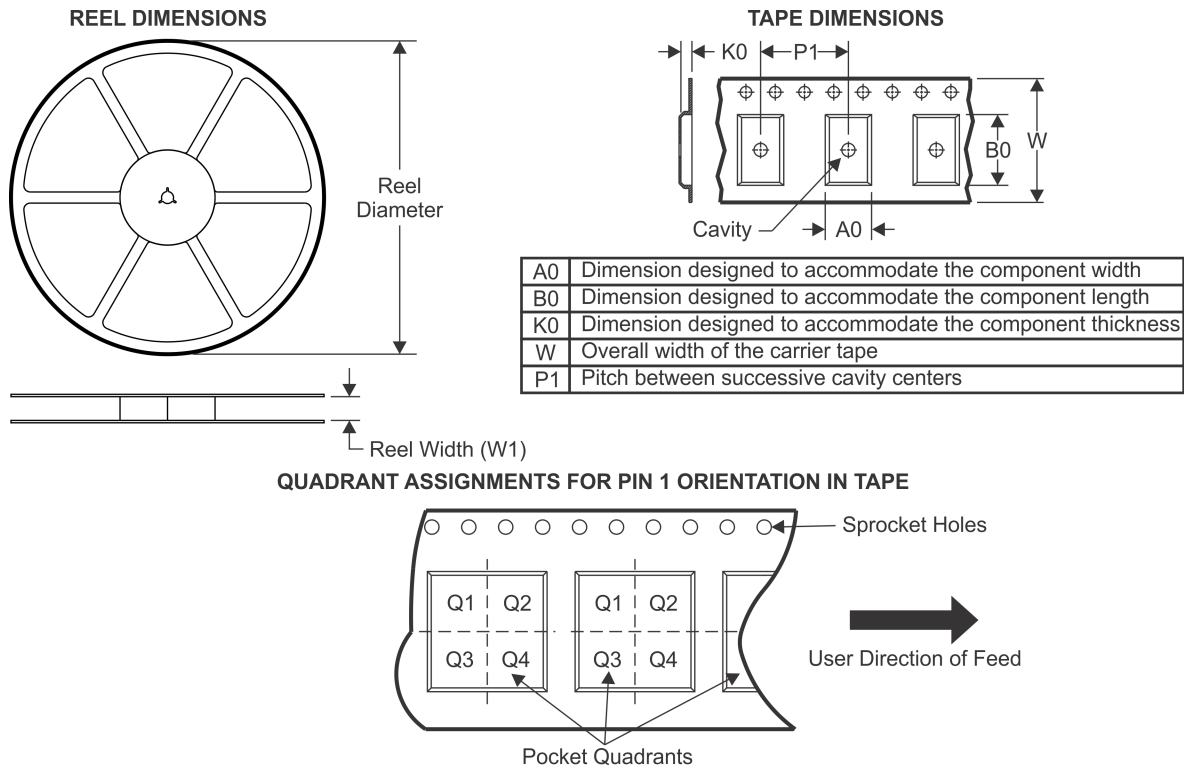
OTHER QUALIFIED VERSIONS OF SN54ACT08, SN74ACT08 :

- Catalog: [SN74ACT08](#)
- Enhanced Product: [SN74ACT08-EP](#), [SN74ACT08-EP](#)
- Military: [SN54ACT08](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



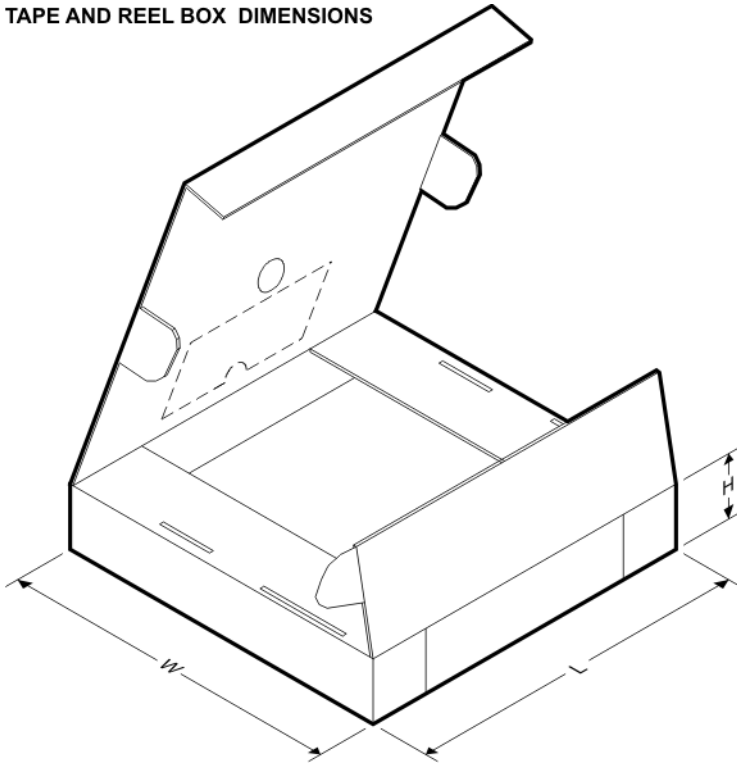
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT08DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74ACT08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT08DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74ACT08DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT08DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT08NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ACT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

3-Aug-2021

TAPE AND REEL BOX DIMENSIONS

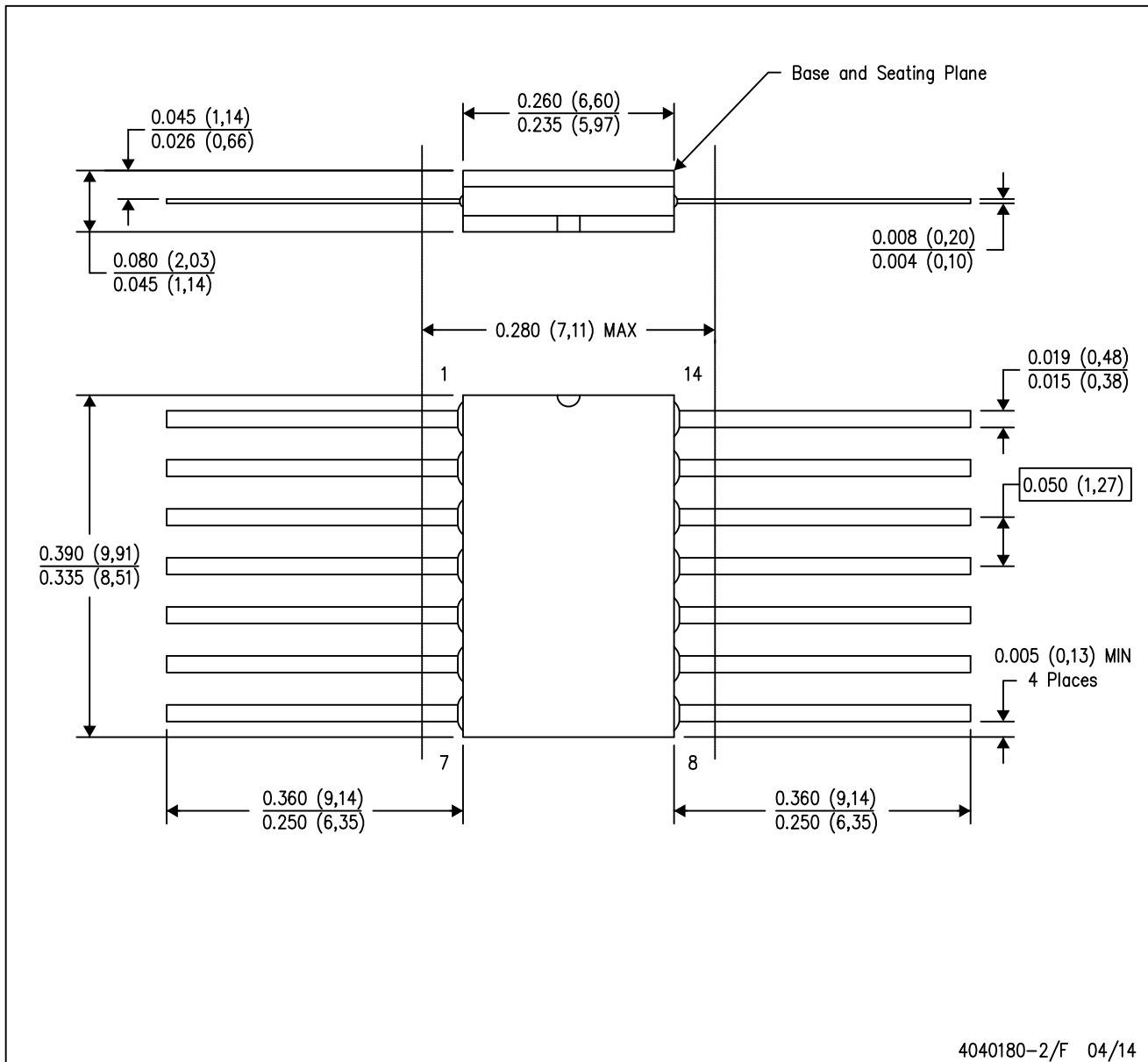


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT08DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74ACT08DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74ACT08DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74ACT08DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74ACT08DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74ACT08DRG4	SOIC	D	14	2500	853.0	449.0	35.0
SN74ACT08DRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74ACT08NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74ACT08PWR	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74ACT08PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74ACT08PWRG4	TSSOP	PW	14	2000	853.0	449.0	35.0

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



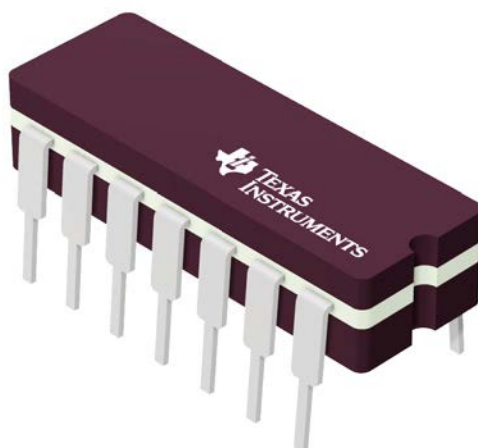
4040180-2/F 04/14

J 14

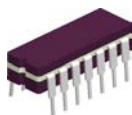
GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

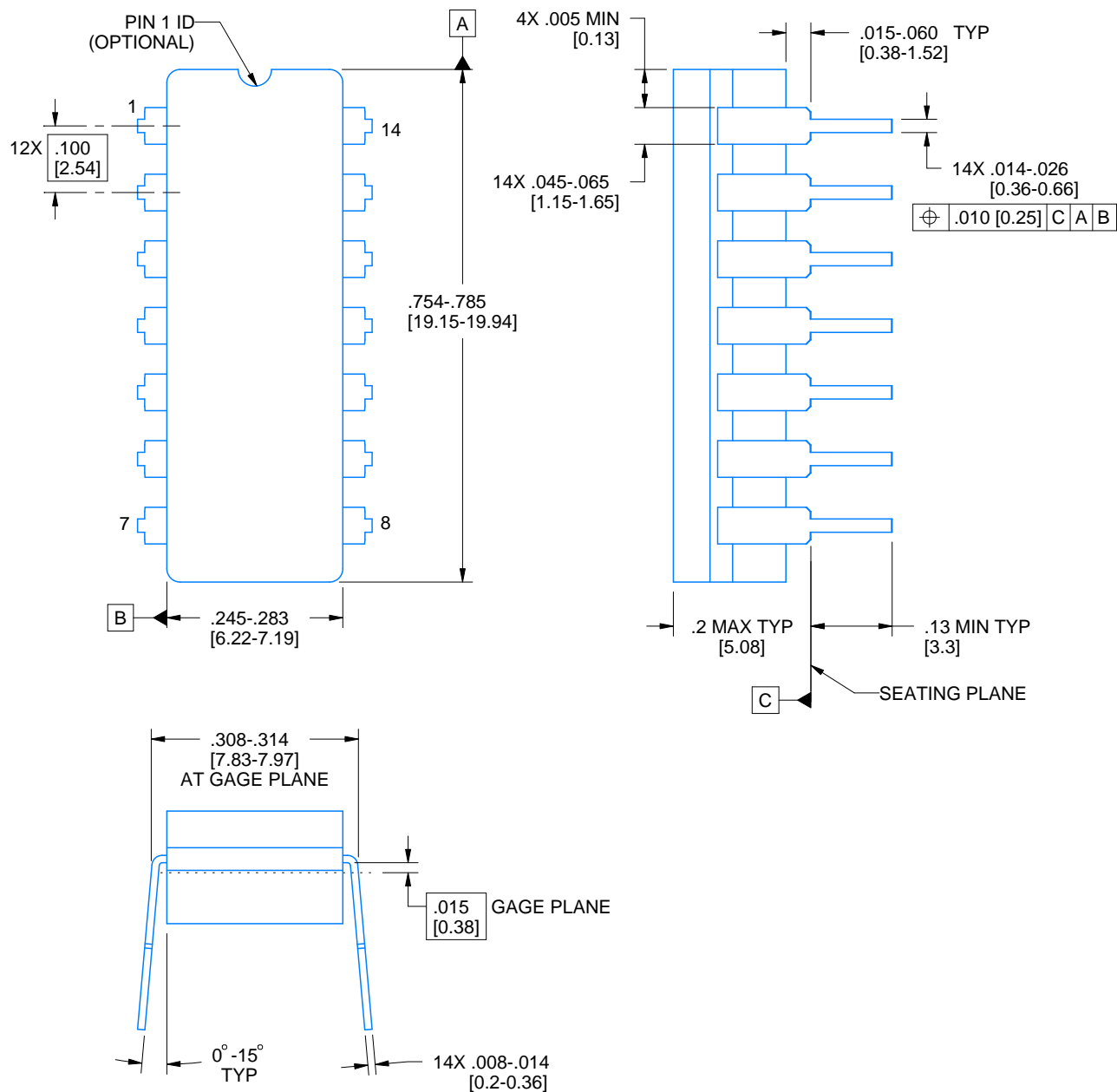


J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

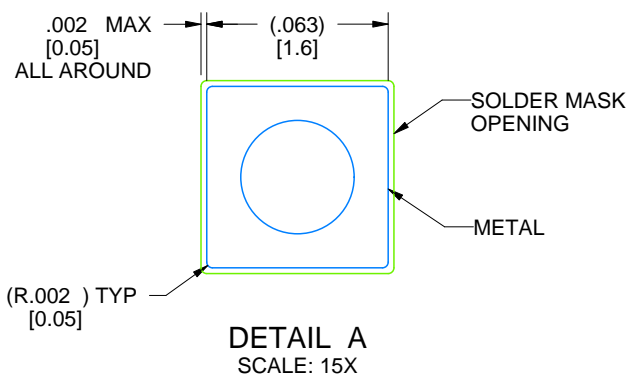
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

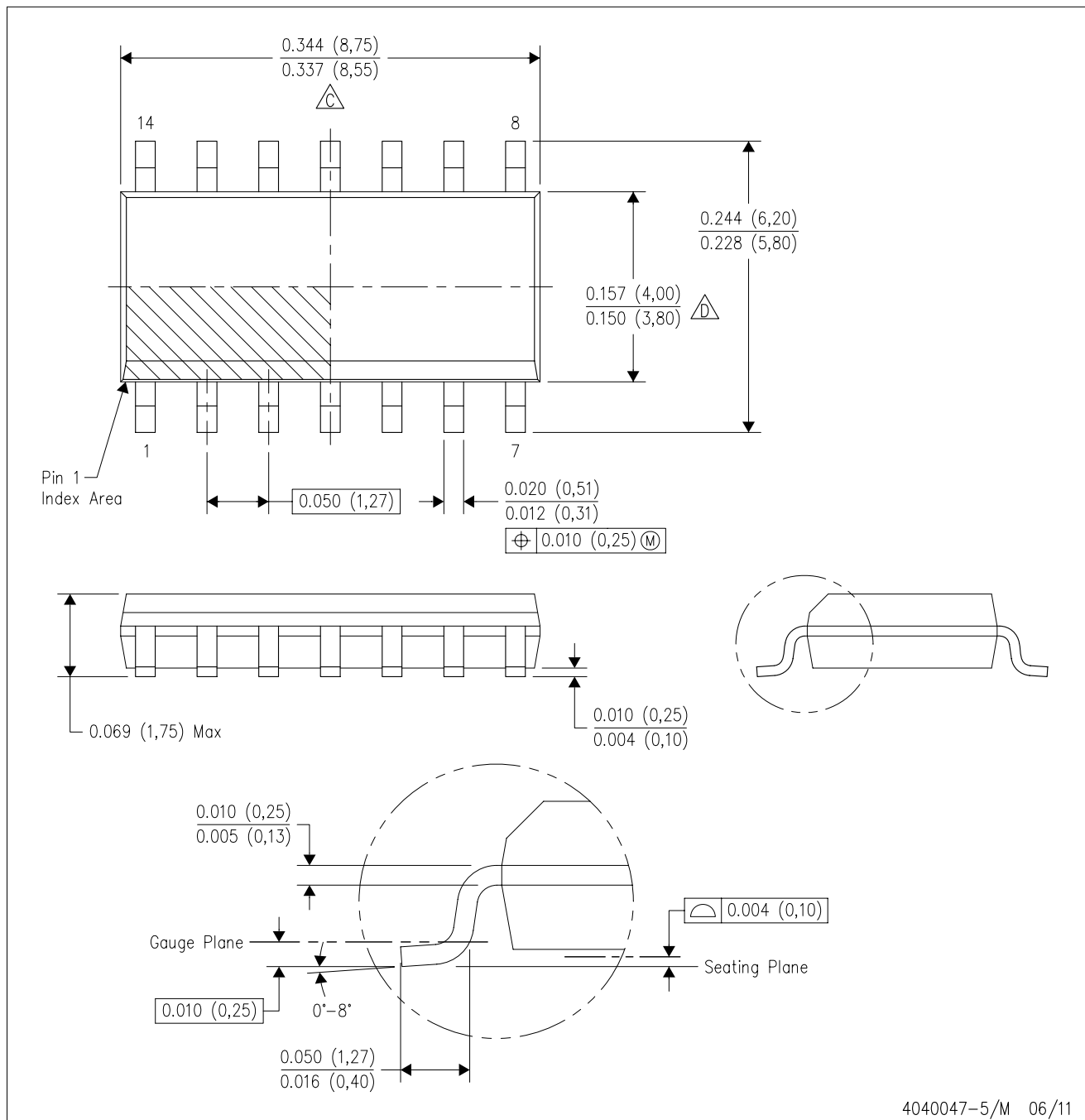


LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



D (R-PDSO-G14)

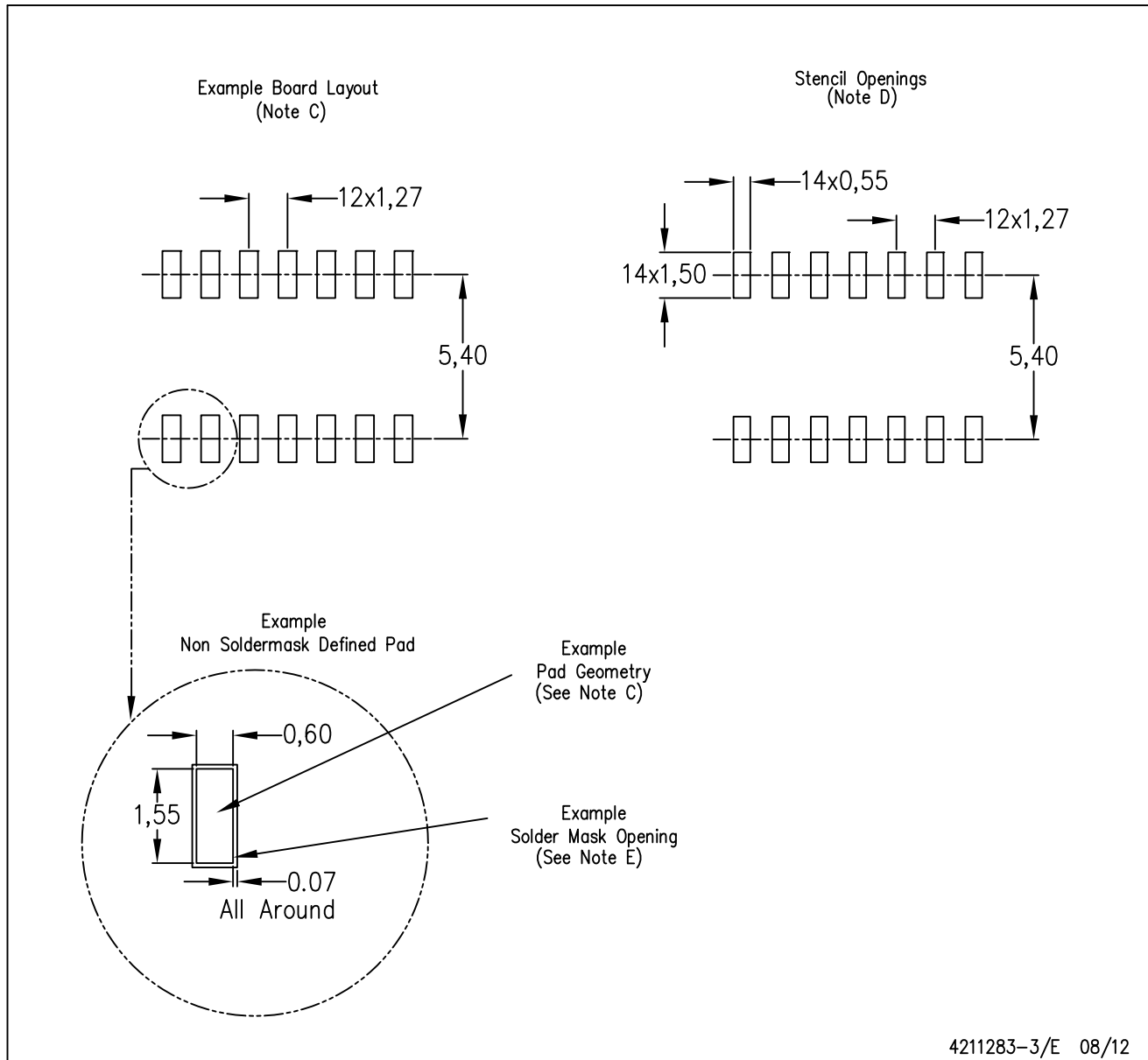
PLASTIC SMALL OUTLINE



4040047-5/M 06/11

D (R-PDSO-G14)

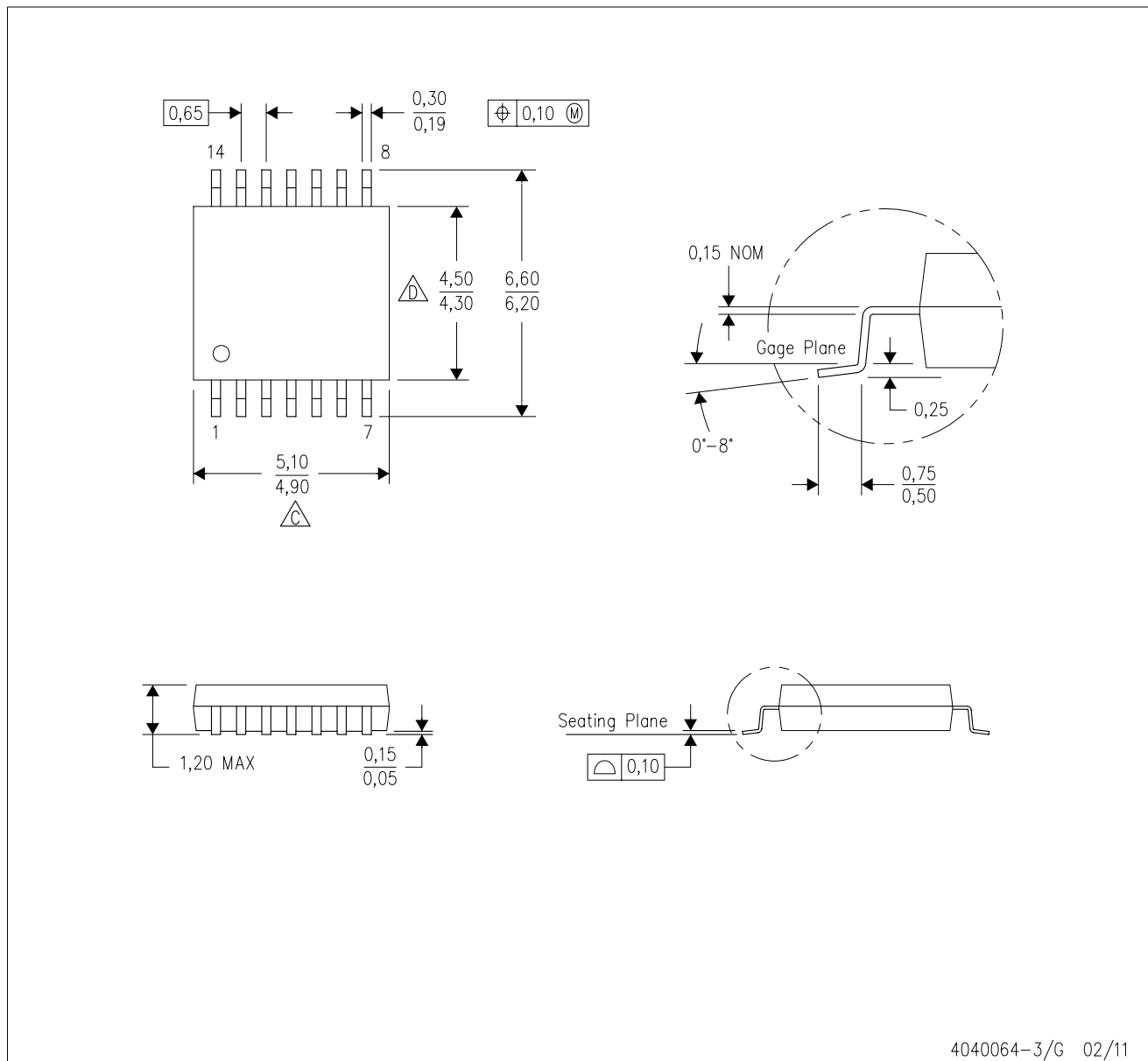
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

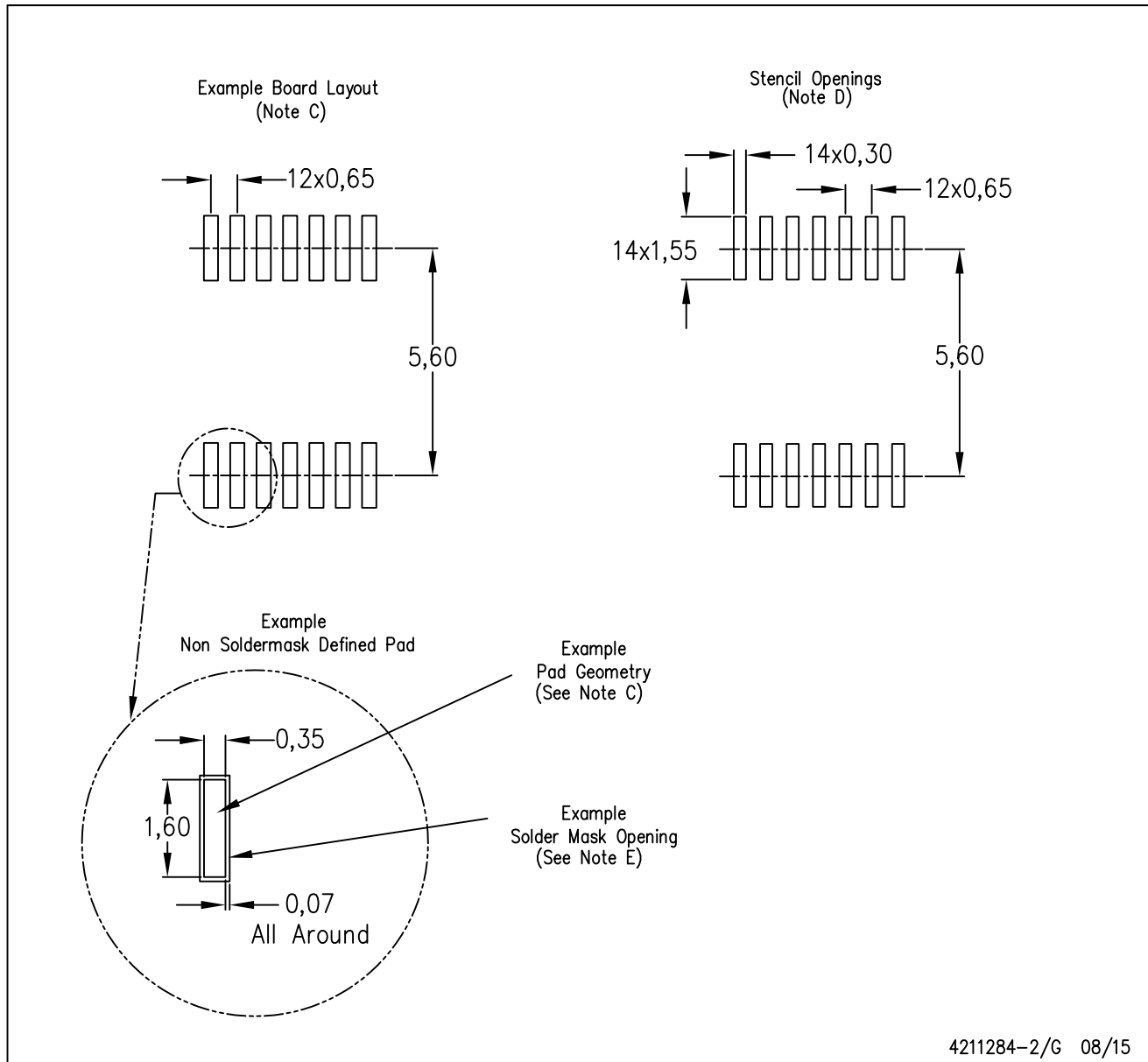


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

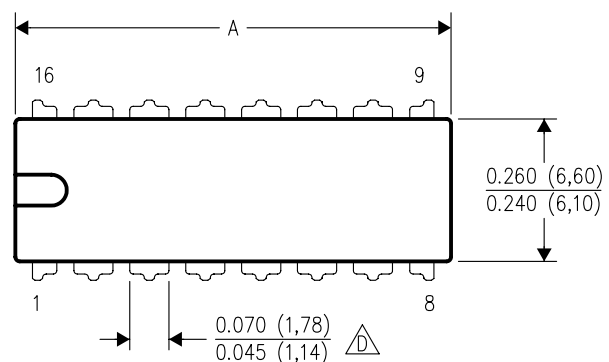


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

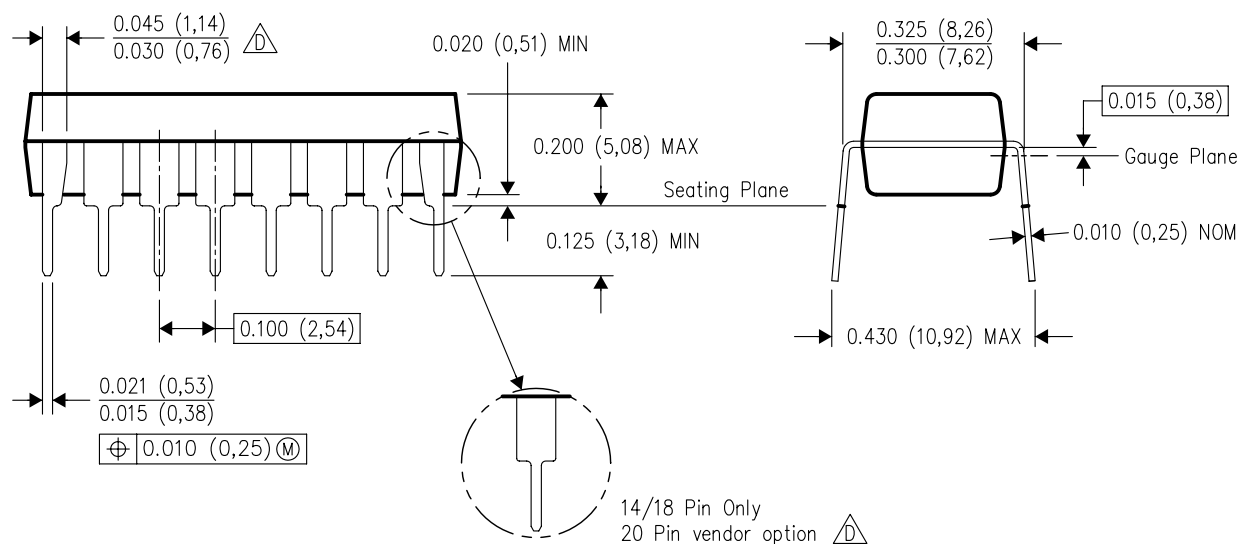
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



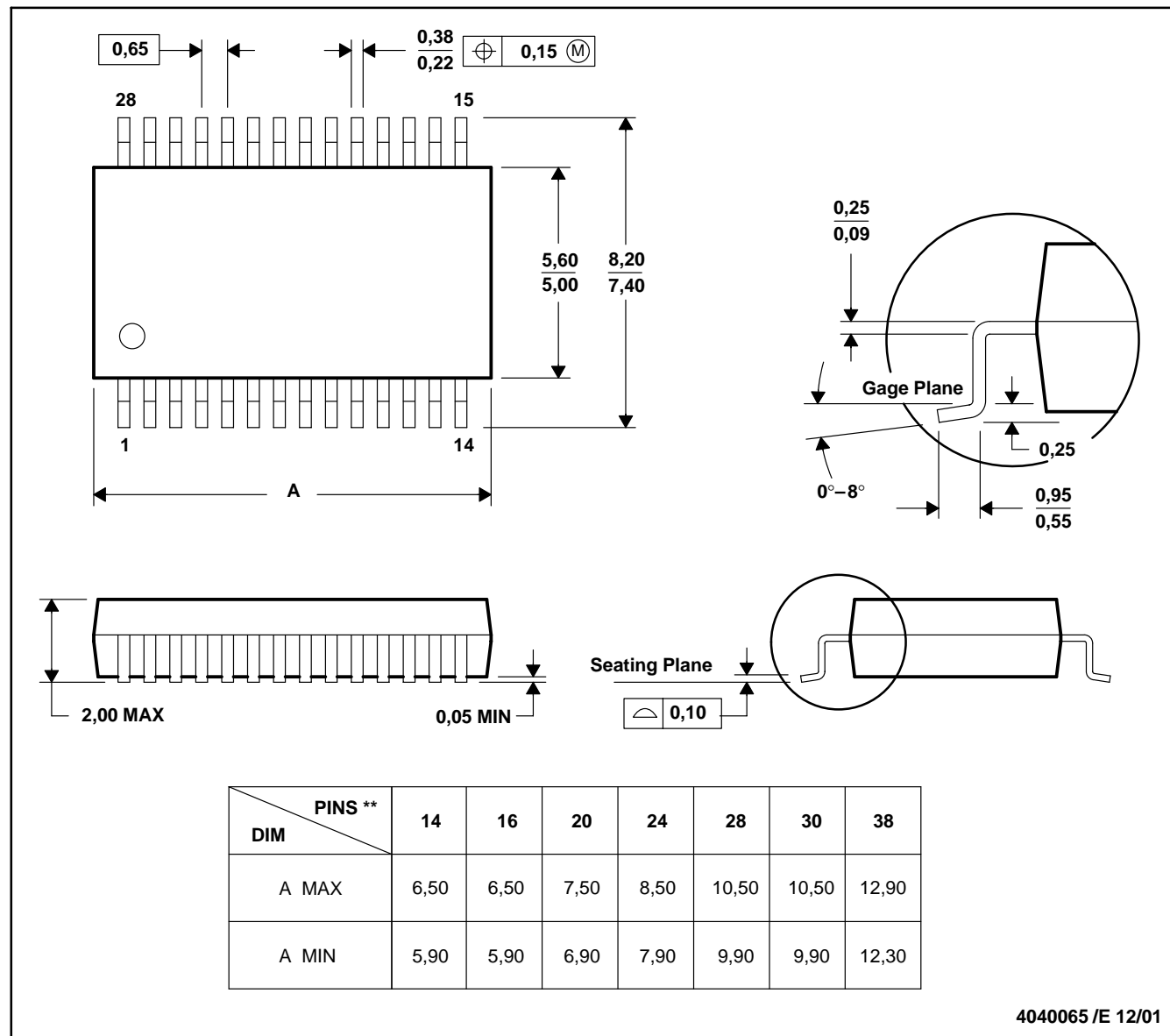
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

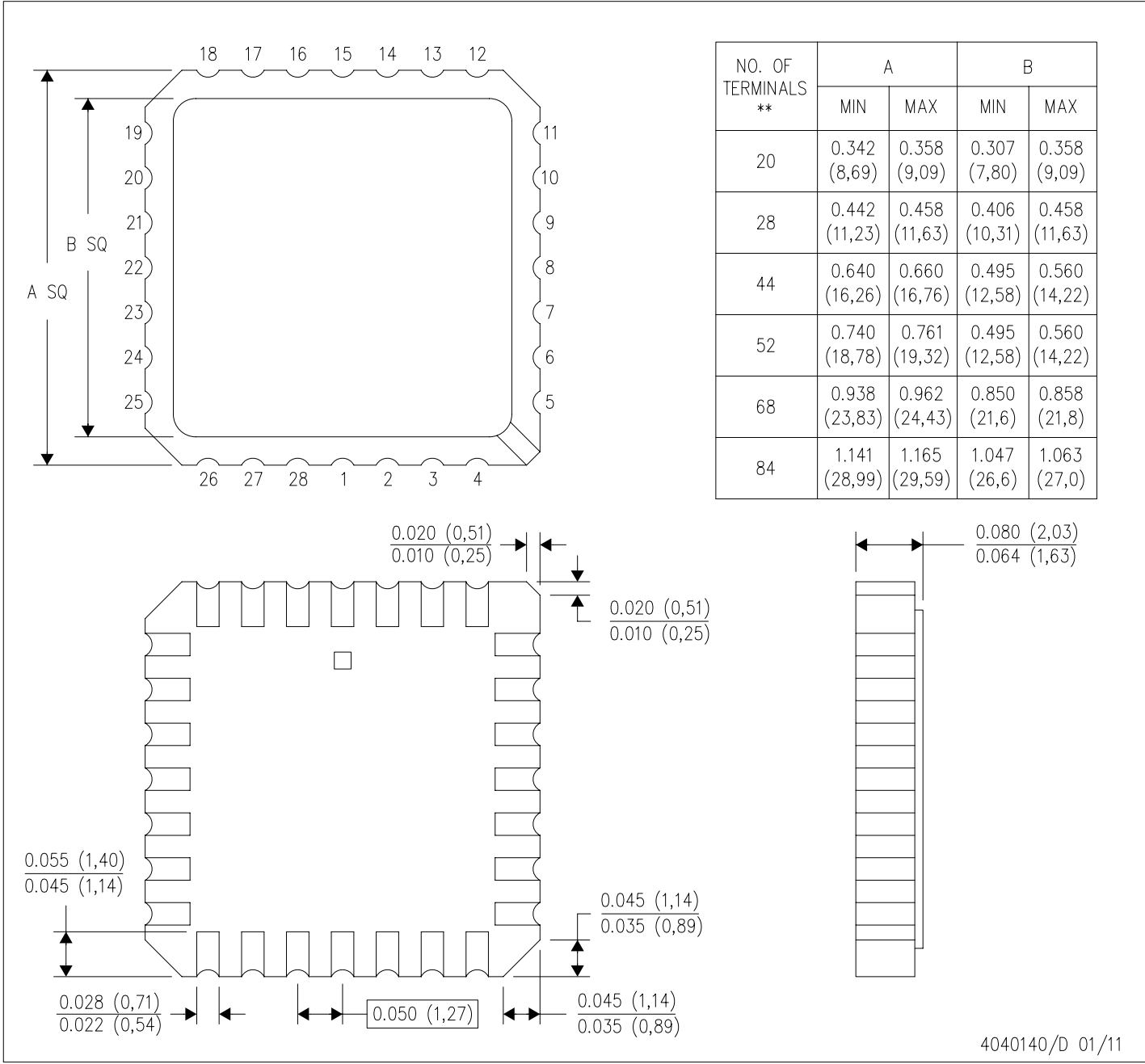
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

FK (S-CQCC-N**)
 28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



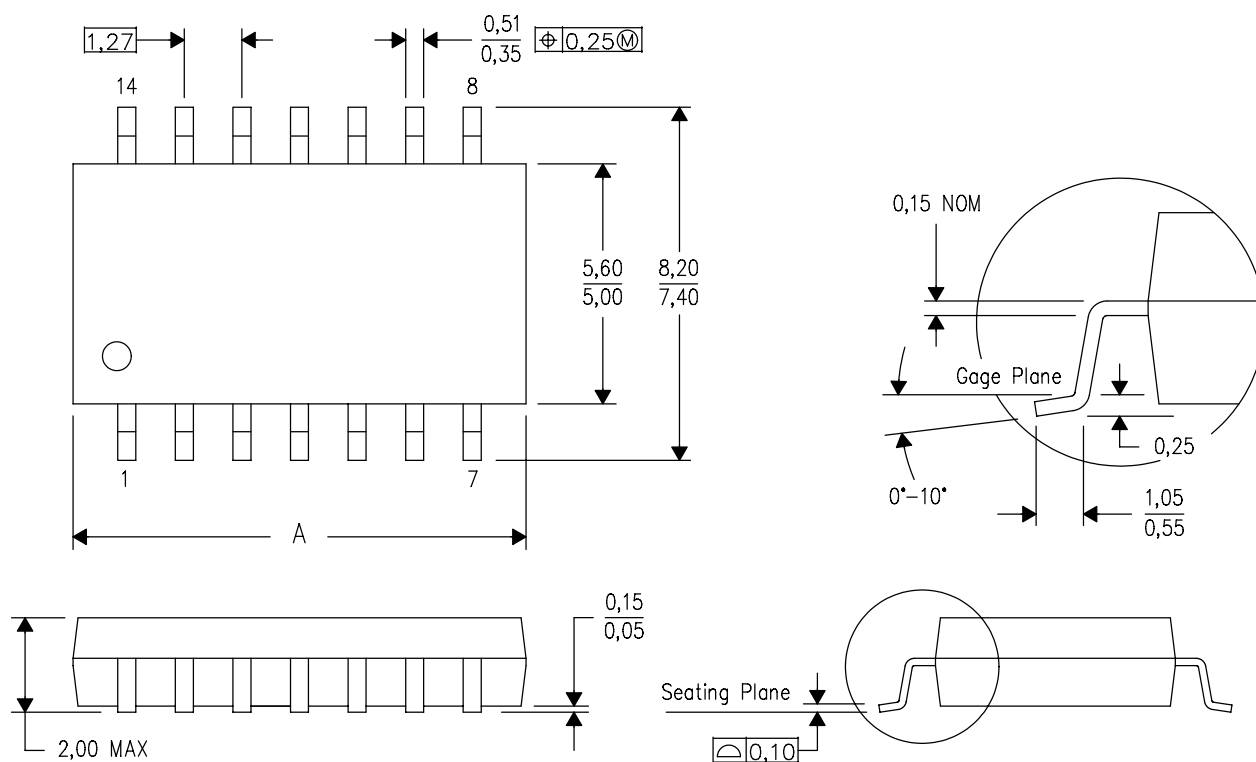
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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