

SGM6610 10A Fully-Integrated Synchronous Boost Converter

GENERAL DESCRIPTION

The SGM6610 is a high power density, fully integrated synchronous boost converter with a $11m\Omega$ power switch and a $13m\Omega$ rectifier switch to provide a high efficiency and small size solution in portable systems. The SGM6610 has wide input voltage range from 2.7V to 12V to support applications with single cell or two cell Lithium batteries. The device has 10A switch current capability and is capable of providing an output voltage up to 12.6V.

The SGM6610 uses peak current control topology to regulate the output voltage. In moderate to heavy load condition, the SGM6610 works in the Pulse Width Modulation (PWM) mode. In light load condition, the device has two operation modes selected by the MODE pin. One is the Pulse Frequency Modulation (PFM) mode to improve the efficiency and another one is the forced PWM mode to avoid application problems caused by low switching frequency. The switching frequency in the PWM mode is adjustable ranging from 200kHz to 2.2MHz by an external resistor. The SGM6610 also implements a programmable soft-start function and an adjustable switching peak current limit function. In addition, the device provides 13.2V output over-voltage protection cycle-by-cycle over-current protection, and thermal shutdown protection.

The SGM6610 is available in Green TQFN-4.5 \times 3.5-20L package. It operates over an ambient temperature range of -40 $^{\circ}$ C to +85 $^{\circ}$ C.

FEATURES

Input Voltage Range: 2.7V to 12V
Output Voltage Range: 4.5V to 12.6V

• 10A Switch Current

 Up to 91% Efficiency at V_{IN} = 3.3V, V_{OUT} = 9V and I_{OUT} = 3A

 Mode Selection Between PFM Mode and Forced PWM Mode at Light Load

• 1µA Current into VIN Pin during Shutdown

• Resistor-Programmable Switch Peak Current Limit

• Adjustable Switching Frequency: 200kHz to 2.2MHz

• Programmable Soft-Start

Output Over-Voltage Protection at 13.2V

• Cycle-by-Cycle Over-Current Protection

• Thermal Shutdown

Available in Green TQFN-4.5×3.5-20L Package

APPLICATIONS

Portable POS Terminal
Bluetooth Speaker
E-Cigarette
Thunderbolt Interface
Quick Charge Power Bank



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION	
SGM6610	TQFN-4.5×3.5-20L	-40°C to +85°C	SGM6610YTQS20G/TR	SGM6610 YTQS20 XXXXX	Tape and Reel, 4000	

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

BOOST Voltage	0.3V to SW + 6V
VIN, SW, FSW, VOUT Voltages	0.3V to 14.5V
EN, VCC, SS, COMP, MODE Voltages	0.3V to 6V
ILIM, FB Voltages	0.3V to 6V
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C

RECOMMENDED OPERATING CONDITIONS

Inductance, Effective Value, L	0.22µH to 4.7µH
Input Capacitance, Effective Value, C_{IN}	10µF (MIN)
Output Capacitance, Effective Value, Cour	τ6.8μF to 1000μF
Input Voltage Range	2.7V to 12V
Output Voltage Range	4.5V to 12.6V
Operating Ambient Temperature Range	40°C to +85°C
Operating Junction Temperature Range	40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

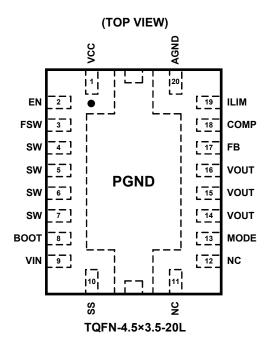
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION



PIN DESCRIPTION

500		110	FUNCTION
PIN	NAME	I/O	FUNCTION
1	VCC	0	Output of the Internal Regulator. A ceramic capacitor of more than 1µF is required between this pin and ground.
2	EN	I	Enable Logic Input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode.
3	FSW	I	The switching frequency is programmed by a resister between this pin and the AGND pin.
4, 5, 6, 7	SW	I	The Switching Node Pin of the Converter. It is connected to the drain of the internal low-side power MOSFET and source of the internal high-side power MOSFET.
8	воот	0	Power Supply for high-side MOSFET Gate Driver. A ceramic capacitor of 0.1µF must be connected between this pin and SW pin.
9	VIN	1	IC Power Supply Input.
10	SS	0	Soft-Start Programming Pin. An external capacitor sets the ramp rate of the internal error amplifier's reference voltage during soft-start.
11, 12	NC	ı	No Connection Inside the Device. Connect these two pins to ground plane on the PCB for good thermal dissipation.
13	MODE	I	Operation Mode Selection Pin for the Device in Light Load Condition. When this pin is connected to ground, the device works in PWM mode; when this pin is left floating, the device works in PFM mode.
14, 15, 16	VOUT	0	Boost Converter Output.
17	FB	I	Voltage Feedback. Connect to the center tape of a resistor divider to program the output voltage.
18	COMP	0	Output of the Internal Error Amplifier. The loop compensation network should be connected between this pin and the AGND pin.
19	ILIM	0	Adjustable Switch Peak Current Limit. An external resister should be connected between this pin and AGND pin.
20	AGND	_	Signal Ground of the IC.
Exposed Pad	PGND	_	Power Ground of the IC. It is connected to the source of the low-side MOSFET.

ELECTRICAL CHARACTERISTICS

(Minimum and maximum values are at V_{IN} = 2.7V to 5.5V and Full = -40°C to +85°C. Typical values are at V_{IN} = 3.6V and T_A = +25°C. L = 1.2 μ H, C_{OUT} = 47 μ F, unless otherwise specified noted.)

Public Voltage Range Vin	PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Vin Under-Voltage Lockout Threshold Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Threshold Vin Under-Voltage Vin	POWER SUPPLY							
Vin Under-Voltage Lockout Threshold Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Hysteresis Vin Under-Voltage Lockout Threshold Voc Under-Voltage Lockout Threshold Voc Under-Voltage Lockout Threshold Vin Pin Vin Pin Pin Vin Pin Pin Vin Pin Pin Vin Pin Pin Pin Pin Pin Pin Pin Pin Pin P	Input Voltage Range		V _{IN}		2.7		12	V
Vin Under-Voltage Lockout Hysteresis	\(\langle \)		.,	V _{IN} rising		2.5		.,
VCC Under-Voltage Lockout Threshold Vcc_UMAD Vcc_Efalling Vcc_UMAD	VIN Under-Voltage Lockout Thresh	nold	V _{IN_UVLO}	V _{IN} falling		2.4		V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	VIN Under-Voltage Lockout Hyster	esis	V _{IN_HYS}			100		mV
Departing Quiescent Current VOUT Pin Io 100 kΩ · Ves = 1.23 V · Vout = 12V 80 μA	VCC Under-Voltage Lockout Thres	shold	V _{CC_UVLO}	V _{CC} falling		2.1		V
VOUT Pin Vout Pin Pin Vout Pin Pin Pin Pin Vout Pin	0 " 0 " 10 "	VIN Pin		IC enabled, V _{EN} = 2V, no load, R _{IIIM} =		0.2		
Sistor Middle Connected to the VOUT pin V.3 V.5	Operating Quiescent Current	VOUT Pin	IQ			80		μΑ
EN AND MODE INPUT EN High Threshold Voltage	Shutdown Current into the IN Pin	1	I _{SHDN}			0.5		μA
No.	VCC Regulation		Vcc	I _{VCC} = 5mA, V _{IN} = 8V		5.0		V
EN Low Threshold Voltage V_{ENL} $V_{CC} = 5V$ 0.3 $0.$	EN AND MODE INPUT							
EN Internal Pull-Down Resistance R_{EN} $V_{CC} = 5V$ 800 RQ RQ RQ RQ RQ RQ RQ RQ	EN High Threshold Voltage		V_{ENH}	V _{CC} = 5V	1.5			V
MODE High Threshold Voltage V_{MODEH} $V_{CC} = 5V$ V	EN Low Threshold Voltage		V _{ENL}	V _{CC} = 5V			0.3	V
MODE Low Threshold Voltage V _{MODE} V _{CC} = 5V 800 KΩ	EN Internal Pull-Down Resistance		R _{EN}	V _{CC} = 5V		800		kΩ
MODE Internal Pull-Up Resistance R_{MODE} $V_{CC} = 5V$	MODE High Threshold Voltage		V_{MODEH}	V _{CC} = 5V	4.0			V
DUTPUT Dutput Voltage Range V_{OUT} V_{REF} V_{RE	MODE Low Threshold Voltage		V_{MODEL}	V _{CC} = 5V			1.5	V
Output Voltage Range Vout 4.5 12.6 V Reference Voltage at the FB Pin V_{REF} PWM mode 1.204 V FB Pin Leakage Current $I_{LKG_{LFB}}$ V_{FB} 0.1 nA Soft-Start Charging Current I_{SS} 5 μ A ERROR AMPLIFIER COMP Pin Sink Current I_{SINK} $V_{FB} = V_{REF} + 100mV$, $V_{COMP} = 1.2V$ 27 μ A COMP Pin Source Current I_{SOURCE} $V_{FB} = V_{REF} - 100mV$, $V_{COMP} = 1.2V$ 22 μ A High Clamp Voltage at the COMP Pin V_{CLPH} $V_{FB} = 1.1V$, $R_{ILIM} = 100k\Omega$, $V_{COMP} = 1.2V$ 2.0 V_{CLPH} Low Clamp Voltage at the COMP Pin V_{CCLPH} $V_{FB} = 1.3V$, $V_{RILIM} = 100k\Omega$, $V_{CDMP} = 1.0V$ 0.4 $V_{CDMP} = 1.0V$ POWER SWITCH $V_{CDMP} = 1.2V$ 140 $V_{CDMP} = 1.0V$ High-side MOSFET On-Resistance $V_{CDMP} = 1.2V$ 13 $M\Omega$ Low-side MOSFET On-Resistance $V_{CDMP} = 1.2V$ 13 $M\Omega$ Low-side MOSFET On-Resistance $V_{CDMP} = 1.2V$ 11 $M\Omega$ COURRENT LIMIT $V_{CDMP} = 1.2V$ $V_{CDMP} = $	MODE Internal Pull-Up Resistance	!	R _{MODE}	V _{CC} = 5V		800		kΩ
Reference Voltage at the FB Pin $V_{REF} = \begin{array}{c ccccccccccccccccccccccccccccccccccc$	OUTPUT							
Reference Voltage at the FB Pin V_{REF} V_{FB} V_{F	Output Voltage Range		V_{OUT}		4.5		12.6	V
PFM mode 1.206 FB Pin Leakage Current I_{LKG_FB} $V_{FB} = 1.2V$ 0.1	Potoronoo Voltago et the EP Din		V	PWM mode		1.204		\/
Soft-Start Charging Current I_{SS} 5 μ A ERROR AMPLIFIER COMP Pin Sink Current I_{SINK} $V_{FB} = V_{REF} + 100\text{mV}, V_{COMP} = 1.2\text{V}$ 27 μ A COMP Pin Source Current I_{SOURCE} $V_{FB} = V_{REF} - 100\text{mV}, V_{COMP} = 1.2\text{V}$ 22 μ A High Clamp Voltage at the COMP Pin V_{CCLPH} $V_{FB} = 1.1\text{V}, R_{ILIM} = 100\text{k}\Omega$ 2.0 V_{CCLPH} $V_{FB} = 1.3\text{V}, R_{ILIM} = 100\text{k}\Omega$, MODE pin floating V_{CCLPL} V_{CCLPL} $V_{COMP} = 1.2\text{V}$ 140 V_{CCLPL} POWER SWITCH High-side MOSFET On-Resistance V_{CCLPL} $V_{$	Reference voltage at the FB Fill		V REF	PFM mode		1.206		\ \ \
ERROR AMPLIFIER COMP Pin Sink Current I_{SINK} $V_{FB} = V_{REF} + 100 \text{mV}, V_{COMP} = 1.2 \text{V}$ 27 μA COMP Pin Source Current I_{SOURCE} $V_{FB} = V_{REF} - 100 \text{mV}, V_{COMP} = 1.2 \text{V}$ 22 μA High Clamp Voltage at the COMP Pin V_{CCLPH} $V_{FB} = 1.1 \text{V}, R_{ILIM} = 100 \text{k}\Omega$ 2.0 V_{CCLPH} $V_{FB} = 1.3 \text{V}, R_{ILIM} = 100 \text{k}\Omega$, MODE pin floating V_{CCLPL} V_{CCLPL} V_{CCLPL} V_{CCLPL} $V_{COMP} = 1.2 \text{V}$ $V_{CCMP} = 1.$	FB Pin Leakage Current		I _{LKG_FB}	V _{FB} = 1.2V		0.1		nA
COMP Pin Sink Current I_{SINK} $V_{FB} = V_{REF} + 100 \text{mV}, V_{COMP} = 1.2 \text{V}$ 27 μA COMP Pin Source Current I_{SOURCE} $V_{FB} = V_{REF} - 100 \text{mV}, V_{COMP} = 1.2 \text{V}$ 22 μA High Clamp Voltage at the COMP Pin V_{CCLPH} $V_{FB} = 1.1 \text{V}, R_{ILIM} = 100 \text{k}\Omega$ V_{CCLPL} $V_{FB} = 1.3 \text{V}, R_{ILIM} = 100 \text{k}\Omega$, MODE pin floating V_{CCLPL}	Soft-Start Charging Current		I _{SS}			5		μA
COMP Pin Source Current I_{SOURCE} $V_{FB} = V_{REF} - 100 \text{mV}, V_{COMP} = 1.2 \text{V}$ 22 μA High Clamp Voltage at the COMP Pin V_{CCLPH} $V_{FB} = 1.1 \text{V}, R_{ILIM} = 100 \text{k}\Omega$ 2.0 V Low Clamp Voltage at the COMP Pin V_{CCLPL} $V_{FB} = 1.3 \text{V}, R_{ILIM} = 100 \text{k}\Omega, MODE pin floating}$ 0.4 V Error Amplifier Transconductance G_{EA} $V_{COMP} = 1.2 \text{V}$ $V_{CCMP} = 1.2 \text{V}$ V_{CCMP}	ERROR AMPLIFIER							
High Clamp Voltage at the COMP Pin V_{CCLPL} $V_{FB} = 1.1V$, $R_{ILIM} = 100k\Omega$ 2.0 V Low Clamp Voltage at the COMP Pin V_{CCLPL} $V_{FB} = 1.3V$, $R_{ILIM} = 100k\Omega$, MODE pin floating 0.4 V Error Amplifier Transconductance G_{EA} $V_{COMP} = 1.2V$ 140 μ A/V POWER SWITCH High-side MOSFET On-Resistance $R_{DS(ON)}$	COMP Pin Sink Current		I _{SINK}	$V_{FB} = V_{REF} + 100$ mV, $V_{COMP} = 1.2$ V		27		μΑ
Low Clamp Voltage at the COMP Pin V_{CCLPL} $V_{FB} = 1.3V$, $R_{ILIM} = 100k\Omega$, MODE pin floating V_{CCLPL} $V_{FB} = 1.3V$, $V_{FB} = 1$	COMP Pin Source Current		I _{SOURCE}	$V_{FB} = V_{REF} - 100 \text{mV}, V_{COMP} = 1.2 \text{V}$		22		μΑ
Error Amplifier Transconductance G_{EA} $V_{COMP} = 1.2V$ 140 μ AVV POWER SWITCH High-side MOSFET On-Resistance $R_{DS(ON)}$ $V_{CC} = 5V$ 13 $m\Omega$ CURRENT LIMIT Peak Switch Current Limit I_{LIM} $R_{ILIM} = 100k\Omega, V_{CC} = 5V$ 11.9 A	High Clamp Voltage at the COMP	Pin	V _{CCLPH}			2.0		V
POWER SWITCH High-side MOSFET On-Resistance $R_{DS(ON)}$ $V_{CC} = 5V$ 13 $mΩ$ Low-side MOSFET On-Resistance $V_{CC} = 5V$ 11 $mΩ$ CURRENT LIMIT Peak Switch Current Limit I_{LIM} $R_{ILIM} = 100kΩ$, $V_{CC} = 5V$ 11.9 A	Low Clamp Voltage at the COMP F	Pin	V _{CCLPL}			0.4		V
High-side MOSFET On-Resistance $R_{DS(ON)}$ V_{CC} = 5V	Error Amplifier Transconductance		G_{EA}	V _{COMP} = 1.2V		140		μA/V
Low-side MOSFET On-Resistance $V_{CC} = 5V$ 11 m Ω CURRENT LIMIT Peak Switch Current Limit I_{LIM} $R_{ILIM} = 100k\Omega$, $V_{CC} = 5V$ 11.9 A	POWER SWITCH							
Low-side MOSFET On-Resistance $V_{CC} = 5V$ 11 $mΩ$ CURRENT LIMIT Peak Switch Current Limit I_{LIM} $R_{ILIM} = 100kΩ$, $V_{CC} = 5V$ 11.9 A	High-side MOSFET On-Resistance)	D	V _{CC} = 5V		13		mΩ
Peak Switch Current Limit I_{LIM} $R_{ILIM} = 100k\Omega$, $V_{CC} = 5V$ 11.9 A	Low-side MOSFET On-Resistance	!	NDS(ON)	V _{CC} = 5V		11		mΩ
	CURRENT LIMIT							
Reference Voltage at the ILIM Pin V _{ILIM} 1.204 V	Peak Switch Current Limit		I _{LIM}	$R_{ILIM} = 100k\Omega, V_{CC} = 5V$		11.9		A
	Reference Voltage at the ILIM Pin		V _{ILIM}			1.204		V

ELECTRICAL CHARACTERISTICS

(Minimum and maximum values are at V_{IN} = 2.7V to 5.5V and Full = -40°C to +85°C. Typical values are at V_{IN} = 3.6V and T_A = +25°C. L = 1.2 μ H, C_{OUT} = 47 μ F, unless otherwise specified noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING FREQUENCY						
Switching Frequency	f _{SW}	$R_{FREQ} = 301k\Omega, V_{IN} = 3.6V, V_{OUT} = 12V$		500		kHz
Minimum On-Time	t _{ON_MIN}	$R_{FREQ} = 301k\Omega, V_{IN} = 3.6V, V_{OUT} = 12V$		120		ns
ROTECTION						
Output Over-Voltage Protection Threshold	V _{OVP}	V _{OUT} rising		13.2		V
Output Over-Voltage Protection Hysteresis	V _{OVP_HYS}	V _{OUT} falling below V _{OVP}		0.15		V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T _{SD}	T _A rising		155		°C
Thermal Shutdown Hysteresis	T _{SD_HYS}	T _A falling below T _{SD}		140		°C

TYPICAL APPLICATION

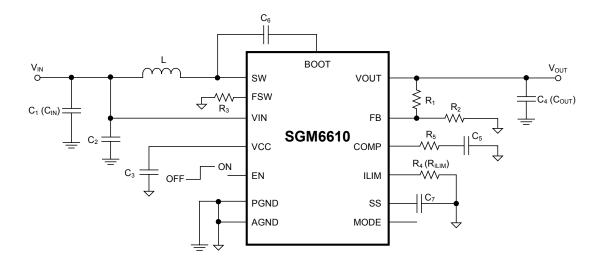


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

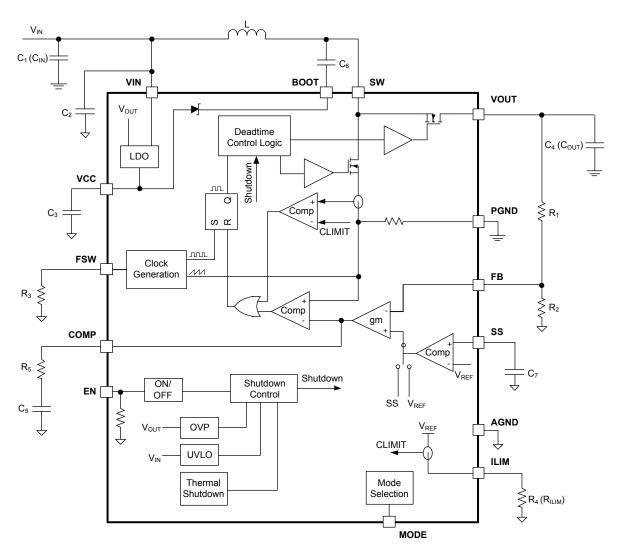


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM6610 is a fully-integrated synchronous boost converter with a $11m\Omega$ power switch and a $13m\Omega$ rectifier switch to output high power from a single cell or two-cell Lithium batteries. The device is capable of providing an output voltage of 12.6V and delivering up to 30W power from a single cell Lithium battery. The SGM6610 uses peak current control topology to regulate the output voltage. In moderate to heavy load condition, the SGM6610 works in the Pulse Width Modulation (PWM) mode. The switching frequency in the PWM mode is adjustable ranging from 200kHz to 2.2MHz by an external resistor. In light load condition, the device has two operation modes selected by the MODE pin. When the MODE pin is left floating, the SGM6610 works in the Pulse Frequency Modulation (PFM) mode. The PFM mode brings high efficiency at the light load. When the MODE pin is short to ground, the SGM6610 works in the forced PWM mode (FPWM). The FPWM mode can avoid the acoustic noise and other problems caused by the low switching frequency. The SGM6610 implements cycle-by-cycle current limit to protect the device from overload conditions during boost switching. The switch peak current limit is programmable by an external resistor. The SGM6610 uses external loop compensation, which provides flexibility to use different inductors and output capacitors. The peak current control scheme gives excellent transient line and load response with minimal output capacitance.

Enable and Startup

The SGM6610 has an adjustable soft-start function to prevent high inrush current during start-up. To minimize the inrush current during start-up, an external capacitor, connected to the SS pin and charged with a constant current, is used to slowly ramp up the internal positive input of the error amplifier. When the EN pin is pulled high, the soft-start capacitor $C_{\rm SS}$ (C_7 in the Figure 1) is charged with a constant current of 5µA typically. During this time, the SS pin voltage is compared with the internal reference (1.204V), the lower one is fed into the internal positive input of the error amplifier. The output of the error amplifier (which determines the inductor peak current value) ramps up slowly as the SS pin voltage goes up. The soft-start phase is completed after the SS pin voltage exceeds the internal reference

(1.204V). The larger the capacitance at the SS pin, the slower the ramp of the output voltage and the longer the soft-start time. A 47nF capacitor is usually sufficient for most applications. When the EN pin is pulled low, the voltage of the soft-start capacitor is discharged to ground.

Use Equation 1 to calculate the soft-start time.

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}}$$
 (1)

Where t_{SS} is the soft-start time, V_{REF} is the internal reference voltage of 1.204V, C_{SS} is the capacitance between the SS pin and ground. I_{SS} is the soft-start charging current of 5 μ A.

Under-Voltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The SGM6610 has both VIN UVLO function and VCC UVLO function. It disables the device from switching when the falling voltage at the VIN pin trips the UVLO threshold $V_{\text{IN_UVLO}}$, which is typically 2.4V. The device starts operating when the rising voltage at the VIN pin is 100mV above the $V_{\text{IN_UVLO}}$. It also disables the device when the falling voltage at the VCC pin trips the UVLO threshold $V_{\text{CC_UVLO}}$, which is typically 2.1V.

Adjustable Switching Frequency

This device features a wide adjustable switching frequency ranging from 200kHz to 2.2MHz. The switching frequency is set by a resistor connected between the FSW pin and the AGND pin of the SGM6610. A resistor must always be connected from the FSW pin to AGND pin for proper operation. The resistor value required for a desired frequency can be calculated using Equation 2.

$$R_{FREQ} = \frac{1}{C_{FREQ} \times f_{SW} - 0.0000002}$$
 (2)

Where R_{FREQ} is the resistance connected between the FSW pin and the AGND pin, C_{FREQ} = 6.3pF, f_{SW} is the desired switching frequency.

DETAILED DESCRIPTION (continued)

Adjustable Peak Current Limit

Equation 3 to calculate the resistor value:

To avoid an accidental large peak current, an internal cycle-by-cycle current limit is adopted. The low-side switch is turned off immediately as soon as the switch current touches the limit. The peak switch current limit can be set by a resistor at the ILIM pin to ground. The relationship between the current limit and the resistance depends on the status of the MODE pin. When the MODE pin is floating, namely the SGM6610 is set to work in the PFM mode at light load, use

$$I_{LIM} = \frac{1190000}{R_{ILIM}}$$
 (3)

Where R_{ILIM} (R_4) is the resistance between the ILIM pin and ground, I_{LIM} is the switch peak current limit.

When the resistor value is $100k\Omega$, the typical current limit is 11.9A.

Considering the device variation and the tolerance over temperature, the minimum current limit at the worst case can be 2A lower than the value calculated by above equations.

Over-Voltage Protection

If the output voltage at the VOUT pin is detected above 13.2V (typical value), the SGM6610 stops switching immediately until the voltage at the VOUT pin drops the hysteresis value lower than the output over-voltage protection threshold. This function prevents over-voltage on the output and secures the circuits connected to the output from excessive overvoltage.

Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of +155°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically +140°C, then the device starts switching again.

Device Functional Modes

The synchronous boost converter SGM6610 operates at a constant frequency Pulse Width Modulation (PWM) in moderate to heavy load condition. At the beginning of each switching cycle, the low-side N-MOSFET switch, shown in Figure 2, is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips, and it turns off the low-side N-MOSFET switch and the inductor current goes through the body diode of the high-side N-MOSFET in a dead-time duration. After the dead-time duration, the high-side N-MOSFET switch is turned on. Because the output voltage is higher than the input voltage, the inductor current decreases. The high-side switch is turned off until the next clock is reached. After a short dead-time duration, the low-side switch turns on again and the switching cycle is repeated.

In light load condition, the SGM6610 implements two operation modes, PFM mode and forced PWM mode, to meet different application requirements. The operation mode is set by the status of the MODE pin. When the MODE pin is connected to ground, the device works in the forced PWM mode. When the MODE pin is left floating, the device works in the PFM mode.

PWM Mode

In the forced PWM mode, the SGM6610 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor peak current down, delivering less power from input to output. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency will be low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency in light load condition.

DETAILED DESCRIPTION (continued)

PFM Mode

The SGM6610 improves the efficiency at light load with the PFM mode. When the converter operates in light load condition, the output of the internal error amplifier decreases to make the inductor peak current down, delivering less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. Once the current through the high side N-MOSFET is zero, the high-side MOSFET is turned off until the beginning of the next switching cycle. When the output of the error amplifier continuously goes down and reaches a threshold with respect to the peak current of $I_{\text{LIM}}/12$, the

output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the SGM6610 delivers, the output voltage increases above the nominal setting output voltage. The SGM6610 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 0.2% higher than the nominal setting voltage. With the PFM operation mode, the SGM6610 keeps the efficiency above 80% even when the load current decreases to 1mA. In addition, the output voltage ripple is much smaller at light load due to low peak current refer to Figure 3.

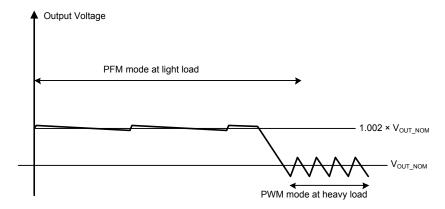


Figure 3. PFM Mode Diagram

APPLICATION INFORMATION

The SGM6610 is designed for outputting voltage up to 12.6V with 10A switch current capability to deliver more than 30W power. The SGM6610 operates at a constant frequency Pulse Width Modulation (PWM) in moderate to heavy load condition. In light load condition, the converter can either operate in the PFM mode or in the forced PWM mode according to the mode selection. The PFM mode brings high efficiency over entire load range, but the PWM mode can avoid the acoustic noise as the switching frequency is fixed. The converter uses the peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The SGM6610 can work with different inductor and output capacitor combination by external loop compensation. It also supports adjustable switching frequency ranging from 200kHz to 2.2MHz.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES						
Input Voltage Range	3.3V to 4.2V						
Output Voltage	9V						
Output Voltage Ripple	100mV peak to peak						
Output Current Rating	3A						
Operating Frequency	600kHz						
Operation Mode at Light Load	PFM						

Setting Switching Frequency

The switching frequency is set by a resistor connected between the FSW pin and the AGND pin of the SGM6610.

The resistor value required for a desired frequency can be calculated using Equation 4.

$$R_{FREQ} = \frac{1}{C_{FREQ} \times f_{SW} - 0.0000002}$$
 (4)

Where R_{FREQ} is the resistance connected between the FSW pin and the AGND pin, C_{FREQ} = 6.3pF, f_{SW} is the desired switching frequency.

Setting Peak Current Limit

The peak input current is set by selecting the correct external resistor value correlating to the required current limit. Because the SGM6610 is configured to work in the PFM mode in light load condition, use Equation 5 to calculate the correct resistor value:

$$I_{LIM} = \frac{1190000}{R_{ILIM}}$$
 (5)

Where R_{ILIM} (R_4) is the resistance between the ILIM pin and ground, I_{LIM} is the switch peak current limit.

For a typical current limit of 11.9A, the resistor value is $100k\Omega$. Considering the device variation and the tolerance over temperature, the minimum current limit at the worst case can be 2A lower than the value calculated by Equation 6. The minimum current limit must be higher than the required peak switch current at the lowest input voltage and the highest output power to make sure the SGM6610 does not hit the current limit and still can regulate the output voltage in these conditions.

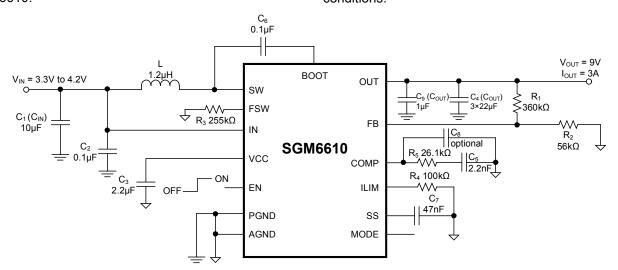


Figure 4. SGM6610 3.3V to 9V/3A Output Converter

Setting Output Voltage

The output voltage is set by an external resistor divider (R_1 , R_2 in the Figure 1). Typically, a minimum current of 20 μ A flowing through the feedback divider gives good accuracy and noise covering. A standard 56k Ω resistor is typically selected for low-side resister R_2 . The value of R_1 is then calculated as:

$$R_{1} = \frac{(V_{OUT} - V_{REF}) \times R_{2}}{V_{REF}}$$
 (6)

Inductor Selection

Because the selection of the inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The SGM6610 is designed to work with inductor values between $0.22\mu H$ and $4.7\mu H$. A $0.22\mu H$ inductor is typically available in a smaller or lower-profile package, while a $4.7\mu H$ inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a $4.7\mu H$ inductor can maximize the controller's output current capability.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0A current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 7 to Equation 9 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, SGMICRO recommends using the minimum switching frequency, the inductor value with -30% tolerance, and a

low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 7.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times n}$$
 (7)

Where V_{OUT} is the output voltage of the boost regulator, I_{OUT} is the output current of the boost regulator, V_{IN} is the input voltage of the boost regulator. η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in Equation 8.

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}}$$
 (8)

Where I_{PP} is the inductor peak-to-peak ripple, L is the inductor value, f_{SW} is the switching frequency, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Therefore, the peak current, I_{LPEAK} , seen by the inductor is calculated with Equation 9.

$$I_{LPEAK} = I_{DC} + \frac{I_{PP}}{2} \tag{9}$$

Set the current limit of the SGM6610 higher than the peak current I_{LPEAK} . Then select the inductor with saturation current higher than the setting current limit.

Boost converter efficiency is dependent on the resistance of its current path, the switching loss associated with the switching MOSFETs, and the inductor's core loss. The SGM6610 has optimized the internal switch resistance. However, the overall efficiency is affected significantly by the inductor's DC resistance (DCR), equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information.

Generally, SGMICRO would recommend an inductor with lower DCR and ESR. However, there is a tradeoff among the inductor's inductance, DCR and ESR resistance, and its footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors. Table 2 lists recommended inductors for the

SGM6610. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the Sumida's inductor CDMC8D28NP-1R2MC is selected for its small size and low DCR.

Table 2. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE MAX (L × W × H mm)	VENDOR
CDMC8D28NP-1R2MC	1.2	7.0	12.2 / 12.9	9.5 × 8.7 × 3.0	Sumida
744311150	1.5	7.2	14.0 / 11.0	7.3 × 7.2 × 4.0	Wurth
PIMB104T-2R2MS	2.2	7.0	18 / 12	11.2 × 10.3 × 4.0	Cyntec
PIMB103T-2R2MS	2.2	9.0	16 / 13	11.2 × 10.3 × 3.0	Cyntec
PIMB065T-2R2MS	2.2	12.5	12 / 10.5	7.4 × 6.8 × 5.0	Cyntec

Input Capacitor Selection

For good input voltage filtering, SGMICRO recommends low-ESR ceramic capacitors. The VIN pin is the power supply for the SGM6610. A 0.1 μ F ceramic bypass capacitor is recommended as close as possible to the VIN pin of the SGM6610. The VCC pin is the output of the internal LDO. A ceramic capacitor of more than 1 μ F is required at the VCC pin to get a stable operation of the LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasite inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100 mV. Generally, $10 \mu \text{F}$ input capacitance is sufficient for most applications.

NOTE

DC bias effect: high-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. The differences between the rated capacitor value and the effective capacitance result from package size and voltage rating in combination with material. A 10V rated 0805 capacitor with $10\mu F$ can have an effective capacitance of less $5\mu F$ at an output voltage of 5V.

Output Capacitor Selection

For small output voltage ripple, SGMICRO recommends a low-ESR output capacitor like a ceramic capacitor. Typically, three 22µF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient

response. Take care when evaluating a capacitor's derating under DC bias. The bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the following equations to calculate the minimum required effective caapctance C_{OUT} :

$$V_{RIPPLE_DIS} = \frac{(V_{OUT} - V_{IN_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}}$$
(10)

$$V_{RIPPLE ESR} = I_{LPEAK} \times R_{C ESR}$$
 (11)

Where $V_{\text{RIPPLE_DIS}}$ is output voltage ripple caused by charging and discharging of the output capacitor, $V_{\text{RIPPLE_ESR}}$ is output voltage ripple caused by ESR of the output capacitor, $V_{\text{IN_MIN}}$ is the minimum input voltage of boost converter, V_{OUT} is the output voltage, I_{OUT} is the output current, I_{LPEAK} is the peak current of the inductor, f_{SW} is the converter switching frequency, R_{C} ESR is the ESR of the output capacitors.

Loop Stability

The SGM6610 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network comprised of resister $R_{\rm 5},$ ceramic capacitors $C_{\rm 5}$ and $C_{\rm 8}$ is connected to the COMP pin.

The power stage small signal loop response of constant off time (COT) with peak current control can be modeled by Equation 12.

$$G_{PS}(S) = \frac{R_{o} \times (1-D)}{2 \times R_{SENSE}} \times \frac{(1 + \frac{S}{2 \times \pi \times f_{ESRZ}})(1 - \frac{S}{2 \times \pi \times f_{RHPZ}})}{1 + \frac{S}{2 \times \pi \times f_{D}}} \quad (12)$$

Where D is the switching duty cycle, R_O is the output load resistance, R_{SENSE} is the equivalent internal current sense resistor, which is 0.08Ω .

$$f_{p} = \frac{2}{2\pi \times R_{o} \times C_{out}}$$
 (13)

Where C_{OUT} is output capacitor.

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$
 (14)

Where R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_O \times (1-D)^2}{2\pi \times L} \tag{15}$$

The COMP pin is the output of the internal transconductance amplifier. Equation 16 shows the small signal transfer function of compensation network.

$$G_{c}(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{(1 + \frac{S}{2 \times \pi \times f_{COMZ}})}{(1 + \frac{S}{2 \times \pi \times f_{COMP1}})(1 + \frac{S}{2 \times \pi \times f_{COMP2}})}$$
 (16)

Where G_{EA} is the amplifier's transconductance, R_{EA} is the amplifier's output resistance, V_{REF} is the reference voltage at the FB pin, V_{OUT} is the output voltage, f_{COMP1} , f_{COMP2} are the poles' frequency of the compensation network, f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_{C} . The higher in frequency that the loop gain stays above zero before crossing over, the faster the

loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW} , or 1/5 of the RHPZ frequency, f_{RHPZ} .

Then set the value of R_5 , C_5 , and C_8 (in Figure 4) by following these equations:

$$R_{5} = \frac{2\pi \times V_{\text{OUT}} \times R_{\text{SENSE}} \times f_{\text{C}} \times C_{\text{OUT}}}{(1-D) \times V_{\text{RFF}} \times G_{\text{FA}}}$$
(17)

Where f_C is the selected crossover frequency.

The value of C₅ can be set by Equation 18.

$$C_{5} = \frac{R_{o} \times C_{OUT}}{2R_{5}}$$
 (18)

The value of C₈ can be set by Equation 19.

$$C_8 = \frac{R_{ESR} \times C_{OUT}}{R_5}$$
 (19)

If the calculated value of C_8 is less than 10pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

Table 3. Recommended L, $R_{\scriptscriptstyle 5}$ and $C_{\scriptscriptstyle 5}$ for Different Output Voltage and Frequency

f _{sw} (kHz)	V _{OUT} (V)	L (µH)	C₅ (nF)	R ₅ (kΩ)
600	12	1.2	2.2	30
600	9	1.2	2.2	26.1
600	5	0.68	4.7	13
2200	12	0.47	1	88.7
2200	9	0.47	1	66.5
2200	5	0.22	2.2	49.9
220	12	4.7	8.2	8.8
220	9	3.3	8.2	8.8
220	5	2.2	10	4.99

Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. A ground shielding line need to add between SW and

FSW paths to minimize the coupling.

The input capacitor needs to be close to the VIN pin and GND pin in order to reduce the I_{INPUT} supply ripple.

The layout should also be done with well consideration of the thermal as this is a high power density device. A thermal pad that improves the thermal capabilities of the package should be soldered to the large ground plate, using thermal vias underneath the thermal pad.

The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias.

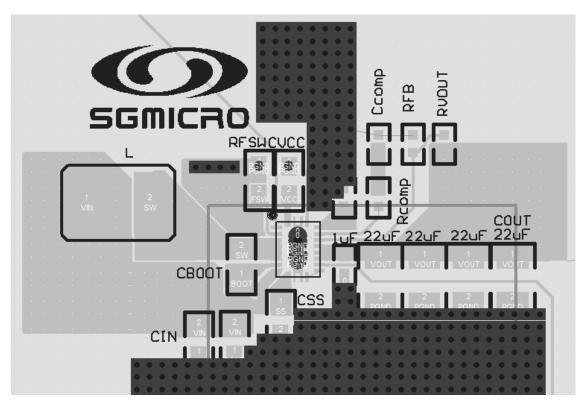
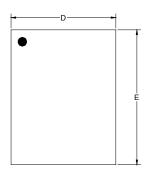
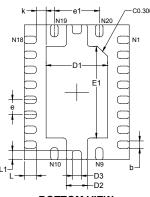


Figure 5. Bottom Layer

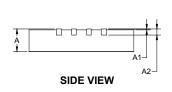
PACKAGE OUTLINE DIMENSIONS TQFN-4.5×3.5-20L

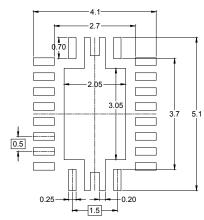


TOP VIEW



BOTTOM VIEW



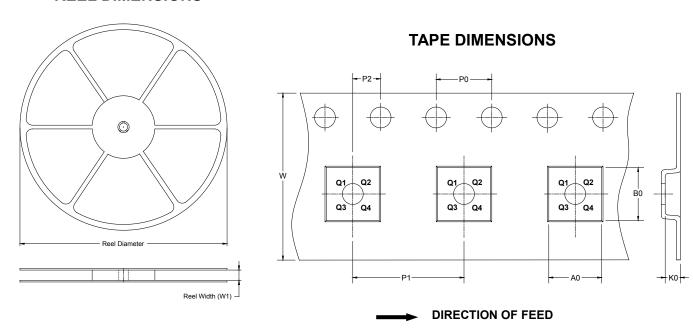


RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	_	nsions meters	Dimensions In Inches		
, , , , , , , , , , , , , , , , , , ,	MIN	MAX	MIN	MAX	
Α	0.700	0.800	0.028	0.031	
A1	0.000	0.050	0.000	0.002	
A2	0.203	REF	0.008	REF	
D	3.400	3.600	0.134	0.142	
D1	1.950	2.150	0.077	0.085	
D2	D2 0.650 0.850 D3 0.250 0.450 E 4.400 4.600	0.850	0.026	0.033	
D3		0.450	0.010 0.173	0.018	
E		4.400 4.600		0.181	
E1	2.950 3.150		0.116	0.124	
k	0.325	REF	0.013 REF		
b	0.200	0.300	0.008	0.012	
L	0.300	0.500	0.012	0.020	
L1	0.224	0.376	0.009	0.015	
е	0.500) BSC	0.020 BSC		
e1	1.500) BSC	0.060	BSC	

TAPE AND REEL INFORMATION

REEL DIMENSIONS

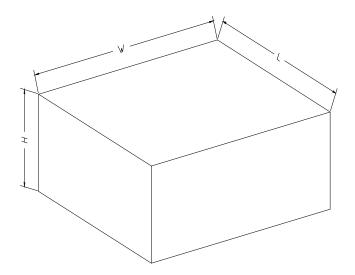


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4.5×3.5-20L	13"	12.4	3.75	4.75	0.95	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5