Data Sheet No. PD60177 Rev. F

IR4426/IR4427/IR4428(S)&(PbF)

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 to 20V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs (IR4426)
- Outputs in phase with inputs (IR4427)
- OutputA out of phase with inputA and OutputB in phase with inputB (IR4428)
- Also available LEAD-FREE

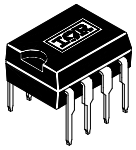
Descriptions

The IR4426/IR4427/IR4428 (S) is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

Product Summary

I_O+/-	1.5A / 1.5A
V_{OUT}	6V - 20V
$t_{on/off}$ (typ.)	85 & 65 ns

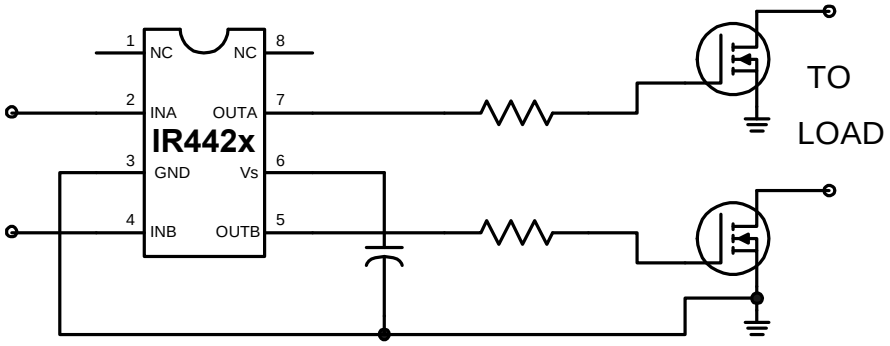
Packages



8 Lead PDIP

8 Lead SOIC

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	Fixed supply voltage		-0.3	25	V
V_O	Output voltage		-0.3	V_S + 0.3	
V_{IN}	Logic input voltage		-0.3	V_S + 0.3	
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V_S	Fixed supply voltage	6	20	V
V_O	Output voltage	0	V_S	
V_{IN}	Logic input voltage	0	V_S	
T_A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “0” input voltage (OUTA=LO, OUTB=LO) (IR4426) Logic “1” input voltage (OUTA=HI, OUTB=HI) (IR4427) Logic “0” input voltage (OUTA=LO), Logic “1” input voltage (OUTB=HI) (IR4428)	2.7	—	—	V	

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DC Electrical Characteristics cont.

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

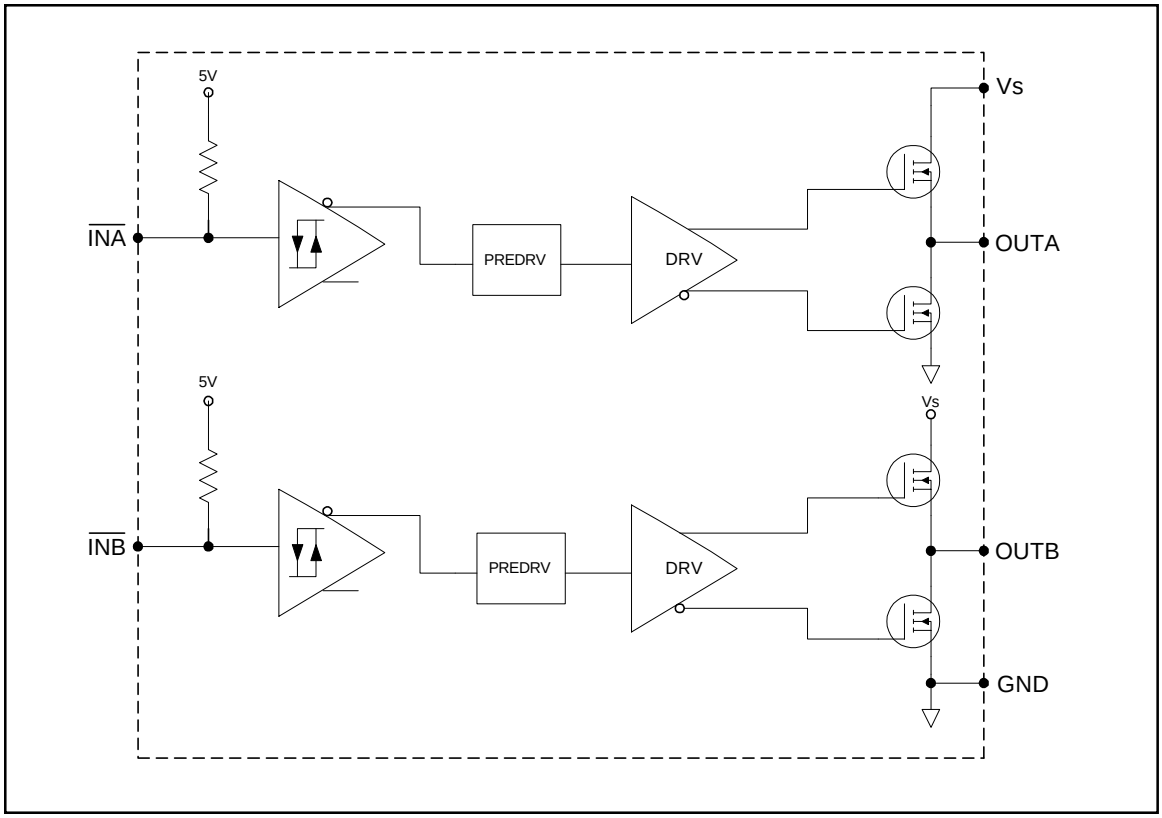
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4426) Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4427) Logic "I" input voltage (OUTA=HI), Logic "0" input voltage (OUTB=LO) (IR4428)	—	—	0.8	V	
V_{OH}	High level output voltage, V_{BIAS}-V_O	—	—	1.2		Io = 0mA
V_{OL}	Low level output voltage, V_O	—	—	0.1		Io = 0mA
I_{IN+}	Logic "1" input bias current (OUT=HI)	—	5	15	µA	V_{IN} = 0V (IR4426) V_{IN} = V_S (IR4427) V_{INA} = 0V (IR4428) V_{INB} = V_S (IR4428)
I_{IN-}	Logic "0" input bias current (OUT=LO)	—	-10	-30		V_{IN} = V_S (IR4426) V_{IN} = 0V (IR4427) V_{INA} = V_S (IR4428) V_{INB} = 0V (IR4428)
I_{QS}	Quiescent Vs supply current	—	100	200		V_{IN} = 0V or V_S
I_{O+}	Output high short circuit pulsed current	1.5	2.3	—	A	V_O = 0V, V_{IN} = 0 (IR4426) V_O = 0V, V_{IN} = V_S (IR4427) V_O = 0V, V_{INA} = 0 (IR4428) V_O = 0V, V_{INB} = V_S (IR4428) PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.5	3.3	—		V_O = 15V, V_{IN} = V_S (IR4426) V_O = 15V, V_{IN} = 0 (IR4427) V_O = 15V, V_{INA} = V_S (IR4428) V_O = 15V, V_{INB} = 0 (IR4428) PW ≤ 10 µs

AC Electrical Characteristics

V_{BIAS} (V_S) = 15V, CL = 1000pF, T_A = 25°C unless otherwise specified.

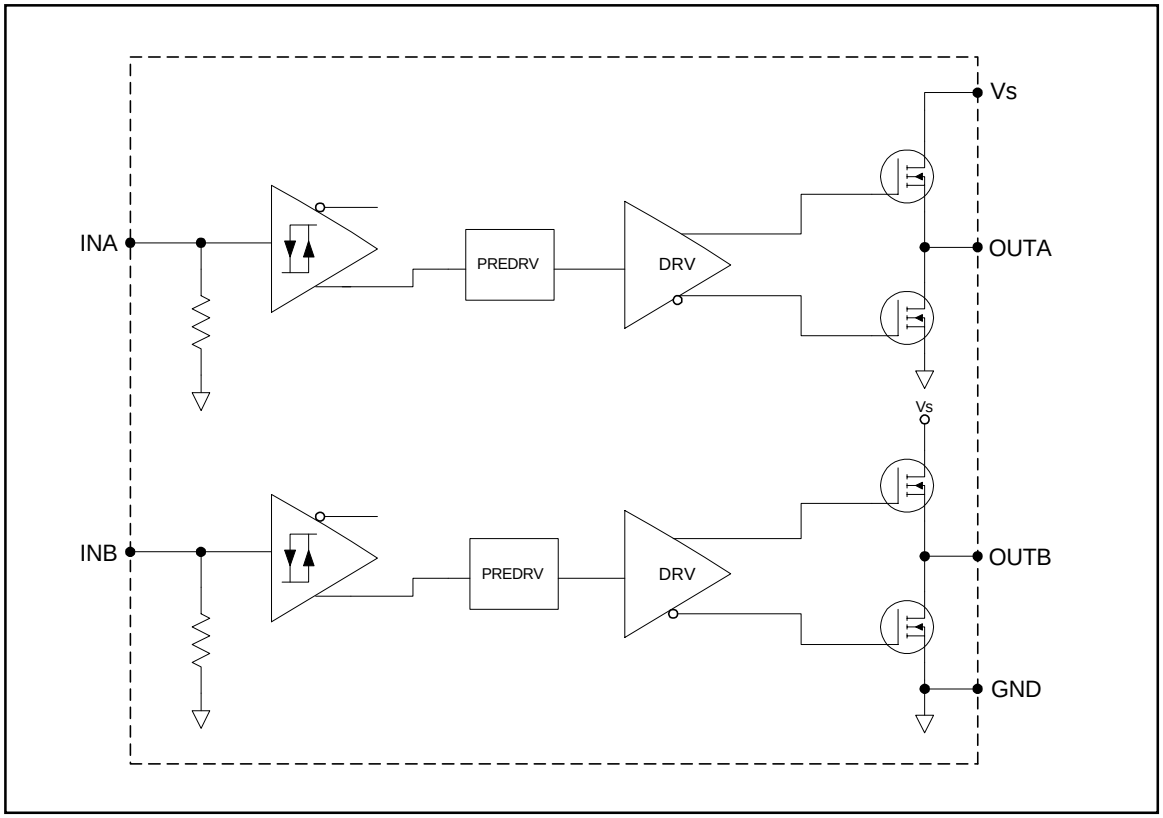
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
t_{d1}	Turn-on propagation delay	—	85	160	ns	figure 4
t_{d2}	Turn-off propagation delay	—	65	150		
t_r	Turn-on rise time	—	15	35		
t_f	Turn-off fall time	—	10	25		

Functional Block Diagram IR4426

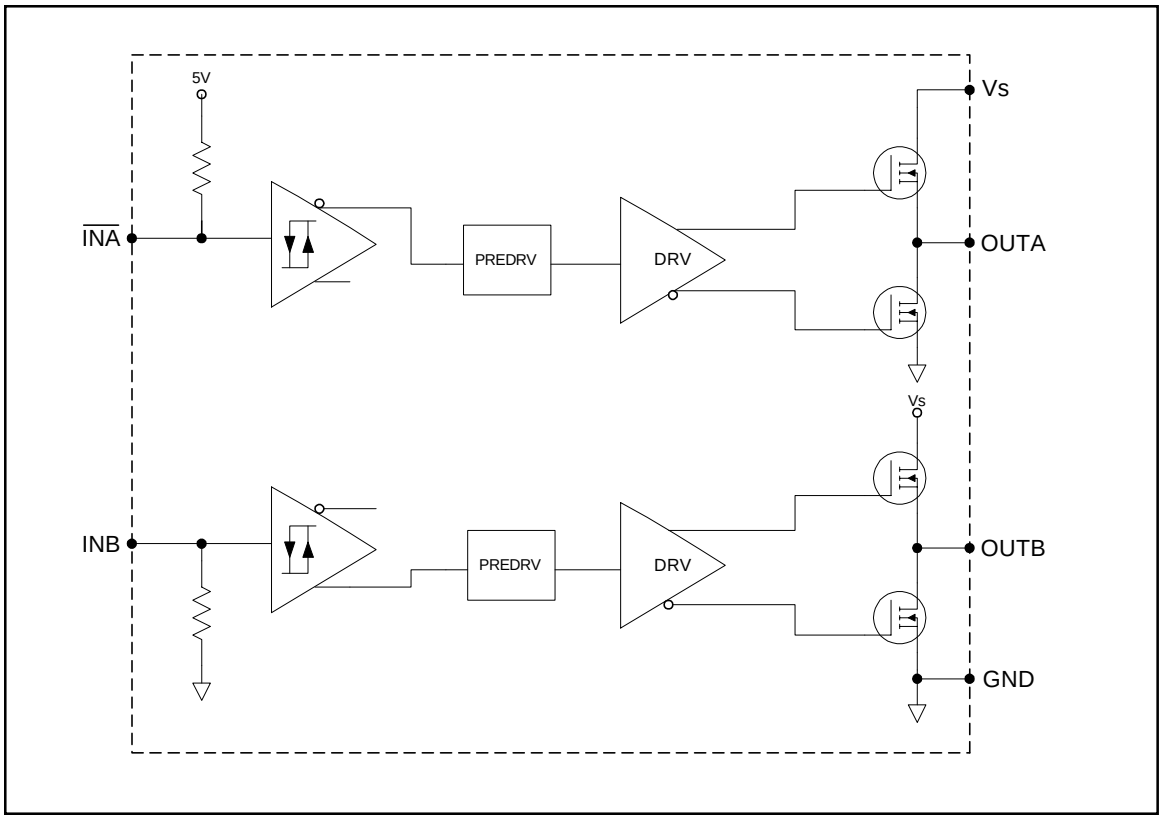


ADVANCE INFORMATION

Functional Block Diagram IR4427



Functional Block Diagram IR4428

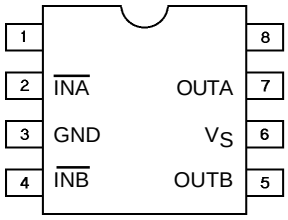
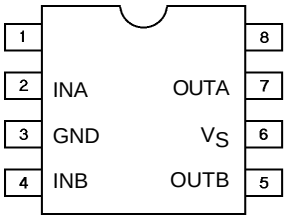
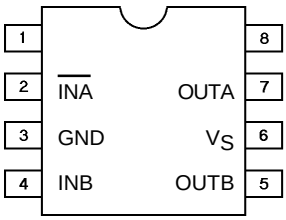


Lead Definitions

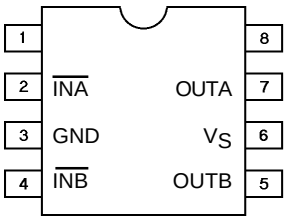
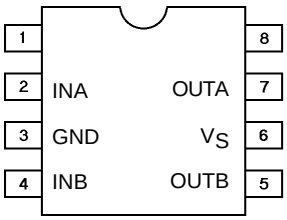
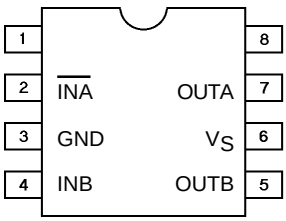
Symbol	Description
V_S	Supply voltage
GND	Ground
INA	Logic input for gate driver output (OUTA), out of phase (IR4426, IR4428), in phase (IR4427)
INB	Logic input for gate driver output (OUTB), out of phase (IR4426), in phase (IR4427, IR4428)
OUTA	Gate drive output A
OUTB	Gate drive output B

ADVANCE INFORMATION

Lead Assignments

 8 Lead PDIP	 8 Lead PDIP	 8 Lead PDIP
IR4426	**IR4427**	**IR4428**
Part Number		

Lead Assignments

 8 Lead SOIC	 8 Lead SOIC	 8 Lead SOIC
IR4426S	**IR4427S**	**IR4428S**
Part Number		

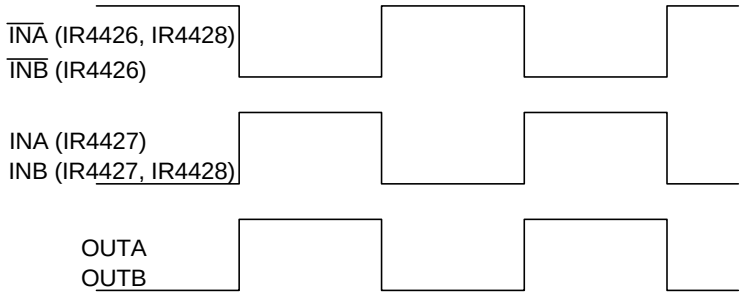


Figure 3. Timing Diagram

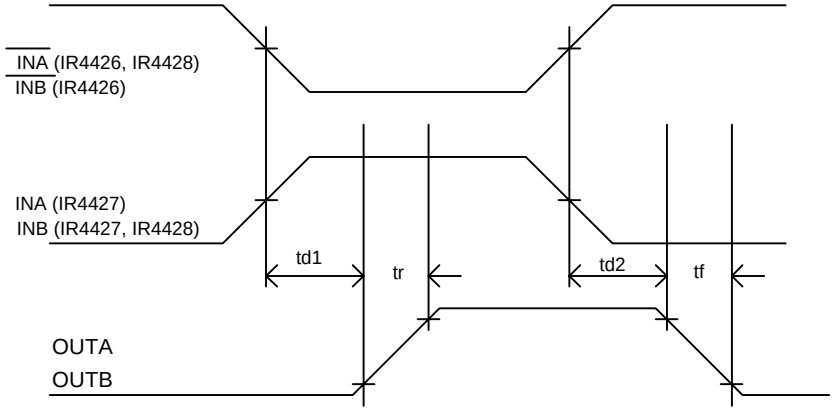


Figure 4. Switching Time Waveforms

ADVANCE INFORMATION

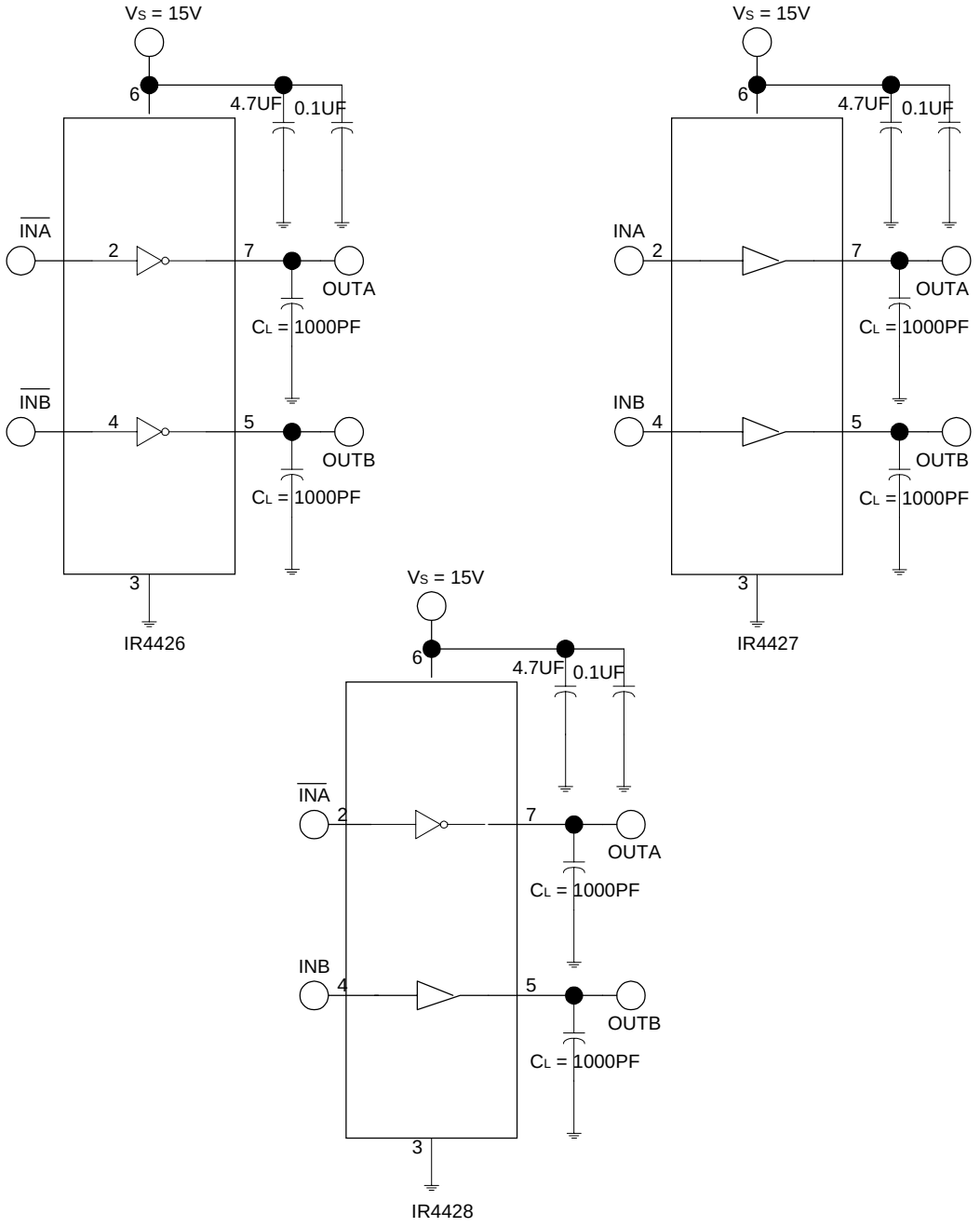
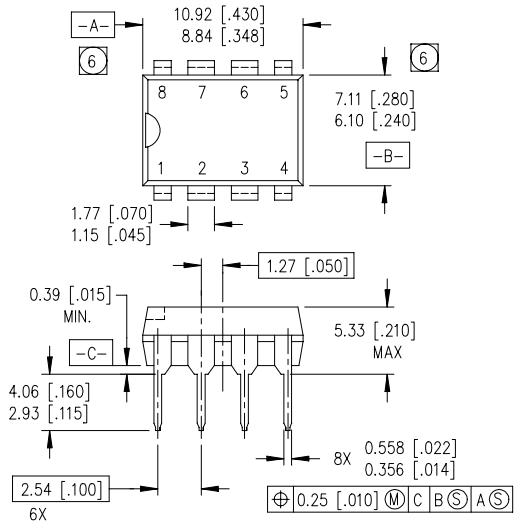


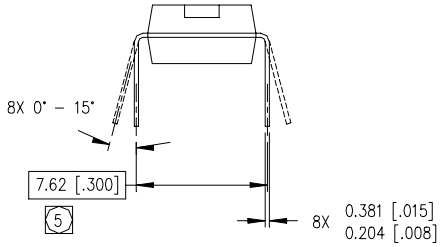
Figure 5. Switching Time Test Circuits

Caseoutline



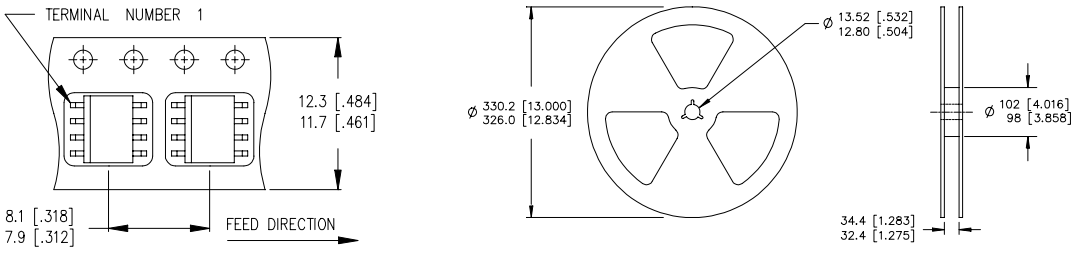
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP 01-3003 01

Tape & Reel

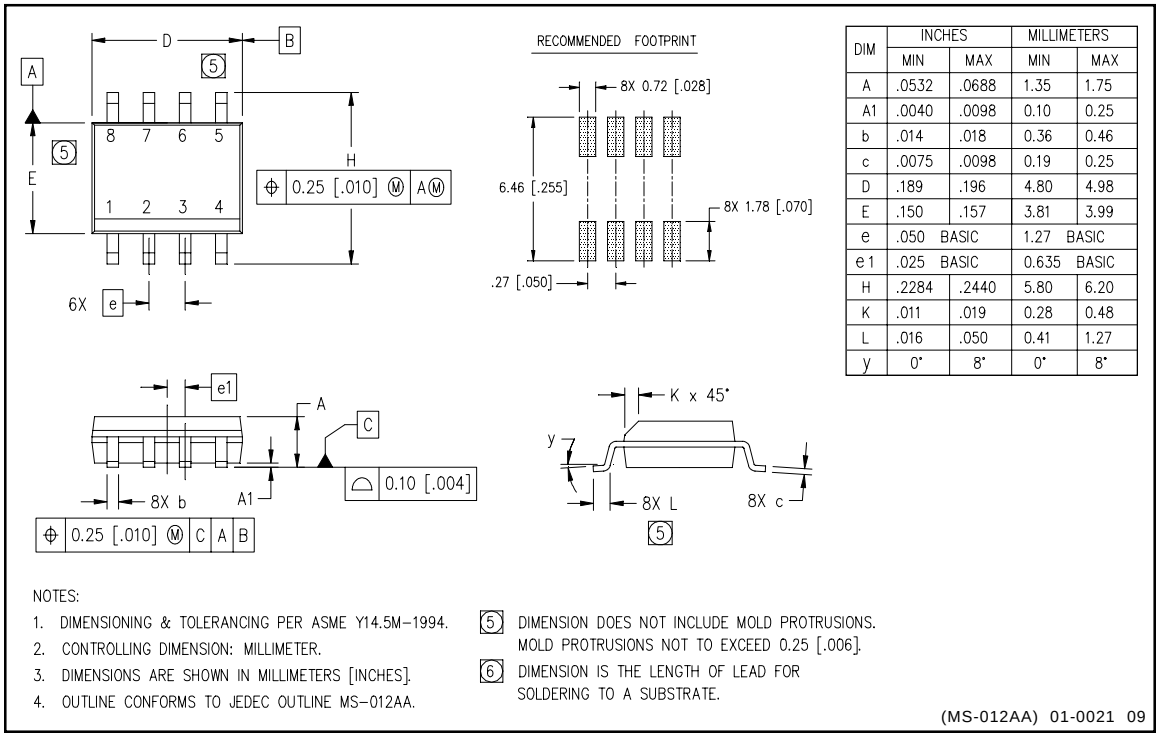


NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. OUTLINE CONFORMS TO EIA–481 & EIA–541.

ADVANCE INFORMATION

Case Outline - 8 Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

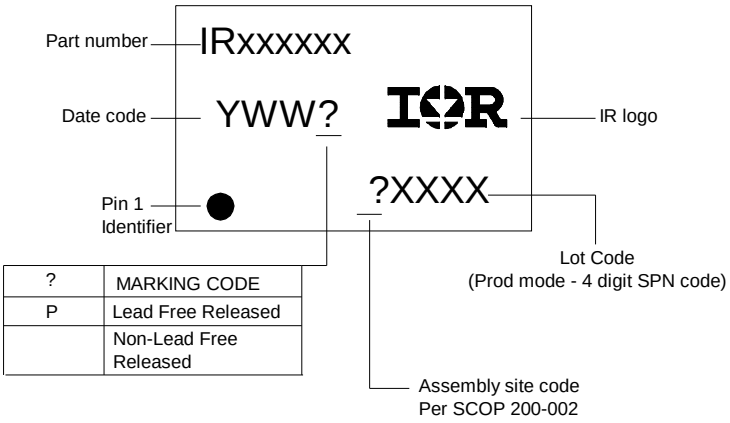
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(MS-012AA) 01-0021 09

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR4426 order IR4426
8-Lead SOIC IR4426S order IR4426S
8-Lead PDIP IR4427 order IR4427
8-Lead SOIC IR4427S order IR4427S
8-Lead PDIP IR4428 order IR4428
8-Lead SOIC IR4428S order IR4428S

Leadfree Part

8-Lead PDIP IR4426 order IR4426PbF
8-Lead SOIC IR4426S order IR4426SPbF
8-Lead PDIP IR4427 order IR4427PbF
8-Lead SOIC IR4427S order IR4427SPbF
8-Lead PDIP IR4428 order IR4428PbF
8-Lead SOIC IR4428S order IR4428SPbF