SGM61040
4A High Efficiency Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61040 is a high efficiency and miniature size synchronous Buck converter for low input voltage applications. This high frequency device does not need external compensation and is a perfect solution for compact designs. The 2.5V to 5.5V input voltage range is suitable for almost all available battery chemistries. For the SGM61040A version, to keep the high efficiency in the whole load range, the device operates in pulse width modulation (PWM) mode at normal load and automatically enters the power-save mode (PSM) at light loads.

This device is based on an adaptive off-time architecture, but still allows a wide range of output capacitors from 22μF to 150μF and even more. This flexibility makes the device a good choice for system power rails supplies. The adaptive off-time architecture provides excellent output voltage accuracy and superb load transient response.

The SGM61040 is available in a Green TDFN-2×2-7L package.

FEATURES

- **2.5V to 5.5V Input Voltage Range**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Adaptive Off-Time Architecture**
- **Up to 95% Efficiency**
- **Low R_{DSON} MOSFET Switches (27mΩ/12mΩ)**
- **42μA (TYP) Operating Quiescent Current**
- **Ultra-Low Quiescent Current in Shutdown Mode**
- **Power-Save Mode at Light Loads (SGM61040A)**
- **100% Duty Cycle Capability for Low Dropout**
- **Startup with Pre-biased Output**
- **Output Discharge Function**
- **Power Good Output**
- **Hiccup Mode Short-Circuit Protection**
- **Thermal Shutdown Protection**
- **Available in a Green TDFN-2×2-7L Package**

APPLICATIONS

Battery-Powered Applications
Point-of-Load
Processor Power Supplies
Hard Disk Drives (HDD)/Solid State Drives (SSD)

TYPICAL APPLICATION

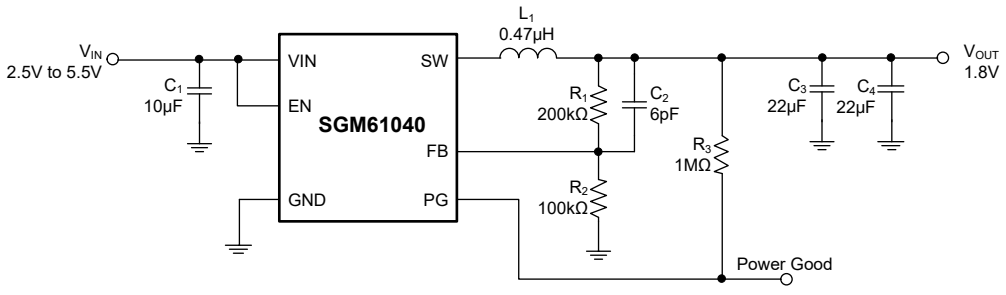


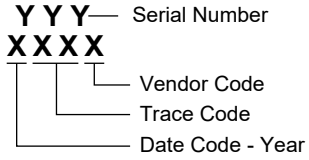
Figure 1. SGM61040 Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61040A	TDFN-2×2-7L	-40℃ to +125℃	SGM61040AXTEP7G/TR	GAM XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Pin Voltages Referred to GND
VIN, FB, EN, PG ..... -0.3V to 6V
SW (DC) ..... -0.3V to V_{IN} + 0.3V
SW (AC, Less than 10ns) while Switching ..... -3V to 9V
Package Thermal Resistance
TDFN-2×2-7L, θ_{JA} ..... 109℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.5V to 5.5V
Output Voltage Range, V_{OUT} ..... 0.6V to V_{IN}
PG Pin Sink Current, I_{SINK_PG} 1mA
Maximum Pull-Up Voltage for PG, V_{PG} 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

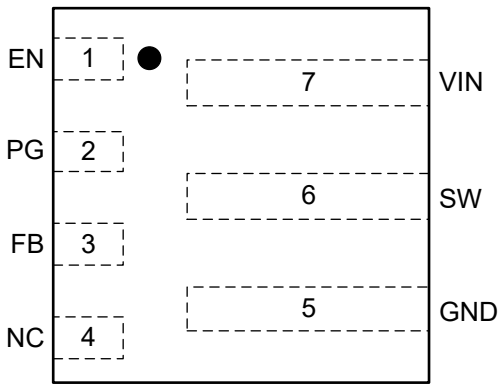
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-7L

PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
1	EN	I	Active High Device Enable Input Pin. Pull this pin to logic high to enable the device and pull it low to disable it. An internal 550kΩ (TYP) pull-down resistor disables the device by default. This resistor is removed when the device is enabled.
2	PG	O	Open-Drain Power Good Output Pin. This output is released to go high if the device is in power good status. Pull up this pin to a 5.5V or less voltage rail. It can be left open if not used.
3	FB	I	Feedback Pin. Connect a resistor divider between the output voltage sense point and ground and tap it to the FB pin to set the output voltage.
4	NC	—	No Connection. The pin can be connected to the ground or leave it floating.
5	GND	G	Ground Pin.
6	SW	P	Switch Node of the Power Converter. Connect it to the output inductor.
7	VIN	P	Input Voltage Pin.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Input Voltage Range	V_{IN}		2.5		5.5	V
Quiescent Current into VIN	I_Q	Enabled, no load, no switching (SGM61040A)		42		μA
Shutdown Current into VIN	I_{SD}	Disabled (EN = Low)		0.05		μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling		2.2		V
Under-Voltage Lockout Hysteresis		V_{IN} rising		200		mV
Thermal Shutdown Threshold	T_{JSD}	T_J rising		160		℃
Thermal Shutdown Hysteresis		T_J falling		25		℃
EN Input						
Logic High Input Voltage	V_{IH}	V_{IN} = 5V		0.98		V
Logic Low Input Voltage	V_{IL}	V_{IN} = 5V		0.86		V
Input Leakage Current (into EN Pin)	I_{EN_LKG}	EN = High		0.01		μA
Pull-Down Resistance at EN Pin	R_{PD}	EN = Low		550		kΩ
Soft-Start, Power Good						
Soft-Start Time	t_{SS}	Measure from EN high to 95% × V_{OUT} (set)		0.8		ms
Power Good Threshold	V_{PG}	V_{OUT} rising		95% × V_{OUT} (set)		V
		V_{OUT} falling		90% × V_{OUT} (set)		
PG Low State Output Voltage	V_{PG_OL}	I_{SINK} = 1mA		0.13		V
PG Leakage Current (into PG Pin)	I_{PG_LKG}	V_{PG} = 5V		0.01		μA
Output and Feedback						
Feedback Regulation Voltage	V_{FB}	PWM mode, 2.5V ≤ V_{IN} ≤ 5.5V, T_J = 0℃ to +85℃		0.6		V
Feedback Input Leakage Current	I_{FB_LKG}	V_{FB} = 1V		0.01		μA
Output Discharge Resistor	R_{DIS}	EN = Low, V_{OUT} = 1.8V		43		Ω
Power Switches						
High-side MOSFET On-Resistance	R_{DSON}	I_{SW} = 500mA		27		mΩ
Low-side MOSFET On-Resistance		I_{SW} = 500mA		12		mΩ
High-side MOSFET Current Limit	I_{LIM}			5.6		A
PWM Switching Frequency	f_{SW}	I_{OUT} = 1A (SGM61040A)		2.5		MHz

FUNCTIONAL BLOCK DIAGRAM

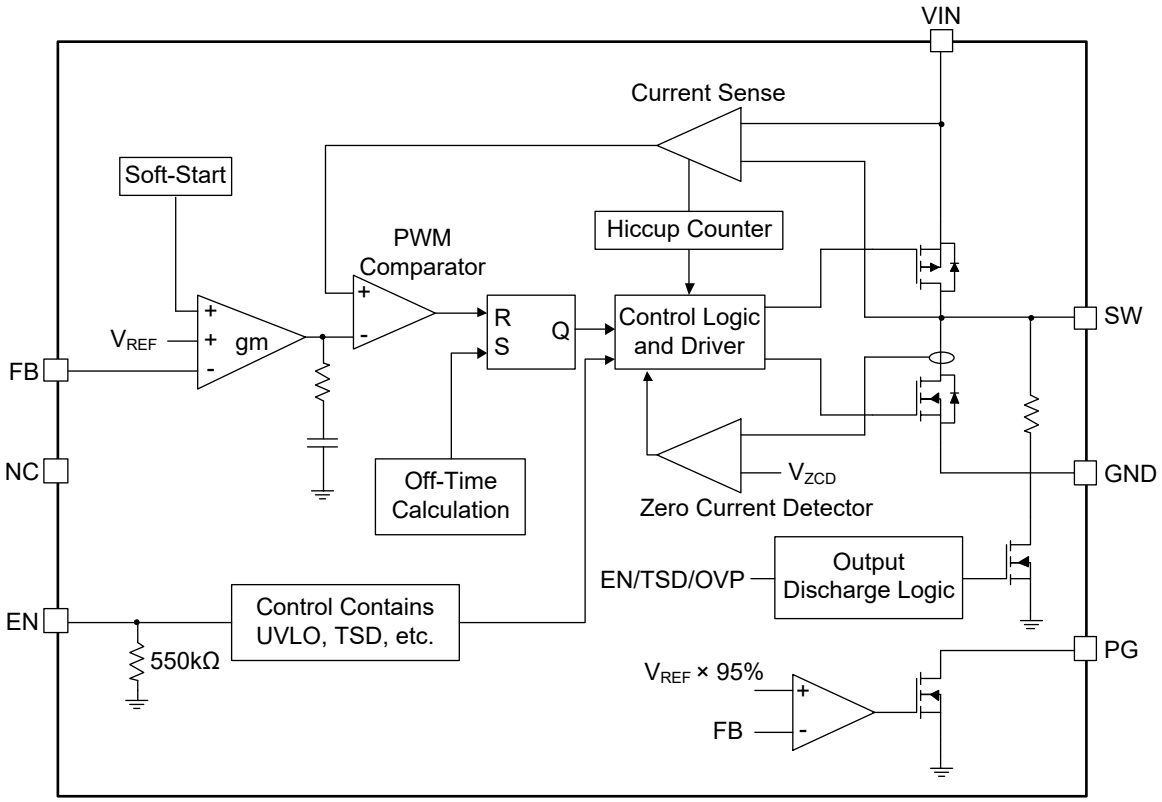


Figure 2. SGM61040 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61040 is a high efficiency Buck switching converter optimized for handheld battery-powered applications. It operates at a quasi-fixed frequency of 2.5MHz and uses adaptive off-time PWM control for the moderate to heavy load range. This allows using a small inductor and small capacitors for compact designs. At light load conditions, SGM61040A operates in power-save mode to reduce the switching frequency and losses for longer battery life. The power-save mode quiescent current is 42μA (TYP) while the shutdown current is only 0.05μA (TYP).

Under-Voltage Lockout (UVLO)

Operating with insufficient supply voltage can cause device malfunction or failure. The UVLO protection shuts down the device if the input voltage is below the V_{UVLO} threshold. The UVLO comparator has a 200mV hysteresis band.

Device Enable and Disable

When the input voltage is valid, pulling the EN input to logic high will enable the device and pulling it low will shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.05μA (TYP). A 550kΩ pull-down resistor is internally placed between EN and GND when the device is disabled.

During shutdown, an internal 42Ω resistor connects SW and GND and softly discharges the output capacitors. This discharge function is also activated when the shutdown is caused by a thermal shutdown, UVLO, or short-circuit protection.

Power Good Output (PG)

PG is an open-drain output with 1mA sinking capability. This pin should be pulled up with an external resistor to a logic high rail no more than 5.5V unless it is not used. The PG signal is in high-impedance state when the output voltage is in regulation range. PG remains low until V_{OUT} exceeds 95% of its nominal (set) value and goes low if V_{OUT} drops below 90% of its nominal value. Table 1 shows how the PG state is changed in different conditions. V_{PG} is the threshold of the PG hysteretic comparator. It has a 5% hysteresis band and goes high when V_{FB} rises above 95% of the V_{REF}.

The PG output is useful for power supply sequencing as well. Usually, the multiple power rails of a system need to be powered in a specific sequence for proper startup. The PG output of the leading power supply is connected to the EN input of the subsequent power supply to implement such sequencing.

Table 1. PG Output State in Different Conditions

Reason	Condition(s)	PG State	
		High Z	Low
Output Voltage	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown by EN	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.6V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 0.6V$	√	

Soft-Start and Pre-biased Output

An 800μs internal soft-start circuit is designed to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage (V_{REF} = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61040 is also capable of starting with a pre-biased output capacitor when it is powering up or enabled. When the device is turning on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device may not be able to start up properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

DETAILED DESCRIPTION (continued)

Power-Save Mode

At light load conditions, the SGM61040A shifts to the power-save mode to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in power-save mode. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Low Dropout Operation (100% Duty Cycle)

When the input voltage reduces, the on-time increases. When the input voltage is lower than the regulation output voltage, the output voltage drops, and the SGM61040 goes into 100% duty cycle mode. The high-side switch is always turned on, and the output voltage is determined by the load current times the R_{DSON} composed by the high-side switch and inductor.

Current Limit and Hiccup Mode Short-Circuit Protection

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM} threshold, HS switch is turned off and the low-side (LS) switch will be turned on to reduce the inductor current and limit the peak.

If 2ms consecutive repetition of this event occurs, the controller will stop switching and turns the output discharge circuit on. Then a new startup will be automatically initiated (hiccup) after 2.5ms (TYP). The hiccup repeats until the overload or short-circuit fault is cleared.

Thermal Shutdown

Thermal protection is designed to protect the die against overheating damage. If the junction temperature exceeds T_{JSD} threshold, the switching stops and the device shuts down. Automatic recovery with a soft-start will begin when the junction temperature drops below the 135℃ falling threshold.

APPLICATION INFORMATION

In this section, power supply design with the SGM61040 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

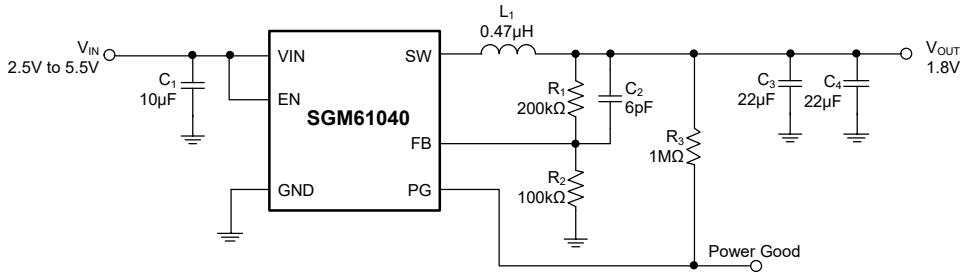


Figure 3. SGM61040 Circuit for 1.8V Output

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.5V to 5.5V
Output Voltage	1.8V
Output Current	≤ 4A
Output Ripple Voltage	< 30mV

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1	10μF, 10V, X7R, 0805, Ceramic P/N: GRM21BR71A106KA73L	Murata
C_2	6pF, 50V, C0G, 0603, Ceramic	Standard
C_3, C_4	22μF, 10V, X5R, 0805, Ceramic P/N: GRM21BR61A226ME44L	Murata
L_1	0.47μH Wire Wound, DCR_{MAX} = 22mΩ, $I_{SAT(30\%)}$ = 15.5A, $I_{RMS(40℃)}$ = 7.4A, SRF = 72MHz, 4mm × 4mm × 2mm, P/N: WPN4020HR47MT	Sunlord
R_1	Value Depends on V_{OUT}, 200kΩ, 1%, 0603, 1/16W Chip Resistor	Standard
R_2	100kΩ, 1%, 0603, 1/16W Chip Resistor	Standard
R_3	1MΩ, 5%, 0603, 1/16W Chip Resistor	Standard

Input Capacitor Selection (C_{IN})

High frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 10μF ceramic capacitor with X5R or better dielectric and 0805 or smaller size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

Inductor Selection (L)

The important factors for inductor selection are inductance (L), saturation current (I_{SAT}), RMS rating (I_{RMS}), DC resistance (DCR) and dimensions. Use Equation 1 to find the inductor peak current (I_{L_MAX}) and peak-to-peak ripple current (ΔI_L) in static conditions:

$$I_{L\_MAX} = I_{O\_MAX} + \frac{\Delta I_L}{2}$$
$$\Delta I_L = V_{OUT} \times \frac{1-D}{L \times f_{SW}} \quad (1)$$

I_{O_MAX} is the maximum load current, $D = V_{OUT}/V_{IN}$ represents duty cycle and f_{SW} is the switching frequency.

I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Typically, the saturation current above high-side current limit is enough, and a 10% to 30% ripple current is selected to calculate the inductance. Larger inductance values reduce the ripple current but lead to sluggish transient response.

Output Capacitor Selection (C_{OUT})

This device is capable to operate with low ESR ceramic capacitors to get low voltage ripple and fast response. Two 22μF capacitors with X7R or X5R dielectric type are recommended. If an output capacitor larger than 150μF is used, appropriate startup current reduction should be considered to avoid current limiting or false triggering of the short-circuit protection during startup.

Output Voltage Setting

Use Equation 2 to select the R_1/R_2 resistor divider to set the V_{OUT}. Select the R_2 value less than 100kΩ to compromise noise sensitivity and light load losses.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

APPLICATION INFORMATION (continued)

Output Filter Design

Table 4 can be used to select the proper LC filter components for most design requirements. The inductor initial tolerance can be as high as -30% to +20% of the nominal value and proper current derating is usually required. Bias voltage may cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value.

L_1 = 0.47μH, C_{OUT} = 22μF × 2 and C_2 = 6pF are the recommended values for the typical application.

Table 4. Proper Output Capacitor and Inductor Combination

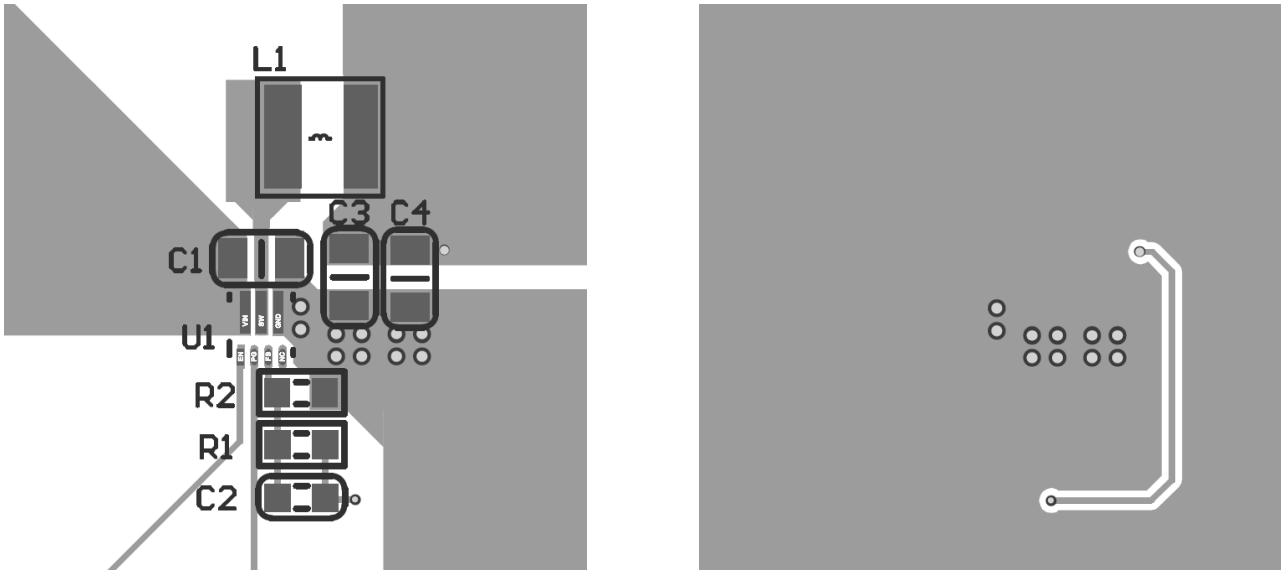
L_1	C_{OUT}	C_2
0.47μH	22μF × 2	6pF
	47μF	6pF
	100μF	—
	150μF	—
1μH	22μF × 2	6pF
	47μF	6pF
	100μF	—
	150μF	—
2.2μH	—	—

Layout Guidelines

A good printed-circuit-board (PCB) layout is a critical element of any high performance design. Follow the guidelines below for designing a good layout for the SGM61040.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device GND pin to minimize the AC current loops. Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep the signal traces like the FB sense line away from SW or other noisy sources.
- Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.

Refer to Figure 4 for a recommended PCB layout.

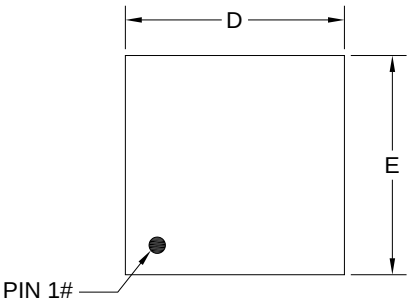


Top Layer Bottom Layer

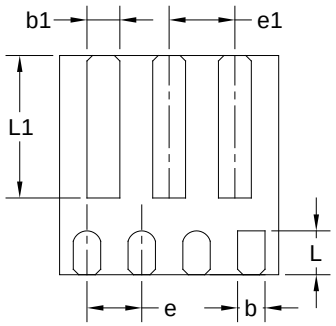
Figure 4. PCB Layout

PACKAGE OUTLINE DIMENSIONS

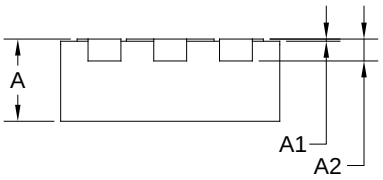
TDFN-2×2-7L



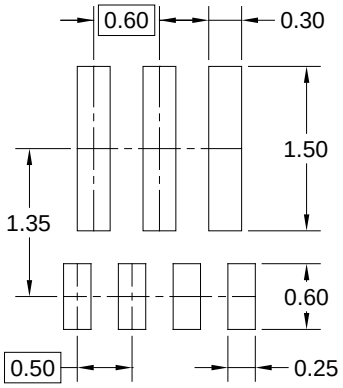
TOP VIEW



BOTTOM VIEW



SIDE VIEW



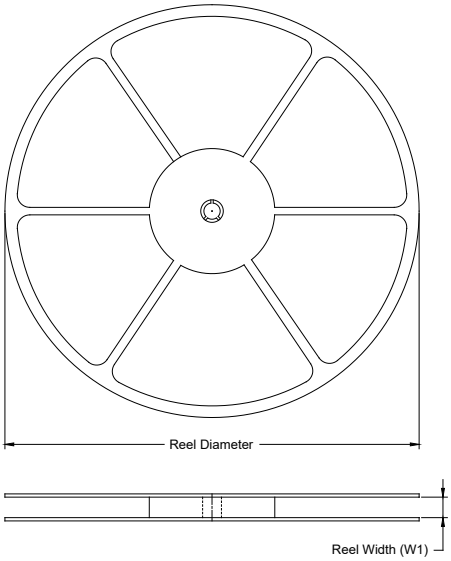
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.200 REF		
b	0.200	0.250	0.300
b1	0.250	0.300	0.350
D	1.900	2.000	2.100
E	1.900	2.000	2.100
e	0.500 BSC		
e1	0.600 BSC		
L	0.300	0.400	0.500
L1	1.200	1.300	1.400

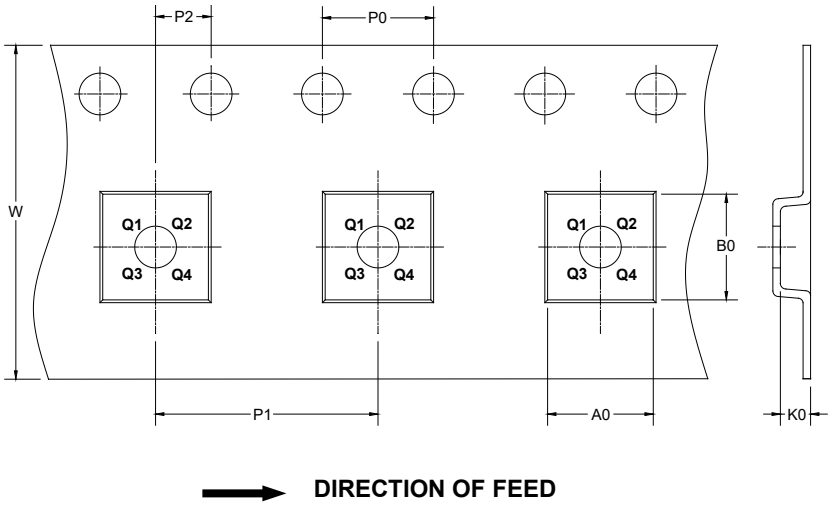
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



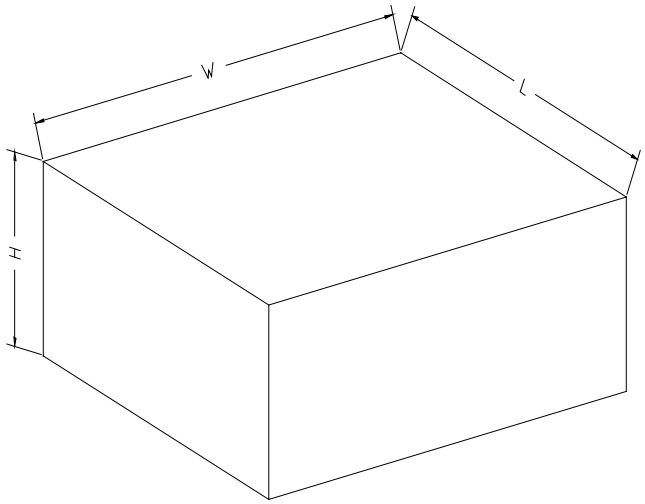
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-7L	7″	9.5	2.30	2.30	1.00	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002