TPS25940x 2.7 – 18V eFuse with True Reverse Blocking and DevSleep Support for SSDs

1 Features

- 2.7 V – 18 V Operating Voltage, 20 V (Max)
- 42 mΩ R_{ON} (Typical)
- 0.6 A to 5.3 A Adjustable Current Limit (±8%)
- IMON Current Indicator Output (±8%)
- 200 µA Operating I_Q (Typical)
- 95 µA DevSleep Mode I_Q (Typical)
- 15 µA Disabled I_Q (Typical)
- ±2% Overvoltage, Undervoltage Threshold
- Reverse Current Blocking
- 1 µs Reverse Voltage Shutoff
- Programmable dV_o/dt Control
- Power Good and Fault Outputs
- -40°C to 125°C Junction Temperature Range
- UL 2367 Recognized
  - File No. 169910
  - R_{ILIM} ≥ 20 kΩ (4.81 A max)
- UL60950 - Safe during Single Point Failure Test
  - Open/Short ILIM detection

2 Applications

- PCIe/SATA/SAS HDD and SSD Drives
- Enterprise and Micro Servers
- Smart Load Switch
- Set-Top-Box (STB), DTVs and Game Consoles
- RAID Cards - Holdup Power Management
- Telecom Switches and Routers
- Adapter Powered Devices

3 Description

The TPS25940 eFuse Power Switch is a compact, feature rich power management device with a full suite of protection functions, including a low power DevSleep™ mode that supports compliance with the SATA™ Device Sleep standard. The wide operating range allows control of many popular DC bus voltages. Integrated back to back FETs provide bidirectional current control making the device well suited for systems with load side holdup energy that must not drain back to a failed supply bus.

Load, source and device protection are provided with many programmable features including overcurrent, dV_o/dt ramp and overvoltage, undervoltage thresholds. For system status monitoring and downstream load control, the device provides PGOOD, $\overline{FLT}$ and precise current monitor output. Precise programmable undervoltage, overvoltage thresholds and the low I_Q DevSleep mode simplify SSD power management design.

The TPS25940 monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse current blocking when $V_{(IN)} < (V_{(OUT)} - 10$ mV). This function supports swift changeover to a boosted voltage energy storage element in systems where backup voltage is greater than bus voltage.

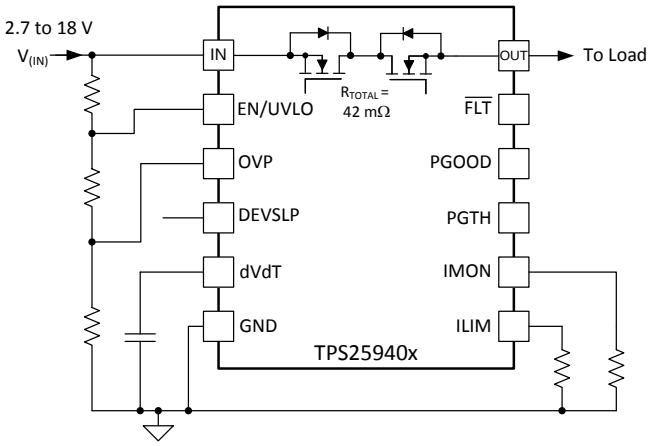
Device Information[1]

PART NUMBER[2]	PACKAGE	BODY SIZE (NOM)
TPS25940A	WQFN (20)	3.00 mm x 4.00 mm
TPS25940L		

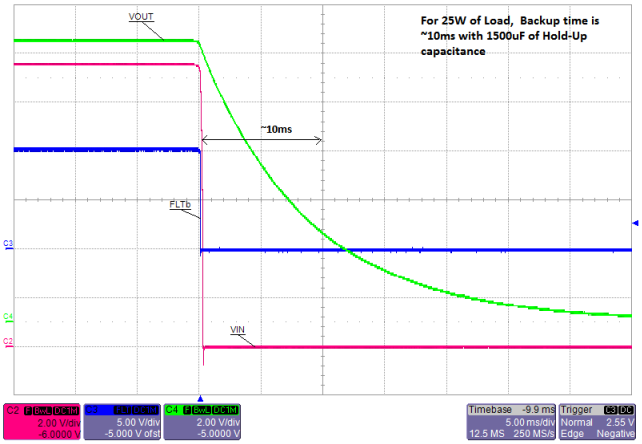
(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) TPS25940L = Latched, TPS25940A = Auto Retry

4 Simplified Schematic



Power Fail Detection and Blocking



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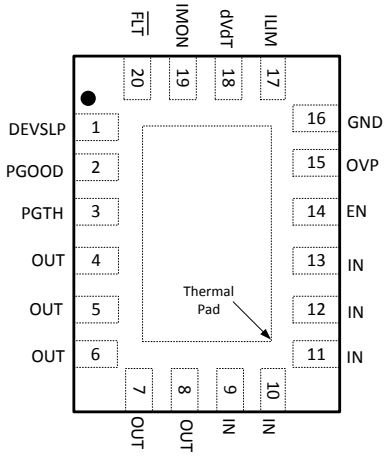
5 Revision History

Changes from Original (June 2014) to Revision A **Page**

- Changed *Features* From: UL2367 Recognition Pending To: UL 2367 Recognized, R_{ILIM} ≥ 20 kΩ (4.81 A max), File No. 169910 ... 1
- Moved the Storage Temperature From the *Handling Ratings* table To *Absolute Maximum Ratings* table ... 4
- Changed the *Handling Ratings* table To: *ESD Ratings* table ... 4
- Added Test Condition to $I_{(LIM)}$: "$R_{(ILIM)}$ = 20 kΩ" in the *Electrical Characteristics* ... 5
- Changed Figure 24. ... 10
- Added condition $R_{(ILIM)}$ = 17.8 kΩ to Figure 40 and Figure 41 ... 13
- Changed Figure 43 ... 17
- Changed Equation 6 to include $I_{(IMON\_OS)}$ ... 21
- Added the NOTE to *Application and Implementation* ... 24
- Added Note to Figure 57 ... 28
- Changed Equation 35 From: $V_{(IN)}$ x $I_{(LOAD)}$ To: $V_{(IN)}$ + $I_{(LOAD)}$ ... 35

6 Pin Configuration and Functions

TPS25940
RVC PACKAGE
(TOP VIEW)



Pin Functions

NAME	NO.	I/O	DESCRIPTION
DEVSLP	1	I	Active High. DevSleep Mode control. A high at this pin will activate the DevSleep mode(Low Power Mode).
PGOOD	2	O	Active High. A high indicates PGTH has crossed the threshold value. It is an open drain output.
PGTH	3	I	Positive input of PGOOD comparator.
OUT	4 - 8	O	Power Output of the device.
IN	9 - 13	I	Power Input and supply voltage of the device.
EN/UVLO	14	I	Input for setting programmable undervoltage lockout threshold. An undervoltage event will open internal FET and assert $\overline{FLT}$ to indicate power-failure. When pulled to GND, resets the fault latch in TPS25940L.
OVP	15	I	Input for setting programmable overvoltage protection threshold. An overvoltage event will open the internal FET and assert $\overline{FLT}$ to indicate overvoltage.
GND	16	—	Ground.
ILIM	17	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit.
dVdT	18	I/O	A capacitor from this pin to GND sets the ramp rate of output voltage.
IMON	19	O	This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage, used as analog current monitor.
$\overline{FLT}$	20	O	Fault event indicator, goes low to indicate fault condition due to Undervoltage, Overvoltage, Reverse voltage and Thermal shutdown event. It is an open drain output.
PowerPAD™			The GND terminal must be connected to the exposed PowerPAD. This PowerPAD must be connected to a PCB ground plane using multiple vias for good thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	IN, OUT, PGTH, PGOOD, EN/UVLO, OVP, DEVSLP, $\overline{FLT}$	–0.3	20	V
	IN (10 ms Transient)		22	
	dVdT, ILIM	–0.3	3.6	
	IMON	–0.3	7	
Sink current	PGOOD, $\overline{FLT}$, dVdT		10	mA
Source current	dVdT, ILIM, IMON	Internally Limited		
Maximum junction, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C
Continuous power dissipation		See the *Thermal Characteristics* (2)		

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	IN	2.7		18	V
	EN/UVLO, OVP, DEVSLP, OUT, PGTH, PGOOD, $\overline{FLT}$	0		18	
	dVdT, ILIM	0		3	
	IMON	0		6	
Resistance	ILIM	16.9		150	kΩ
	IMON	1			
External capacitance	OUT	0.1			µF
	dVdT			470	nF
Operating junction temperature range, T_J		–40	25	125	°C

7.4 Thermal Characteristics (1)

THERMAL METRIC		TPS25940 RVC (20) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	40.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	13.7	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	3.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

Conditions are –40°C ≤ T_J=T_A ≤ 125°C, 2.7 V ≤ $V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND INTERNAL UNDERVOLTAGE LOCKOUT						
$V_{(IN)}$	Operating Input Voltage		2.7		18	V
$V_{(UVR)}$	Internal UVLO threshold, rising		2.2	2.3	2.4	V
$V_{(UVRhys)}$	Internal UVLO hysteresis		105	116	125	mV
$I_{Q(ON)}$	Supply current, Enabled	$V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 3 V	140	210	300	µA
		$V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 12 V	140	199	260	
		$V_{(EN/UVLO)}$ = 2 V, $V_{(IN)}$ = 18 V	140	202	270	
$I_{Q(OFF)}$	Supply current, Disabled	$V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 3 V	4	8.6	15	µA
		$V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 12 V	6	15	20	
		$V_{(EN/UVLO)}$ = 0 V, $V_{(IN)}$ = 18 V	8	18.5	25	
$I_{Q(DEVSLP)}$	Supply current, DevSleep Mode	$V_{(DEVSLP)}$ = 0 V, $V_{(IN)}$ = 2.7V to 18V	70	95	130	µA
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(ENR)}$	EN/UVLO threshold voltage, rising		0.97	0.99	1.01	V
$V_{(ENF)}$	EN/UVLO threshold voltage, falling		0.9	0.92	0.94	V
$V_{(SHUTF)}$	EN threshold voltage for Low I_Q shutdown, falling		0.3	0.47	0.63	V
$V_{(SHUTFhys)}$	EN hysteresis for low I_Q shutdown, hysteresis (1)			66		mV
I_{EN}	EN Input leakage current	0 V ≤ $V_{(EN/UVLO)}$ ≤ 18 V	–100	0	100	nA
OVER VOLTAGE PROTECTION (OVP) INPUT						
$V_{(OVPR)}$	Overvoltage Threshold Voltage, Rising,		0.97	0.99	1.01	V
$V_{(OVPF)}$	Overvoltage Threshold Voltage, Falling		0.9	0.92	0.94	V
$I_{(OVP)}$	OVP Input Leakage Current	0 V ≤ $V_{(OVP)}$ ≤ 5 V	-100	0	100	nA
DEVSLP MODE INPUT (DEVSLP): ACTIVE HIGH						
$V_{(DEVSLPR)}$	DEVSLP threshold voltage, rising		1.6	1.85	2	V
$V_{(DEVSLPF)}$	DEVSLP threshold voltage, falling		0.8	0.96	1.1	V
$I_{(DEVSLP)}$	DEVSLP input leakage current	0.2 V ≤ $V_{(DEVSLP)}$ ≤ 18 V	0.6	1	1.25	µA
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0 V	0.85	1	1.15	µA
$R_{(dVdT)}$	dVdT discharging resistance	EN/UVLO = 0 V, $I_{(dVdT)}$ = 10 mA sinking		16	24	Ω
$V_{(dVdTmax)}$	dVdT maximum capacitor voltage		2.6	2.88	3.1	V
$GAIN_{(dVdT)}$	dVdT to OUT gain	$\Delta V_{(OUT)}/\Delta V_{(dVdT)}$	11.65	11.9	12.05	V/V
CURRENT LIMIT PROGRAMMING (ILIM)						
$V_{(ILIM)}$	ILIM bias voltage			0.87		V
$I_{(LIM)}$	Current limit (2)	$R_{(ILIM)}$ = 150 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	0.53	0.58	0.63	A
		$R_{(ILIM)}$ = 88.7 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	0.9	0.99	1.07	
		$R_{(ILIM)}$ = 42.2 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	1.92	2.08	2.25	
		$R_{(ILIM)}$ = 24.9 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	3.25	3.53	3.81	
		$R_{(ILIM)}$ = 20 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	4.09	4.45	4.81	
		$R_{(ILIM)}$ = 16.9 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	4.78	5.2	5.62	
		$R_{(ILIM)}$ = OPEN, Open resistor current limit (Single Point Failure Test: UL60950)	0.35	0.45	0.55	
		$R_{(ILIM)}$ = SHORT, Shorted resistor current limit (Single Point Failure Test: UL60950)	0.55	0.67	0.8	
$I_{(DEVSLP(LIM))}$	DevSleep Mode Current Limit		0.55	0.67	0.8	A

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(2) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.

Electrical Characteristics (continued)

Conditions are –40°C ≤ T_J=T_A ≤ 125°C, 2.7 V ≤ $V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit current limit (2)	$R_{(ILIM)}$ = 42.2 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ -$V_{(OUT)}$) = 5 V	1.91	2.07	2.24	A
		$R_{(ILIM)}$ = 24.9 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ -$V_{(OUT)}$) = 5 V	3.21	3.49	3.77	
		$R_{(ILIM)}$ = 16.9 kΩ, $V_{(VIN)}$ = 12 V, ($V_{(IN)}$ -$V_{(OUT)}$)= 5 V, -40°C ≤ T_J ≤ 85°C	4.7	5.11	5.52	
$I_{(FASTRIP)}$	Fast-Trip comparator threshold(1)(2)			1.5 x $I_{(LIM)}$ + 0.375		A
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain Factor $I_{(IMON)}$:$I_{(OUT)}$	1 A ≤ $I_{(OUT)}$ ≤ 5 A	47.78	52.3	57.23	µA/A
MOSFET – POWER SWITCH						
R_{ON}	IN to OUT - ON Resistance	1 A ≤ $I_{(OUT)}$ ≤ 5 A, T_J = 25°C	34	42	49	mΩ
		1 A ≤ $I_{(OUT)}$ ≤ 5 A, -40°C ≤ T_J ≤ 85°C	26	42	58	
		1 A ≤ $I_{(OUT)}$ ≤ 5 A, -40°C ≤ T_J ≤ 125°C	26	42	64	
PASS FET OUTPUT (OUT)						
$I_{lkg(OUT)}$	OUT leakage current in off state	$V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 0 V, $V_{(OUT)}$ = 0 V (Sourcing)	–2	0	2	µA
		$V_{(IN)}$ = 2.7 V, $V_{(EN/UVLO)}$ = 0 V, $V_{(OUT)}$ = 18 V (Sinking)	6	13	20	
$V_{(REVTH)}$	$V_{(IN)}$ -$V_{(OUT)}$ threshold for reverse protection comparator, falling		–15	-9.3	–3	mV
$V_{(FWDTH)}$	$V_{(IN)}$ -$V_{(OUT)}$ threshold for reverse protection comparator, rising		86	100	114	mV
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ internal pull-down resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5 mA sinking	10	18	30	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 18 V	–1	0	1	µA
POSITIVE INPUT for POWER-GOOD COMPARATOR (PGTH)						
$V_{(PGTHR)}$	PGTH threshold voltage, rising		0.97	0.99	1.01	V
$V_{(PGTHF)}$	PGTH threshold voltage, falling		0.9	0.92	0.94	V
$I_{(PGTH)}$	PGTH input leakage current	0 V ≤ $V_{(PGTH)}$ ≤ 18 V	–100	0	100	nA
POWER-GOOD COMPARATOR OUTPUT (PGOOD): ACTIVE HIGH						
$R_{(PGOOD)}$	PGOOD internal pull-down resistance	$V_{(PGTH)}$ = 0V, $I_{(PGOOD)}$ = 5 mA sinking	10	20	35	Ω
$I_{(PGOOD)}$	PGOOD input leakage current	0 V ≤ $V_{(PGOOD)}$ ≤ 18 V	–1	0	1	µA
THERMAL SHUT DOWN (TSD)						
$T_{(TSD)}$	TSD Threshold(1)			160		°C
$T_{(TSDhys)}$	TSD Hysteresis(1)			12		°C
	Thermal Fault: (Latched or Auto-Retry)	TPS25940L		LATCHED		
		TPS25940A		AUTO-RETRY		

7.6 Timing Requirements

Conditions are –40°C ≤ T_J=T_A ≤ 125°C, 2.7 V ≤ $V_{(IN)}$ = 18 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted). Refer to Figure 42 for the timing diagrams.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE and UVLO INPUT						
$t_{ON(dly)}$	EN turn on delay	EN/UVLO ↑ (100mV above $V_{(ENR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ < 0.8 nF		220		µs
		EN/UVLO ↑ (100mV above $V_{(ENR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ ≥ 0.8 nF, [$C_{(dVdT)}$ in nF]		100 + 150 x $C_{(dVdT)}$		µs
$t_{OFF(dly)}$	EN turn off delay	EN/UVLO ↓ (100mV below $V_{(ENF)}$) to $\overline{FLT}$↓		2		µs
OVERVOLTAGE PROTECTION INPUT (OVP)						
$t_{OVP(dly)}$	OVP disable delay	OVP↑ (100mV above $V_{(OVPR)}$) to $\overline{FLT}$↓		2		µs
OUTPUT RAMP CONTROL (dV/dT)						
t_{dVdT}	Output ramp time	EN/UVLO ↑ to $V_{(OUT)}$ = 4.5 V, with $C_{(dVdT)}$ = open		0.12		ms
		EN/UVLO ↑ to $V_{(OUT)}$ = 11 V, with $C_{(dVdT)}$ = open	0.25	0.37	0.5	ms
		EN/UVLO ↑ to $V_{(OUT)}$ = 11 V, with $C_{(dVdT)}$ = 1 nF		0.97		ms
CURRENT LIMIT						
$t_{FASTRIP(dly)}$	Fast-Trip comparator delay	$I_{(OUT)}$ > $I_{(FASTRIP)}$		200		ns
REVERSE PROTECTION COMPARATOR						
$t_{REV(dly)}$	Reverse protection comparator delay	($V_{(IN)}$ - $V_{(OUT)}$)↓ (1 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$↓		10		µs
		($V_{(IN)}$ - $V_{(OUT)}$)↓ (10 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$↓		1		µs
$t_{FWD(dly)}$		($V_{(IN)}$ - $V_{(OUT)}$)↑ (10 mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$↑		3.1		µs
POWER-GOOD COMPARATOR OUTPUT (PGOOD): ACTIVE HIGH						
t_{PGOODR}	PGOOD delay (de-glitch) time	Rising edge	0.42	0.54	0.66	ms
t_{PGOODF}		Falling edge	0.42	0.54	0.66	ms
THERMAL SHUT DOWN (TSD)						
	Retry delay in TSD	TPS25940A Only		128		ms

7.7 Typical Characteristics

Conditions are –40°C ≤ T_A = T_J ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

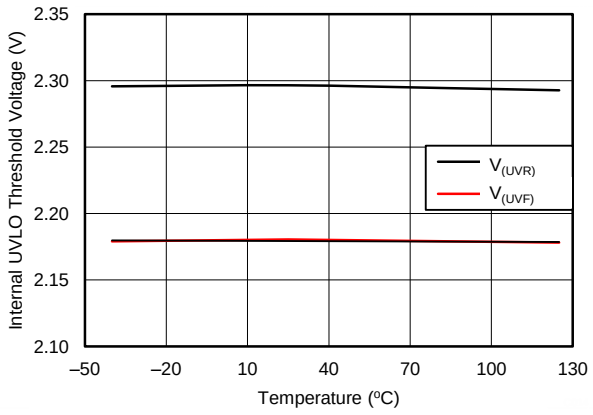


Figure 1. UVLO Threshold Voltage vs Temperature

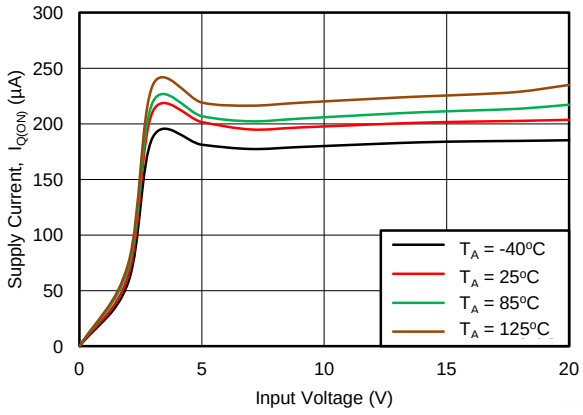


Figure 2. Input Supply Current vs Supply Voltage During Normal Operation

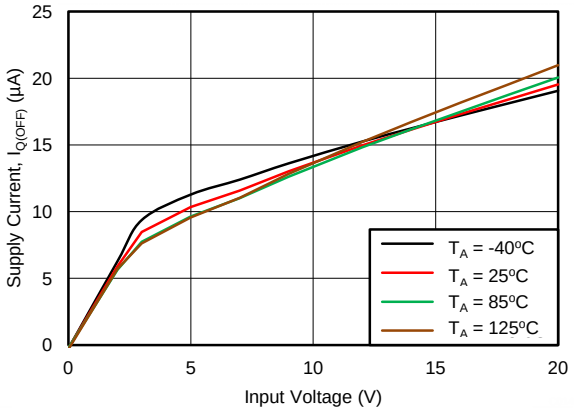


Figure 3. Input Supply Current vs Supply Voltage at Shutdown

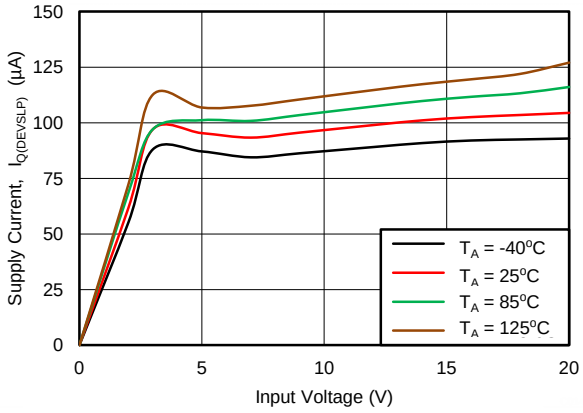


Figure 4. Input Supply Current vs Supply Voltage in DevSleep Mode

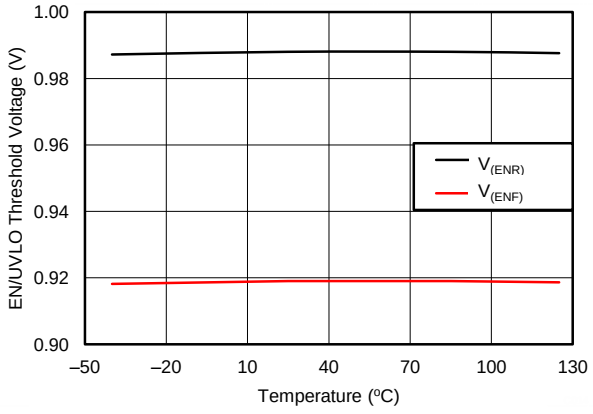


Figure 5. EN Threshold Voltage vs Temperature

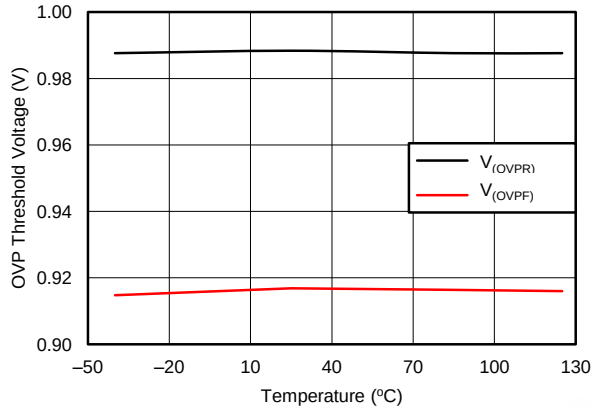


Figure 6. OVP Threshold Voltage vs Temperature

Typical Characteristics (continued)

Conditions are –40°C ≤ T_A = T_J ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

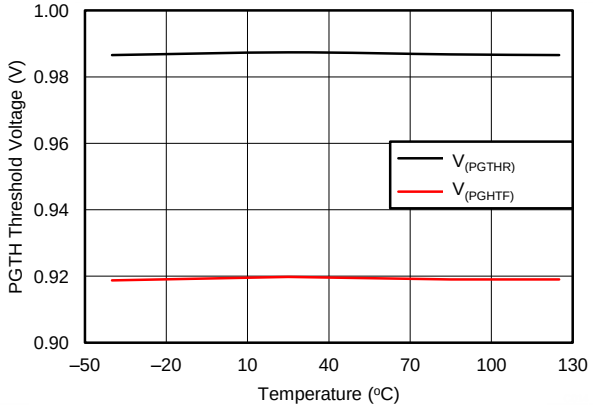


Figure 7. PGTH Threshold Voltage vs Temperature

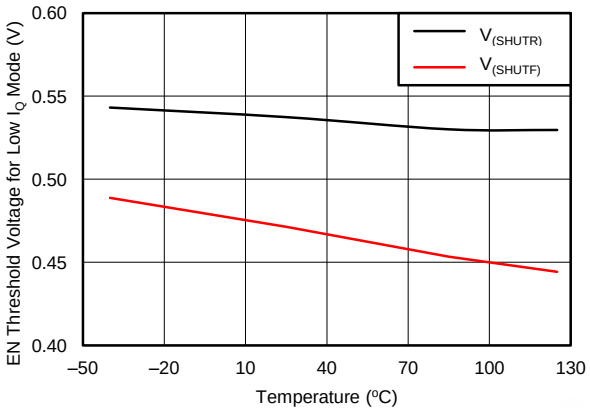


Figure 8. EN Threshold Voltage for Low IQ mode vs Temperature

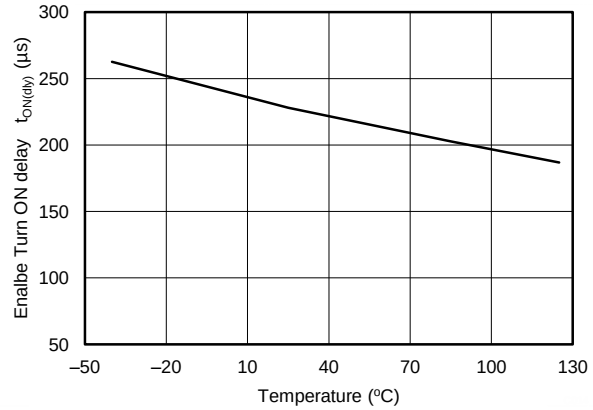


Figure 9. Enable Turn ON Delay vs Temperature

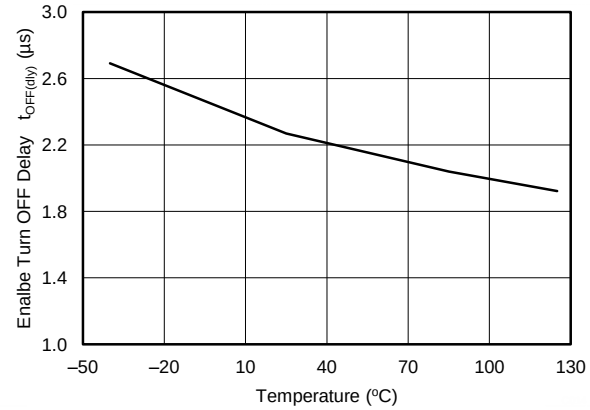


Figure 10. Enable Turn OFF Delay vs Temperature

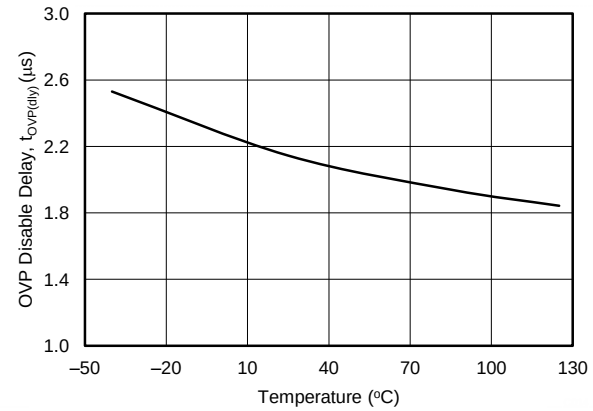


Figure 11. OVP Disable Delay vs Temperature

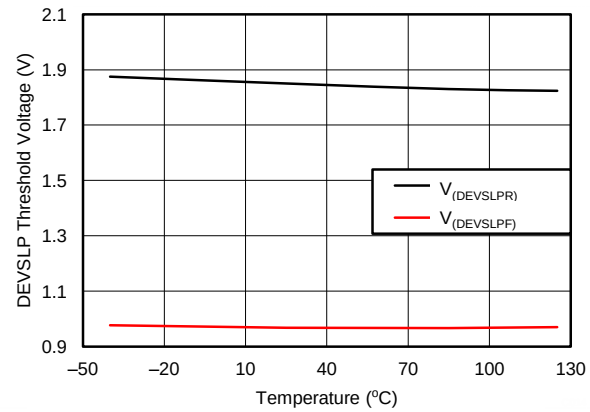


Figure 12. DEVSLP Threshold Voltage vs Temperature

Typical Characteristics (continued)

Conditions are –40°C ≤ T_A = T_J ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

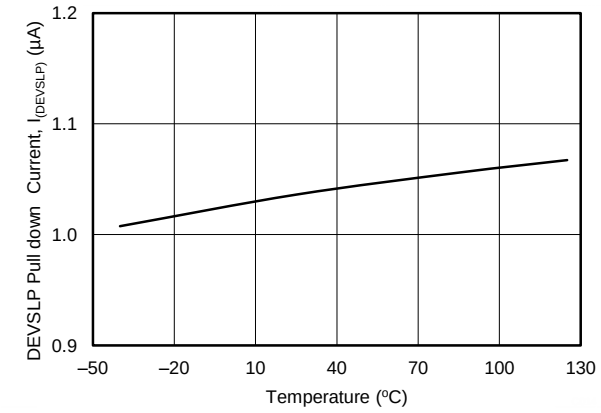


Figure 13. DEVSLP Pull Down Current vs Temperature

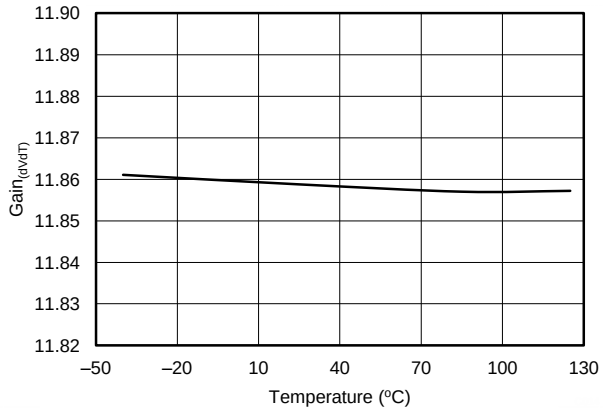


Figure 14. GAIN$_{(dVdT)}$ vs Temperature

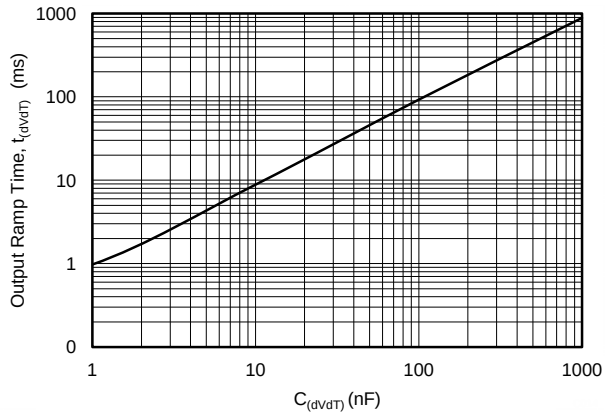


Figure 15. Output Ramp Time vs $C_{(dVdT)}$

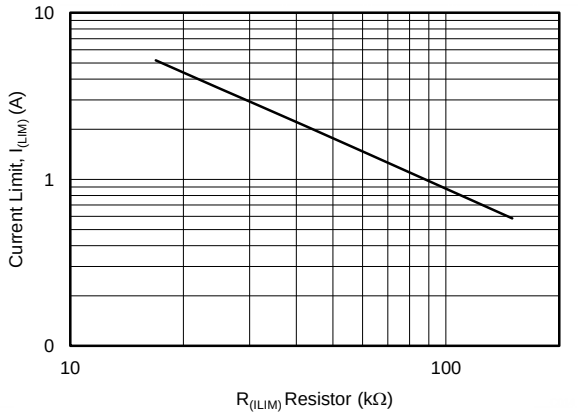


Figure 16. Current Limit vs Current Limit Resistor

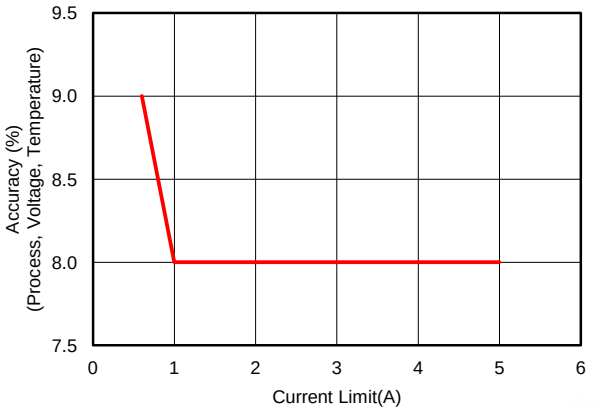


Figure 17. Current Limit Accuracy vs Current Limit

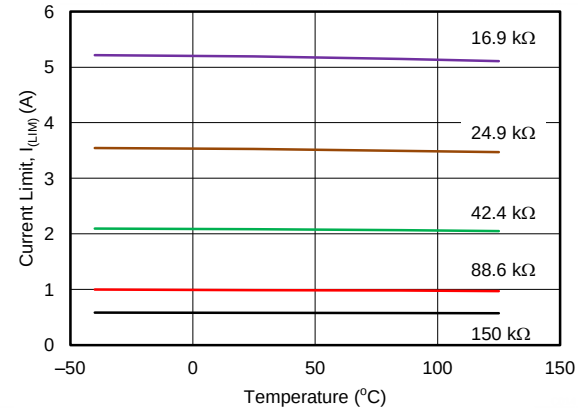


Figure 18. Current Limit vs Temperature Across $R_{(ILIM)}$

Typical Characteristics (continued)

Conditions are –40°C ≤ T_A = T_J ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

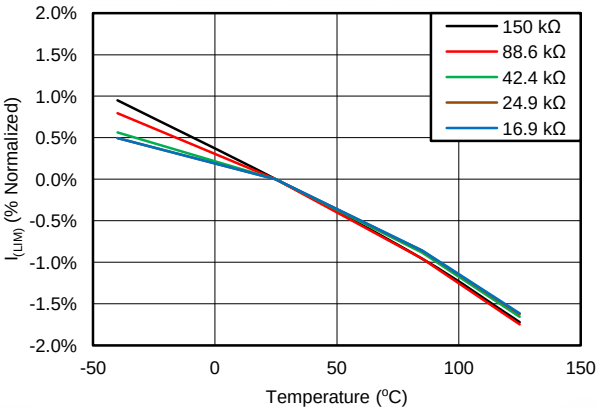
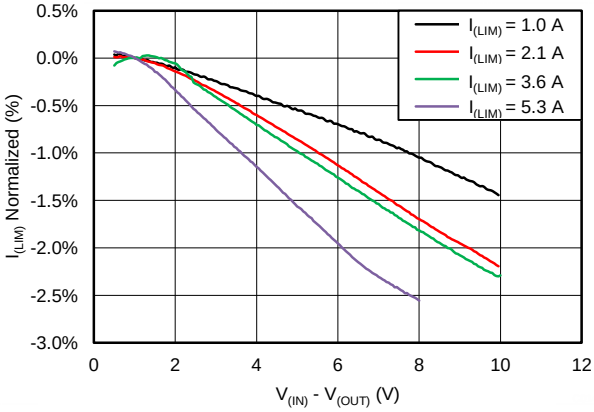


Figure 19. Current Limit (% Normalized) vs $R_{(LIMIT)}$ Resistor



Thermal shutdown occurs when $I_{(LIM)}$ = 5.3 A and [$V_{(IN)}$ - $V_{(OUT)}$] > 8 V

Figure 20. Current Limit Normalized (%) vs $V_{(IN)}$ - $V_{(OUT)}$

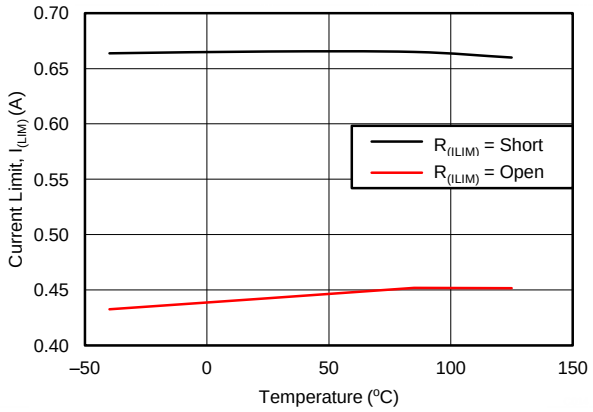


Figure 21. Current Limit for $R_{(ILIM)}$ = Open and Short vs Temperature

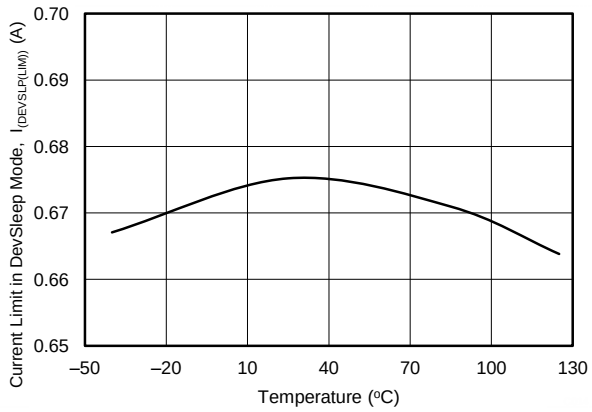


Figure 22. Current Limit in DevSleep Mode vs Temperature

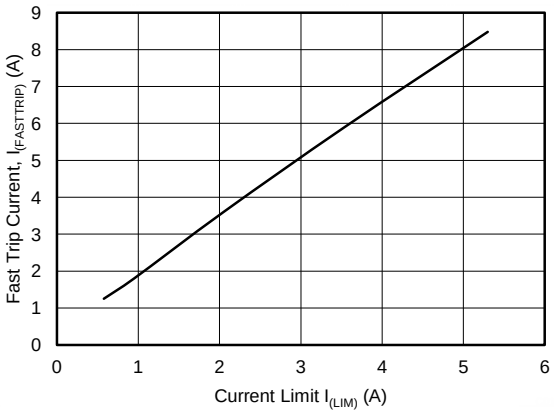


Figure 23. Fast Trip Threshold vs Current Limit

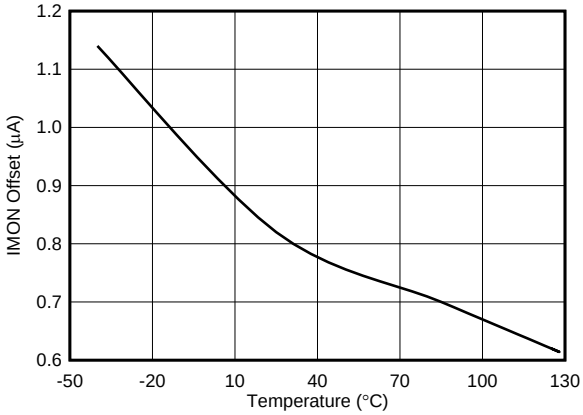


Figure 24. IMON Offset vs Temperature

Typical Characteristics (continued)

Conditions are –40°C ≤ T_A = T_J ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)

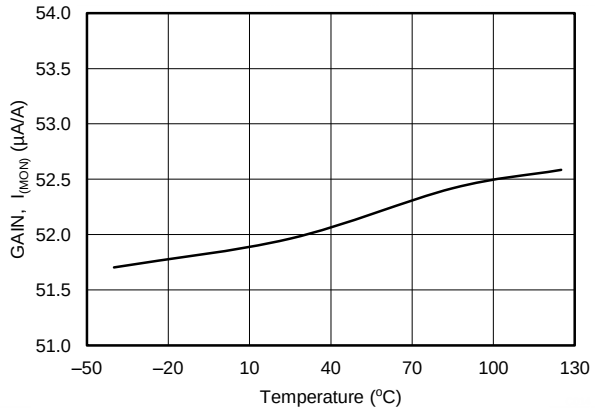


Figure 25. $GAIN_{(IMON)}$ vs Temperature

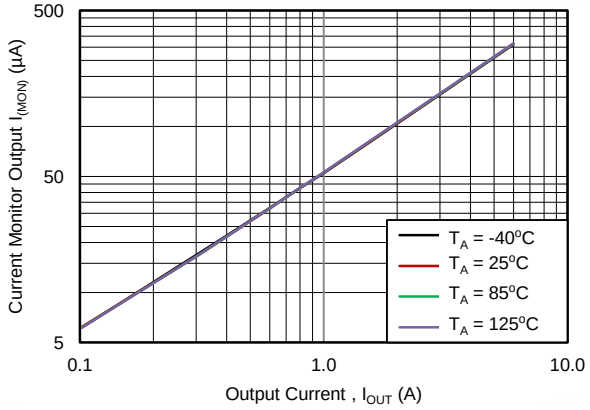


Figure 26. Current Monitor Output vs Output Current

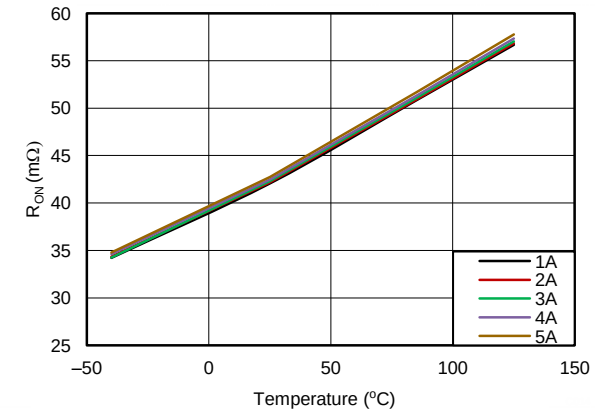


Figure 27. R_{ON} vs Temperature Across Load Current

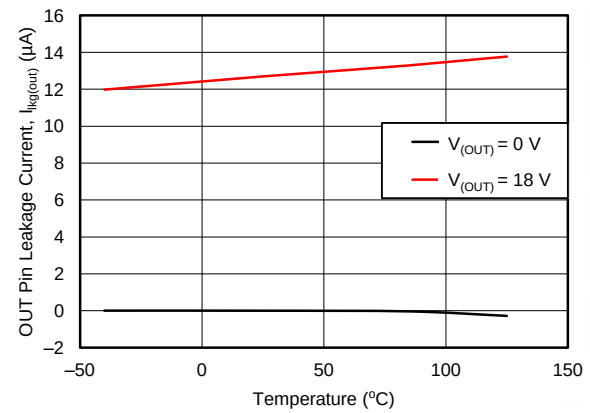


Figure 28. OUT Leakage Current in Off State vs Temperature

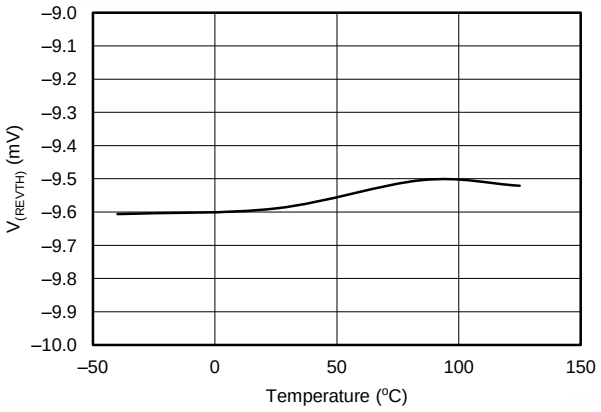


Figure 29. $V_{(REVTH)}$ vs Temperature

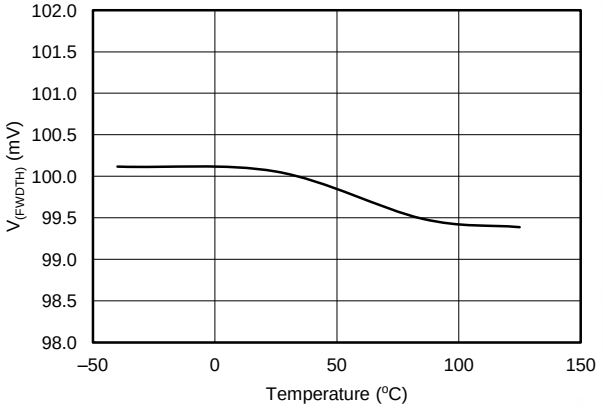
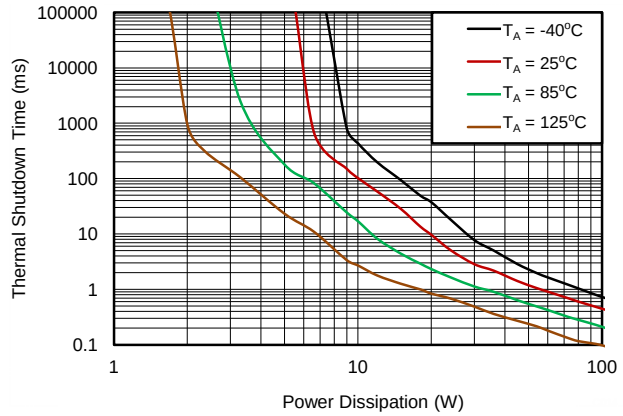


Figure 30. $V_{(FWDTH)}$ vs Temperature

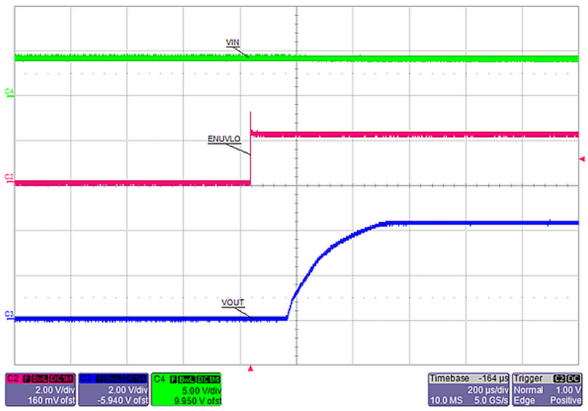
Typical Characteristics (continued)

Conditions are –40°C ≤ T_A = T_J ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)



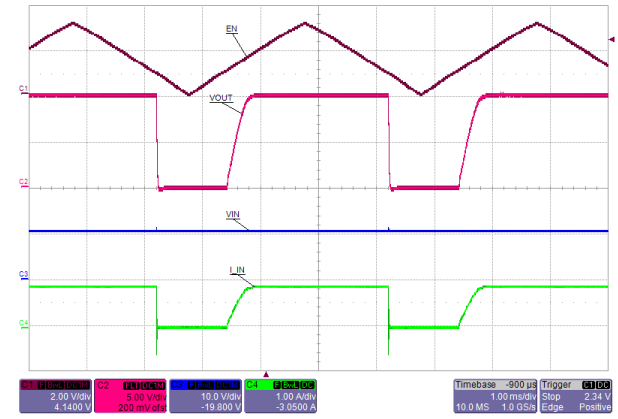
Taken on 2-Layer board, 2oz.(0.08-mm thick) with GND plane area: 14 cm2 (Top) and 20 cm2 (bottom)

Figure 31. Thermal Shutdown Time vs Power Dissipation



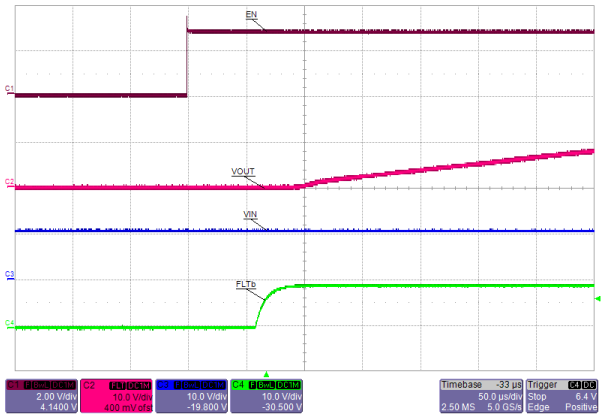
$V_{(IN)}$ = 4.5 V

Figure 32. Turn ON with Enable



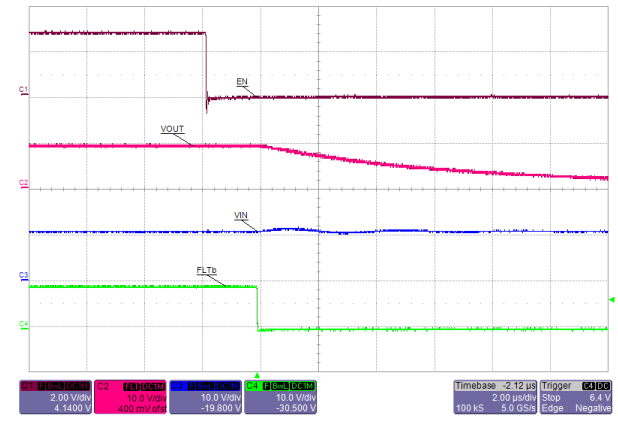
$V_{(IN)}$ = 11 V

Figure 33. Turn ON and OFF with Enable



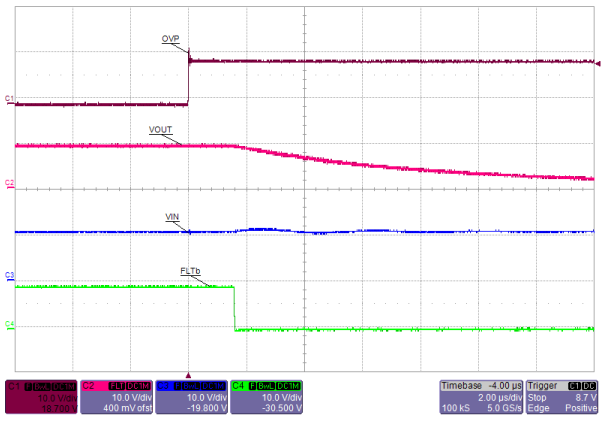
$R_{(\overline{FLT})}$=100 kΩ

Figure 34. EN Turn ON Delay : EN ↑ to Output Ramp ↑



$R_{(\overline{FLT})}$=100 kΩ

Figure 35. EN Turn OFF Delay : EN ↓ to Fault ↓

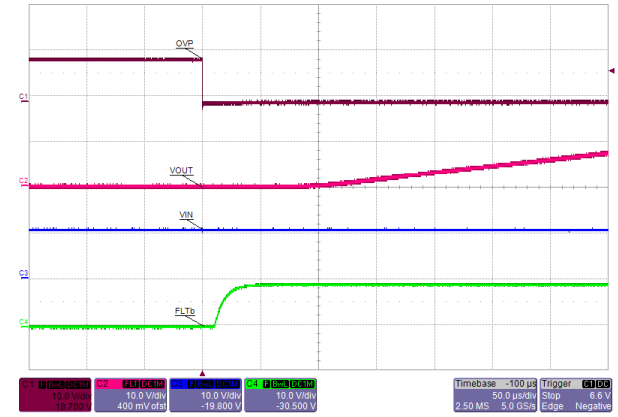


$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{(\overline{FLT})}$=100 kΩ

Figure 36. OVP Turn OFF delay: OVP ↑ to Fault ↓

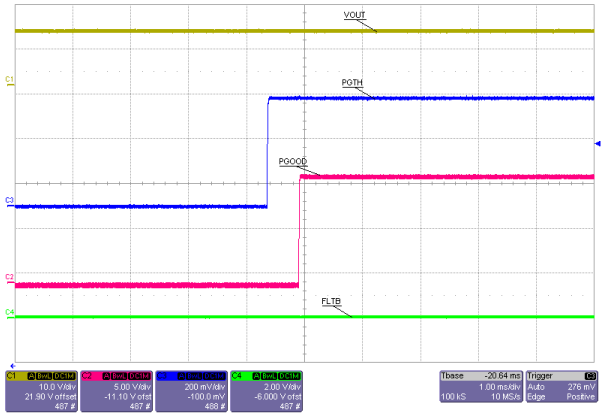
Typical Characteristics (continued)

Conditions are –40°C ≤ T_A = T_J ≤ 125°C, $V_{(IN)}$ = 12 V, $V_{(EN/UVLO)}$ = 2 V, $V_{(OVP)}$ = $V_{(DEVSLP)}$ = $V_{(PGTH)}$ = 0 V, $R_{(ILIM)}$ = 150 kΩ, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN, PGOOD = $\overline{FLT}$ = IMON = OPEN. (unless stated otherwise)



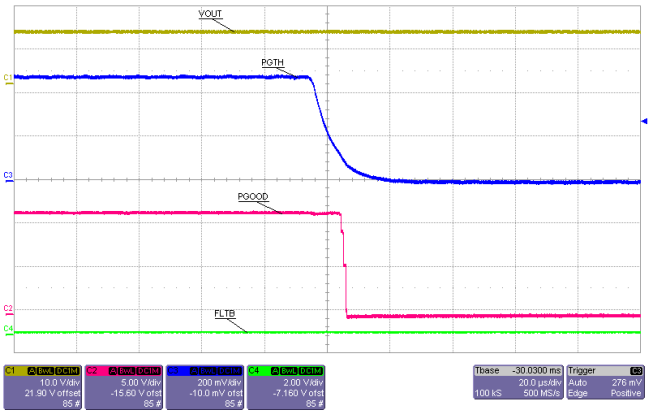
$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{(\overline{FLT})}$=100 kΩ

Figure 37. OVP Turn ON delay: OVP ↓ to Output Ramp ↑



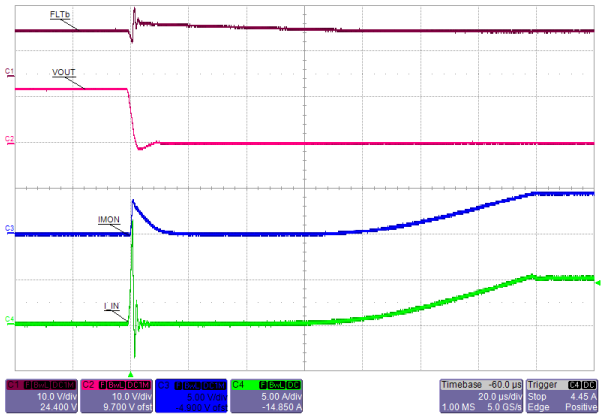
$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{(\overline{FLT})}$= 100 kΩ $R_{(PGOOD)}$= 100 kΩ

Figure 38. Power Good Delay (Rising)



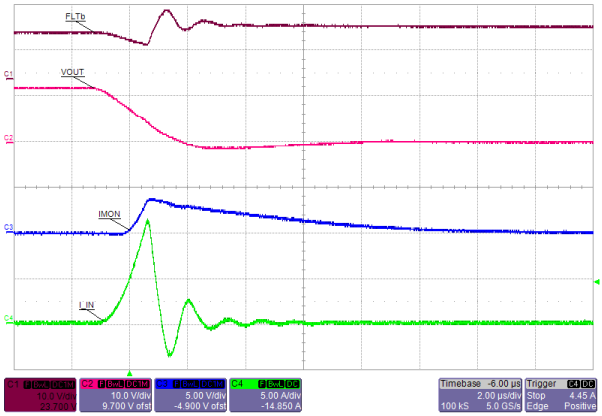
$V_{(IN)}$ = 12 V R_L = 12 Ω $R_{(\overline{FLT})}$= 100 kΩ $R_{(PGOOD)}$= 100 kΩ

Figure 39. Power Good Delay (Falling)



$R_{(\overline{FLT})}$ = 100 kΩ $R_{(IMON)}$ = 16.9 kΩ $R_{(ILIM)}$ = 17.8 kΩ

Figure 40. Hot-Short: Fast Trip Response and Current Regulation



$R_{(\overline{FLT})}$= 100 kΩ $R_{(IMON)}$ = 16.9 kΩ $R_{(ILIM)}$ = 17.8 kΩ

Figure 41. Hot-Short: Fast Trip Response (Zoomed)

8 Parametric Measurement Information

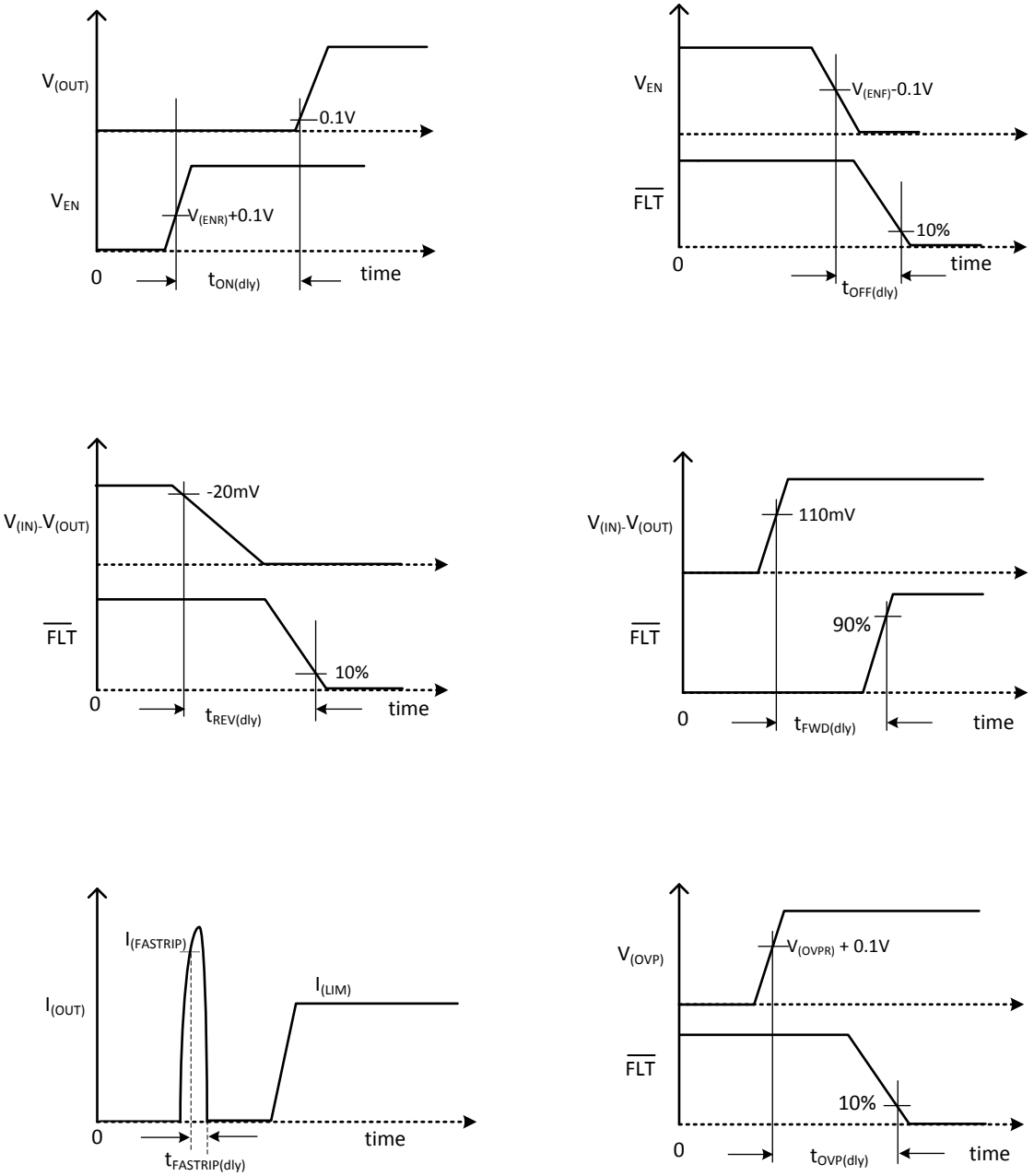


Figure 42. Timing Diagrams

9 Detailed Description

9.1 Overview

TPS25940 is a smart eFuse with integrated back-to-back FETs and enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 2.7 V to 18 V.

For hot-plug-in boards, the device provides hot-swap power management with in-rush current control and programmable output ramp-rate. The device integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.6 A and 5.3 A via an external resistor.

The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault for downstream system. Its overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip.

The device is designed to protect systems such as enterprise SSD drives against sudden power loss events. The device monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse blocking from output when reverse condition or input power fail condition is detected. Also, the device signals the downstream controller to initiate transfer of power to the hold-up capacitor for data hardening.

The additional features include:

- Precise current monitor output for health monitoring of the system
- Additional power good comparator with precision internal reference for output or any other rail voltage monitoring
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for brown-out and overvoltage faults
- A choice of latched or automatic restart mode

9.2 Functional Block Diagram

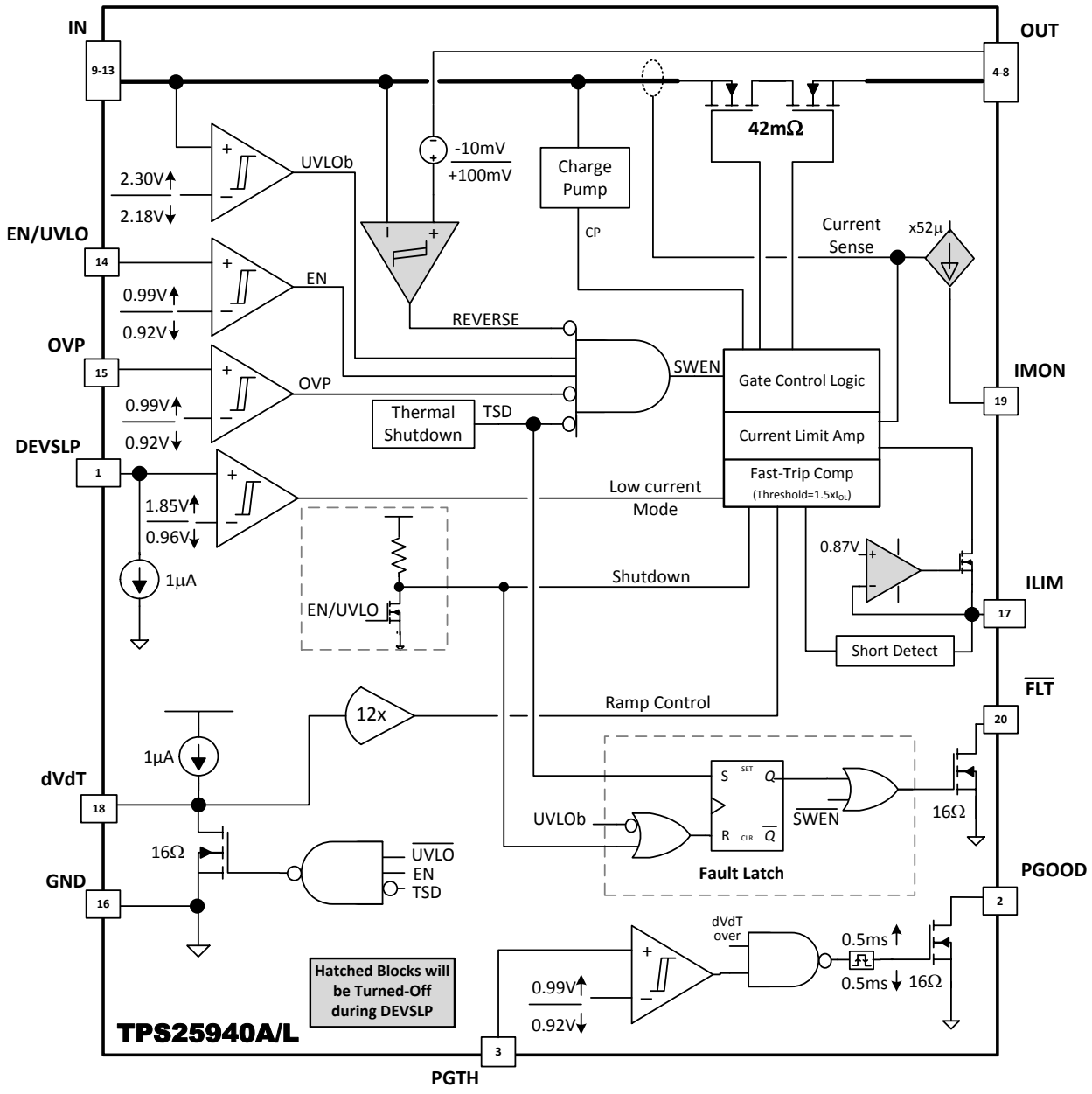


Figure 43. TPS25940A/L Block Diagram

9.3 Feature Description

9.3.1 Enable and Adjusting Undervoltage Lockout

The EN/UVLO pin controls the ON/OFF state of the internal FET. A voltage $V_{(EN/UVLO)} < V_{(ENF)}$ on this pin will turn off the internal FET, thus disconnecting IN from OUT, while voltage below $V_{(SHUTF)}$ will take the device into shutdown mode, with I_Q less than 15 µA to ensure minimal power loss. Cycling EN/UVLO low and then back high resets the TPS25940L that has latched off due to a fault condition.

The internal de-glitch delay on EN/UVLO falling edge is kept low for quick detection of power failure. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO terminal to GND.

The undervoltage lock out can be programmed by using an external resistor divider from supply IN terminal to EN/UVLO terminal to GND as shown in Figure 44. When an undervoltage or input power fail event is detected, the internal FET is quickly turned off, and $\overline{FLT}$ is asserted. If the Under-Voltage Lock-Out function is not needed, the EN/UVLO terminal should be connected to the IN terminal. EN/UVLO terminal should not be left floating.

The device also implements internal undervoltage-lockout (UVLO) circuitry on the IN terminal. The device disables when the IN terminal voltage falls below internal UVLO Threshold $V_{(UVF)}$. The internal UVLO threshold has a hysteresis of 115mV.

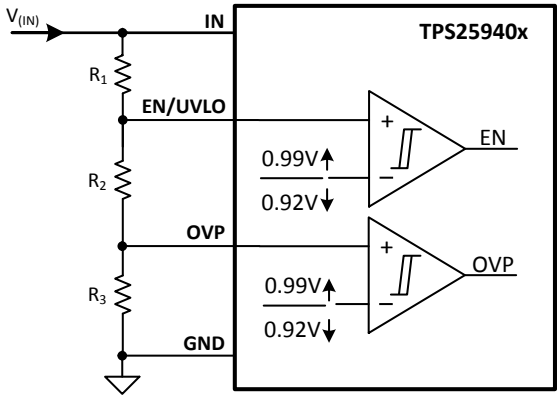


Figure 44. UVLO and OVP Thresholds Set By R_1, R_2 and R_3

9.3.2 Overvoltage Protection (OVP)

The device incorporates circuit to protect system during overvoltage conditions. A resistor divider connected from the supply to OVP terminal to GND (as shown in Figure 44) programs the overvoltage threshold. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. This pin should be tied to GND when not used.

9.3.3 Hot Plug-in and In-Rush Current Control

The device is designed to control the in-rush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. A slew rate controlled startup (dVdT) also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on (as shown in Figure 45). Equation governing slew rate at start-up is shown in Equation 1 :

Feature Description (continued)

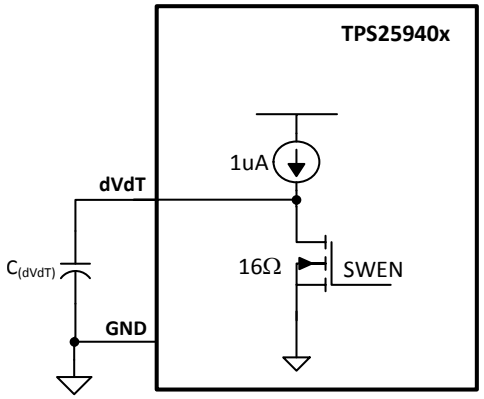


Figure 45. Output Ramp Up Time t_{dVdT} is Set by $C_{(dVdT)}$

$$I_{(dVdT)} = \left(\frac{C_{(dVdT)}}{GAIN_{(dVdT)}} \right) x \left(\frac{dV_{(OUT)}}{dt} \right) \quad (1)$$

Where:

- $I_{(dVdT)}$ = 1 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$ = Desired output slew rate
- $GAIN_{(dVdT)}$ = dVdT to OUT gain = 12

The total ramp time (t_{dVdT}) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using Equation 2:

$$t_{dVdT} = 8.3 \times 10^4 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

The inrush current, $I_{(INRUSH)}$ can be calculated as

$$I_{(INRUSH)} = C_{(OUT)} \times V_{(IN)} / t_{dVdT}. \quad (3)$$

The dVdT pin can be left floating to obtain a predetermined slew rate (t_{dVdT}) on the output. When terminal is left floating, the device sets an internal ramp rate of 12V/ms for output ($V_{(OUT)}$) ramp.

Figure 58 and Figure 59 illustrate the inrush current control behavior of the device. For systems where load is present during start-up, the current never exceeds the overcurrent limit set by $R_{(ILIM)}$ resistor for the application. For defining appropriate charging time/rate under different load conditions, refer to the *Setting Output Voltage Ramp time (t_{dVdT})* section.

9.3.4 Overload and Short Circuit Protection :

At all times load current is monitored by sensing voltage across an internal sense resistor. During overload events, current is limited to the current limit ($I_{(LIM)}$) programmed by $R_{(ILIM)}$ resistor

$$I_{(LIM)} = \frac{89}{R_{(ILIM)}} \quad (4)$$

- $I_{(LIM)}$ is overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ

The device incorporates two distinct levels: a current limit ($I_{(LIM)}$) and a fast-trip threshold ($I_{(FASTRIP)}$). Fast trip and current limit operation are shown in Figure 46.

Bias current on ILIM pin directly controls current-limiting behavior of the device, and PCB routing of this node must be kept away from any noisy (switching) signals.

Feature Description (continued)

9.3.4.1 Overload Protection

For overload conditions, the internal current-limit amplifier regulates the output current to $I_{(LIM)}$. The output voltage droops during the current regulation, resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold ($T_{(TSD)}$), the internal FET is turned off. Once in thermal shutdown, The TPS25940L version stays latched off, whereas TPS25940A commences an auto-retry cycle 128 ms after $T_J < [T_{(TSD)} - 12°C]$. During thermal shutdown, the fault pin $\overline{FLT}$ pulls low to signal a fault condition. Figure 62 and Figure 63 illustrate overload behavior.

9.3.4.2 Short Circuit Protection

During a transient short circuit event, the current through the device increases very rapidly. As current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold $I_{(FASTRIP)}$. This comparator shuts down the pass device within 1µs, when the current through internal FET exceeds $I_{(FASTRIP)}$ ($I_{(OUT)} > I_{(FASTRIP)}$), and terminates the rapid short-circuit peak current. The trip threshold is set to more than 50% of the programmed overload current limit ($I_{(FASTRIP)} = 1.5 \times I_{(LIM)} + 0.375$). The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(LIM)}$. Then, device behaves similar to overload condition. Figure 64 through Figure 66 illustrate the behavior of the system when the current exceeds the fast-trip threshold.

9.3.4.3 Start-Up with Short on Output

During start-up into a short circuit current is limited to $I_{(LIM)}$. Figure 67 and Figure 68 illustrate start-up with a short on the output. This feature helps in quick fault isolation and hence ensures stability of the DC bus.

9.3.4.4 Constant Current Limit Behavior During Overcurrent Faults

When power dissipation in the internal FET [$P_D = (V_{(IN)} - V_{(OUT)}) \times I_{(OUT)}$] > 10 W, there is a ~0 to 5 % thermal fold back in the current limit value so that $I_{(LIM)}$ drops to I_{OS}. Eventually, the device shuts down due to over temperature.

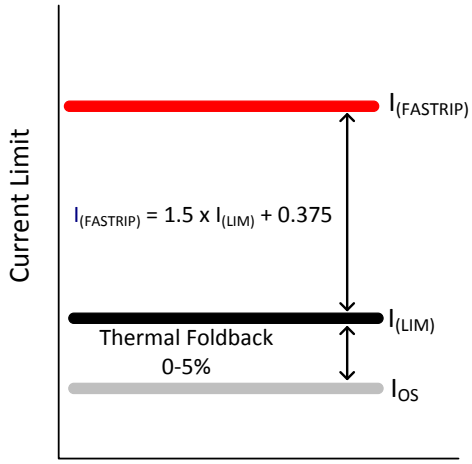


Figure 46. Fast-Trip Current

9.3.5 FAULT Response

The $\overline{FLT}$ open-drain output is asserted (active low) during undervoltage, overvoltage, reverse voltage/current and thermal shutdown conditions. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. The device is designed to eliminate false fault reporting by using an internal "de-glitch" circuit for undervoltage and overvoltage (2.2-µs typical) conditions without the need for external circuitry. This ensures that fault is not accidentally asserted during transients on input bus.

Connect $\overline{FLT}$ with a pull up resistor to Input or Output voltage rail. $\overline{FLT}$ may be left open or tied to ground when not used. $V_{(IN)}$ falling below $V_{(UVF)}$ = 2.1 V resets $\overline{FLT}$.

Feature Description (continued)

9.3.6 Current Monitoring:

The current source at IMON terminal is configured to be proportional to the current flowing from IN to OUT. This current can be converted to a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND terminal. This voltage, computed using Equation 6, can be used as a means of monitoring current flow through the system.

The maximum voltage range for monitoring the current ($V_{(IMONmax)}$) is limited to minimum([$V_{(IN)}$- 2.2 V], 6.0 V) to ensure linear output. This puts limitation on maximum value of $R_{(IMON)}$ resistor and is determined by Equation 5.

$$R_{(IMONmax)} = \frac{\text{minimum } (V_{(IN)} - 2.2, 6)}{1.6 \times I_{(LIM)} \times GAIN_{(IMON)}} \quad (5)$$

The output voltage at IMON terminal is calculated from Equation 6.

$$V_{(IMON)} = \left[I_{(OUT)} \times GAIN_{(IMON)} + I_{(IMON\_OS)} \right] \times R_{(IMON)} \quad (6)$$

Where

- $GAIN_{(IMON)}$ = Gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 52 µA/A
- $I_{(OUT)}$ = Load current
- $I_{(IMON\_OS)}$ = 0.8 µA (typ)

This pin should not have a bypass capacitor to avoid delay in the current monitoring information.

The voltage at IMON pin can be digitized using an ADC (such as ADS1100, SBAS239) to read the current monitor information over an I2C bus.

9.3.7 Power Good Comparator

The device incorporates a Power Good comparator for co-ordination of status to downstream DC-DC converters or system monitoring circuits. The comparator has an internal reference of $V_{(PGTHR)}$ = 0.99 V at negative terminal and positive terminal PGTH can be utilized for monitoring of either input or output of the device. The comparator output PGOOD is an open-drain active high signal, which can be used to indicate the status to downstream units. PGOOD is asserted high when internal FET is fully enhanced and PGTH pin voltage is higher than internal reference $V_{(PGTHR)}$.

The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully enhanced before heavy load is applied by downstream converters. Rising de-glitch delay is determined by Equation 7.

$$t_{PGOOD(degl)} = \text{Maximum}\{(3.5 \times 10^6 \times C_{(dVdT)}), t_{PGOODR}\} \quad (7)$$

Connect the PGOOD pin with a pull up resistor to Input or Output voltage rail. PGOOD may be left open or tied to ground when not used.

9.3.8 IN, OUT and GND Pins

The device has multiple pins for input (IN) and output (OUT).

All IN pins should be connected together and to the power source. A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 2.7 V – 18 V.

Similarly all OUT pins should be connected together and to the load. $V_{(OUT)}$ in the ON condition, is calculated using the Equation 8

$$V_{(OUT)} = V_{(IN)} - (R_{ON} \times I_{(OUT)}) \quad (8)$$

where, R_{ON} is the total ON resistance of the internal FET.

GND terminal is the most negative voltage in the circuit and is used as a reference for all voltage reference unless otherwise specified.

9.3.9 Thermal Shutdown:

Internal over temperature shutdown disables turns off the FET when T_J > 160°C (typical). The TPS25940L version latches off the internal FET, whereas TPS25940A commences an auto-retry cycle128 ms after T_J drops below [$T_{(TSD)}$ - 12°C]. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to signal a fault condition.

9.4 Device Functional Modes

9.4.1 DevSleep Mode for SATA® Interface Devices

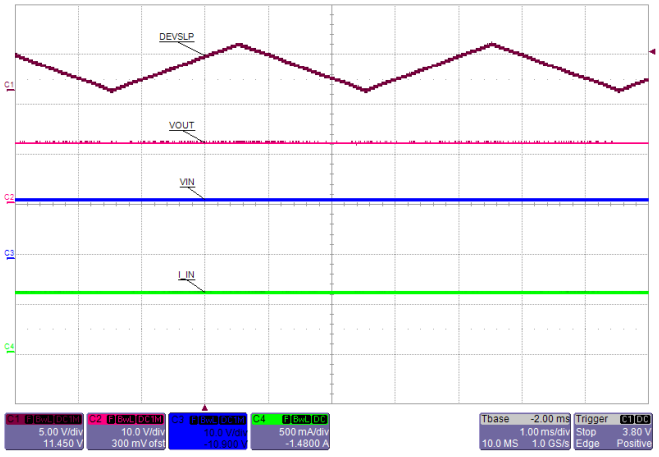
DevSleep is a new state introduced in the SATA® specification, which requires SATA-based storage solutions to reach a level of low power operation. This is appended to meet the aggressive power/battery life requirements of SATA-based mobile devices. DevSleep enables hosts and devices to completely hibernate the SATA interface. This saves more power versus the existing Partial and Slumber interface power states, which require that the PHY be left powered. In this mode, power consumption is limited to 5 mW or less for SSDs.

Detailed information on DevSleep is available in document *'SATA-DevSleep'* and on www.sata-io.org

TPS25940 provides a dedicated DevSleep interface terminal (DEVSLP) to drive the device in low power mode. The DEVSLP terminal is compatible with standard hardware signals asserted from the host controller. When pulled high, it puts the device in low power DevSleep mode. In this mode, the quiescent current consumption of the device is limited to less than 130 µA (95 µA typical). During this mode, the output voltage remains active, the overload current limit is set to $I_{(DEVSLP(LIM))}$ and functionality of reverse comparator and current monitoring is disabled. All other protections are kept active ensuring the safety of the system even in DevSleep mode.

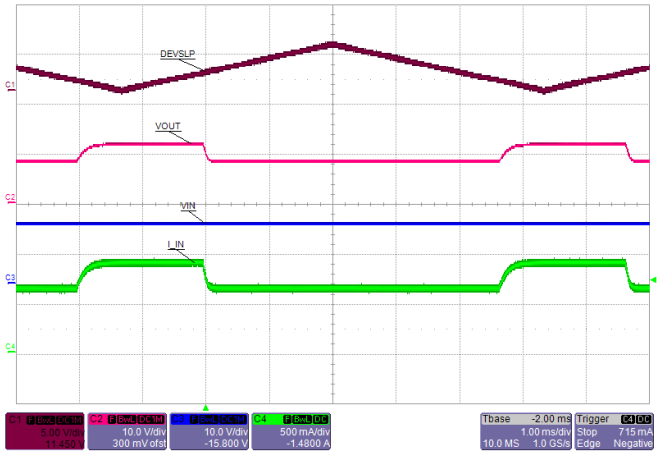
User must ensure that load currents on the bus are limited to less than $I_{(DEVSLP(LIM))}$, when the device is driven to DevSleep mode. Also, while coming out of DevSleep, it is important to sequence the TPS25940 earlier than the load. Otherwise, the load can exceed $I_{(DEVSLP(LIM))}$ and cause TPS25940 to enter the overload mode.

Figure 47 through Figure 50 illustrate the behavior of the system in DevSleep mode.



$V_{(IN)}$ = 12 V $I_{(LIM)}$ = 5.3A R_L = 22Ω
$C_{(OUT)}$ = 1 µF

Figure 47. IN and OUT of DevSleep Mode with 550 mA Load



$V_{(IN)}$ = 12 V $I_{(LIM)}$ = 5.3A R_L = 15Ω
$C_{(OUT)}$ = 1 µF

Figure 48. IN and OUT of DevSleep Mode with 800 mA Load. In DevSleep, Load Current gets Limited to $I_{(DEVSLP(LIM))}$

Device Functional Modes (continued)

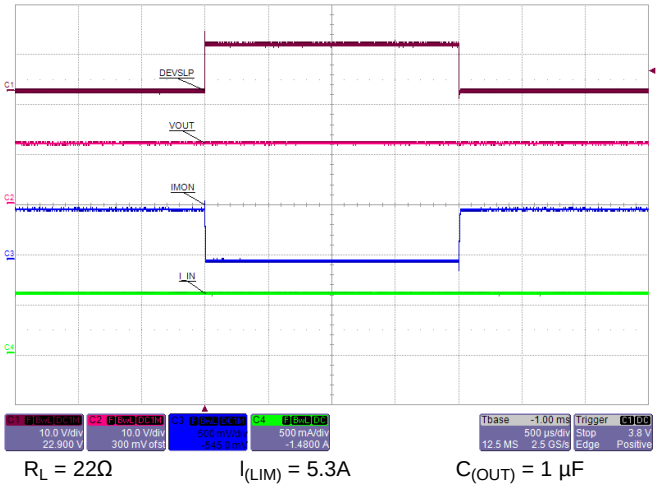


Figure 49. IMON Disabled in DevSleep Mode

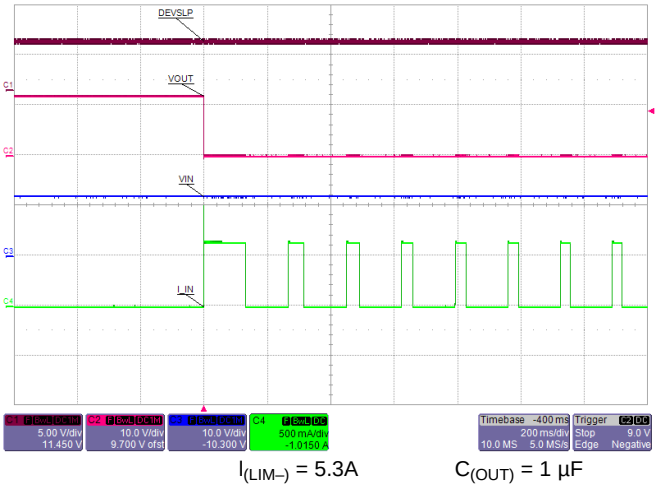


Figure 50. Hot Short and Retry in DevSleep Mode

9.4.2 Shutdown Control

The internal FET and hence the load current can be remotely switched off by taking the UVLO pin below its 0.6 V threshold with an open collector or open drain device as shown in Figure 51. The device quiescent current is reduced to less than 20 µA in this state. Upon releasing the UVLO pin the device turns on with soft-start cycle.

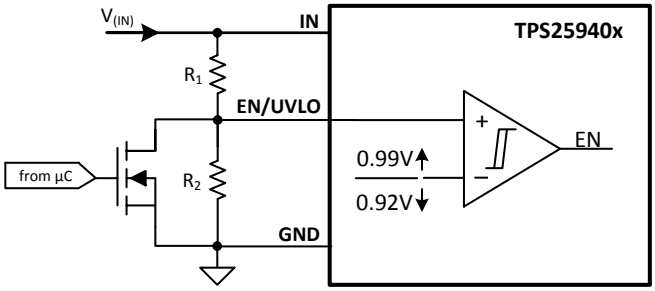


Figure 51. Shutdown Control

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS25940 is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 2.7 V to 18 V with programmable current limit, overvoltage and undervoltage protection. The device aids in controlling the in-rush current and provides fast turn-off during reverse voltage conditions for systems such as Enterprise SSDs, HDDs, Servers, Power Back-up Storage units and RAID cards. The device also provides robust protection for multiple faults on the sub-system rail.

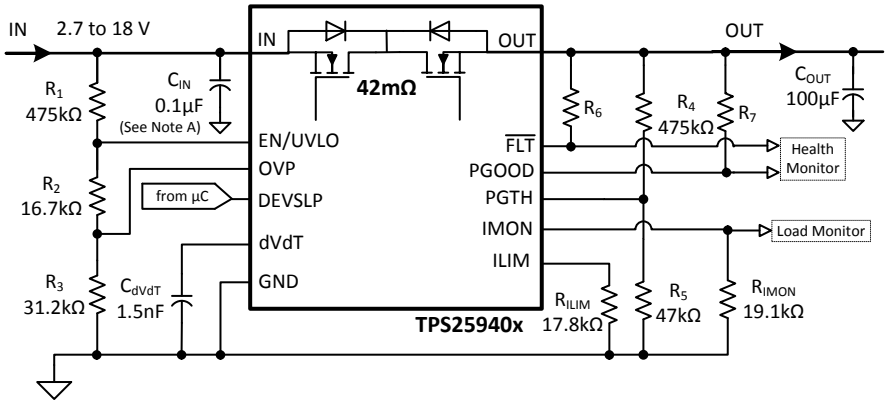
The following design procedure can be used to select component values for the device.

Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS25940 Design Calculator* is available on web folder.

This section presents a simplified discussion of the design process.

10.2 Typical Application

10.2.1 eFuse for Enterprise SSDs



A. C_{IN}: Optional and only for noise suppression.

Figure 52. Typical Application Schematics: eFuse for Enterprise SSDs

Typical Application (continued)

10.2.1.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, $V_{(IN)}$	12 V
Undervoltage lockout set point, $V_{(UV)}$	10.8 V
Overvoltage protection set point , $V_{(LIM)}$	16.5 V
Load at Start-Up , $R_{L(SU)}$	4.8 Ω
Current limit, $I_{(LIM)}$	5 A
Load capacitance , $C_{(OUT)}$	100 µF
Maximum ambient temperatures , T_A	85°C

10.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25940A and TPS25940L.

10.2.1.2.1 Step by Step Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

10.2.1.2.2 Programming the Current-Limit Threshold: $R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4.

$$R_{(ILIM)} = \frac{89}{5} = 17.8k\Omega \tag{9}$$

Choose closest standard value: 17.8k, 1% standard value resistor.

10.2.1.2.3 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using the external voltage divider network of R_1, R_2 and R_3 as connected between IN, EN, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated solving Equation 10 and Equation 11.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)} \tag{10}$$

$$V_{(ENR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)} \tag{11}$$

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)}/(R_1 + R_2 + R_3)$}, it is recommended to use higher values of resistance for R_1, R_2 and R_3.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I_{(R123)}$ must be chosen to be 20x greater than the leakage current expected.

From the device electrical specifications, $V_{(OVPR)}$ = 0.99 V and $V_{(ENR)}$ = 0.99 V. For design requirements, $V_{(OV)}$ is 16.5 V and $V_{(UV)}$ is 10.8 V. To solve the equation, first choose the value of R_3 = 31.2 kΩ and use Equation 10 to solve for (R_1 + R_2) = 488.8 kΩ. Use Equation 11 and value of (R_1 + R_2) to solve for R_2 = 16.47 kΩ and finally R_1= 472.33 kΩ.

Using the closest standard 1% resistor values gives R_1 = 475 kΩ, R_2 = 16.7 kΩ, and R_3 = 31.2 kΩ.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 7% lower than the rising threshold, $V_{(UV)}$. This is calculated using Equation 12.

$$V_{(PFAIL)} = 0.93 \times V_{(UV)} \quad (12)$$

10.2.1.2.4 Programming Current Monitoring Resistor - R_{IMON}

Voltage at IMON pin $V_{(IMON)}$ represents the voltage proportional to load current. This can be connected to an ADC of the downstream system for health monitoring of the system. The $R_{(IMON)}$ need to be configured based on the maximum input voltage range of the ADC used. $R_{(IMON)}$ is set using Equation 13.

$$R_{(IMON)} = \frac{V_{(IMONmax)}}{I_{(LIM)} \times 52 \times 10^{-6}} \ k\Omega \quad (13)$$

For $I_{(LIM)}$ = 5 A, and considering the operating range of ADC from 0 V to 5 V, $V_{(IMONmax)}$ is 5 V and $R_{(IMON)}$ is determined by:

$$R_{(IMON)} = \frac{5}{5 \times 52 \times 10^{-6}} = 19.23 \ k\Omega \quad (14)$$

Selecting $R_{(IMON)}$ value less than determined by Equation 14 ensures that ADC limits are not exceeded for maximum value of load current.

If the IMON pin voltage is not being digitized with an ADC, $R_{(IMON)}$ can be selected to produce a 1V/1A voltage at the IMON pin, using Equation 13.

Choose closest 1 % standard value: 19.1 kΩ.

If current monitoring up to $I_{(FASTRIP)}$ is desired, $R_{(IMON)}$ can be reduced by a factor of 1.6, as in Equation 5.

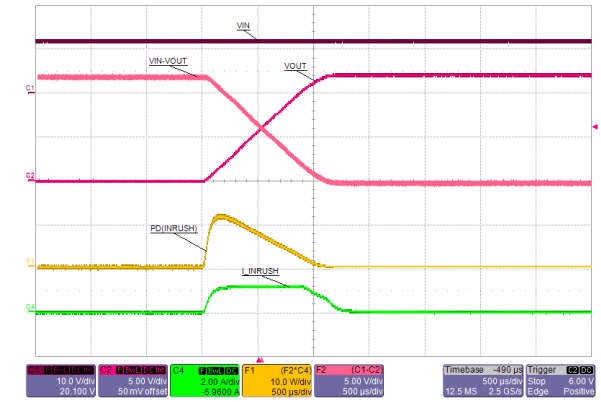
10.2.1.2.5 Setting Output Voltage Ramp time (t_{dVdT})

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor $C_{(dVdT)}$ needed is calculated considering the two possible cases:

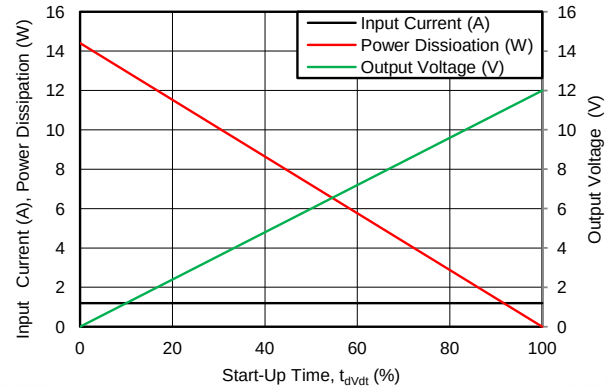
10.2.1.2.5.1 Case1: Start-up Without Load: Only Output Capacitance $C_{(OUT)}$ Draws Current During Start-up

During start-up, as the output capacitor charges, the voltage difference across the internal FET decreases, and the power dissipated decreases as well. Typical ramp-up of output voltage $V_{(OUT)}$ with inrush current limit of 1.2A and power dissipated in the device during start-up is shown in Figure 53. The average power dissipated in the device during start-up is equal to area of triangular plot (red curve in Figure 54) averaged over t_{dVdT}.



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $C_{(OUT)}$=100 µF

Figure 53. Start-up Without Load



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $C_{(OUT)}$=100 µF

Figure 54. $P_{D(INRUSH)}$ Due to Inrush Current

For TPS25940 device, the inrush current is determined as,

$$I = C \times \frac{dV}{dT} \Rightarrow I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (15)$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (16)$$

Equation 16 assumes that load does not draw any current until the output voltage has reached its final value.

10.2.1.2.5.2 Case 2: Start-up With Load: Output Capacitance $C_{(OUT)}$ and Load Draws Current During Start-up

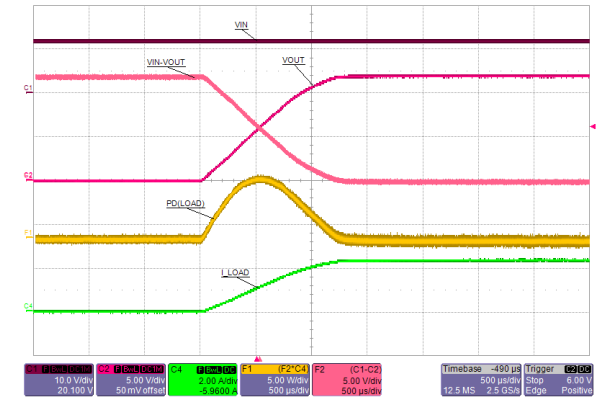
When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load $R_{L(SU)}$ during start-up, load current ramps up proportionally with increase in output voltage during t_{dVdT} time. Typical ramp-up of output voltage, Load current and power dissipation in the device is shown in Figure 55 and power dissipation with respect to time is plotted in Figure 56. The additional power dissipation during start-up phase is calculated as follows.

$$(V_I - V_O)(t) = V_{(IN)} \times \left(1 - \frac{t}{t_{dVdT}}\right) \quad (17)$$

$$I_L(t) = \left(\frac{V_{(IN)}}{R_{L(SU)}}\right) \times \frac{t}{t_{dVdT}} \quad (18)$$

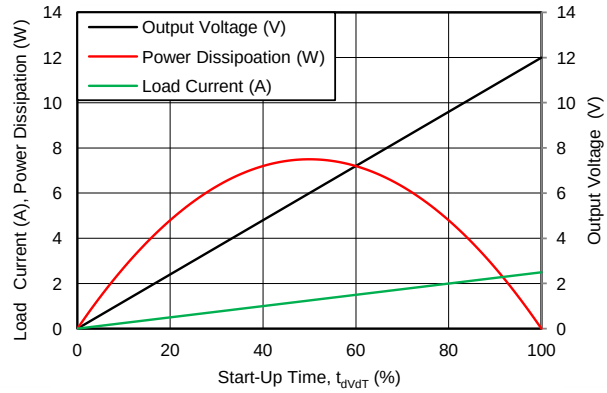
Where $R_{L(SU)}$ is the load resistance present during start-up. Average energy loss in the internal FET during charging time due to resistive load is given by:

$$W_t = \int_0^{tdVdT} V_{(IN)} \times \left(1 - \frac{t}{t_{dVdT}}\right) \times \left(\frac{V_{(IN)}}{R_{L(SU)}} \times \frac{t}{t_{dVdT}}\right) dt \quad (19)$$



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $R_{L(SU)}$ = 4.8 Ω

Figure 55. Start-up With Load



$V_{(IN)}$ = 12 V $C_{(dVdT)}$ = 1 nF $R_{L(SU)}$ = 4.8 Ω

Figure 56. $P_{D(LOAD)}$ in Load During Start-up

On solving Equation 19 the average power loss in the internal FET due to load is:

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (20)$$

Total power dissipated in the device during startup is:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (21)$$

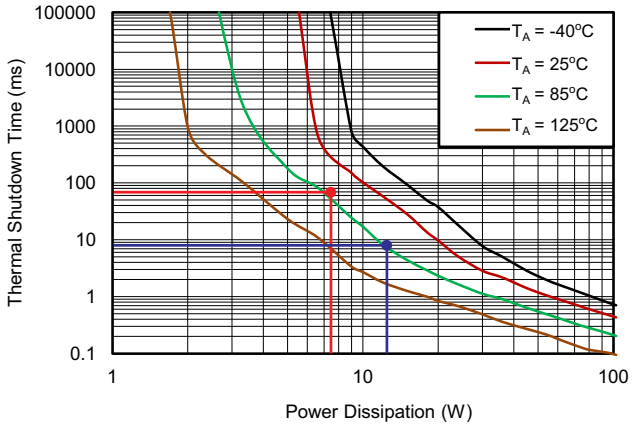
Total current during startup is given by:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (22)$$

If $I_{(STARTUP)} > I_{(LIM)}$, the device limits the current to $I_{(LIM)}$ and the current limited charging time is determined by:

$$t_{dVdT(current\ limited)} = C_{(OUT)} \times \frac{V_{(IN)}}{I_{(LIM)}} \quad (23)$$

The power dissipation, with and without load, for selected start-up time should not exceed the shutdown limits as shown in Figure 57.



Taken on 2-Layer board, 2oz.(0.08-mm thick) with GND plane area: 14 cm2 (Top) and 20 cm2 (bottom)

Figure 57. Thermal Shutdown Limit Plot

For the design example under discussion,

Select ramp-up capacitor $C_{(dVdT)}$ = 1nF, using Equation 2.

$$t_{dvdt} = 8.3 \times 10^{4} \times 12 \times 1 \times 10^{-9} = 0.996\text{ms} = \sim 1\text{ms} \quad (24)$$

The inrush current drawn by the load capacitance ($C_{(OUT)}$) during ramp-up using Equation 3.

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{1 \times 10^{-3}}\right) = 1.2\text{ A} \quad (25)$$

The inrush Power dissipation is calculated, using Equation 16.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 1.2 = 7.2\text{ W} \quad (26)$$

For 7.2 W of power loss, the thermal shut down time of the device should not be less than the ramp-up time t_{dVdT} to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 57 at T_A = 85°C, for 7.2 W of power the shutdown time is ~60 ms. So it is safe to use 1 ms as start-up time without any load on output.

Considering the start-up with load 4.8 Ω, the additional power dissipation, when load is present during start up is calculated, using Equation 20.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{12 \times 12}{4.8} = 5\text{ W} \quad (27)$$

The total device power dissipation during start up is:

$$P_{D(STARTUP)} = (7.2 + 5) = 12.2\text{ W} \quad (28)$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 12.2 W is close to 7.5 ms. It is safe to have 30% margin to allow for variation of system parameters such as load, component tolerance, and input voltage. So it is well within acceptable limits to use the 1 nF capacitor with start-up load of 4.8 Ω.

If there is a need to decrease the power loss during start-up, it can be done with increase of $C_{(dVdT)}$ capacitor.

To illustrate, choose $C_{(dVdT)}$ = 1.5 nF as an option and recalculate:

$$t_{dvdt} = 1.5\text{ms} \quad (29)$$

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{1.5 \times 10^{-3}}\right) = 0.8\text{ A} \quad (30)$$

$$P_{D(INRUSH)} = 0.5 \times 12 \times 0.8 = 4.8\text{ W} \quad (31)$$

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \left(\frac{12 \times 12}{4.8}\right) = 5\text{ W} \quad (32)$$

$$P_{D(STARTUP)} = 4.8 + 5 = 9.8\ W \quad (33)$$

From thermal shutdown limit graph at T_A = 85°C, the shutdown time for 10 W power dissipation is ~17 ms, which increases the margins further for shutdown time and ensures successful operation during start up and steady state conditions.

The spreadsheet tool available on the web can be used for iterative calculations.

10.2.1.2.6 Programing the Power Good Set Point

As shown in Figure 52, R_4 and R_5 sets the required limit for PGOOD signal as needed for the downstream converters. Considering a power good threshold of 11 V for this design, the values of R_4 and R_5 are calculated using Equation 34.

$$V_{(PGTH)} = 0.99 \times \left(1 + \frac{R_4}{R_5}\right) \quad (34)$$

It is recommended to have high values for these resistors to limit the current drawn from the output node. Choosing a value of R_4 = 475 kΩ, R_5 = 47 kΩ provides $V_{(PGTH)}$ = 11 V.

10.2.1.2.7 Support Component Selections - R_6, R_7 and C_{IN}

Reference to application schematics, R_6 and R_7 are required only if PGOOD and $\overline{FLT}$ are used; these resistors serve as pull-ups for the open-drain output drivers. The current sunk by each of these pins should not exceed 10 mA (refer to the Absolute Maximum Ratings table). C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for $C_{(IN)}$.

10.2.1.3 Application Curves

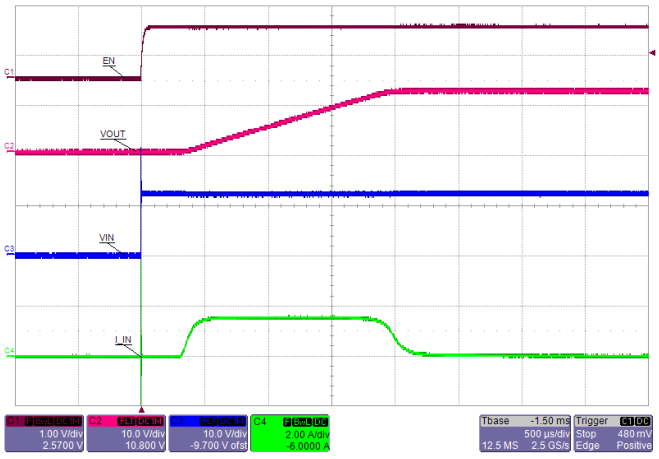


Figure 58. Hot-Plug Start-Up: Output Ramp Without Load on output

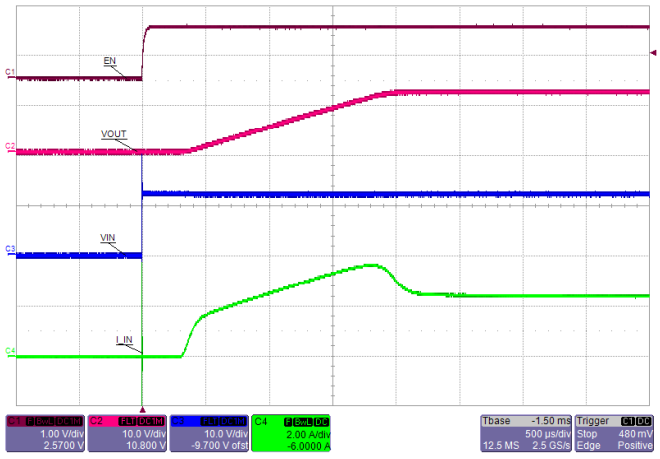


Figure 59. Hot-Plug Start-Up: Output Ramp With Start-up load of 4.8Ω

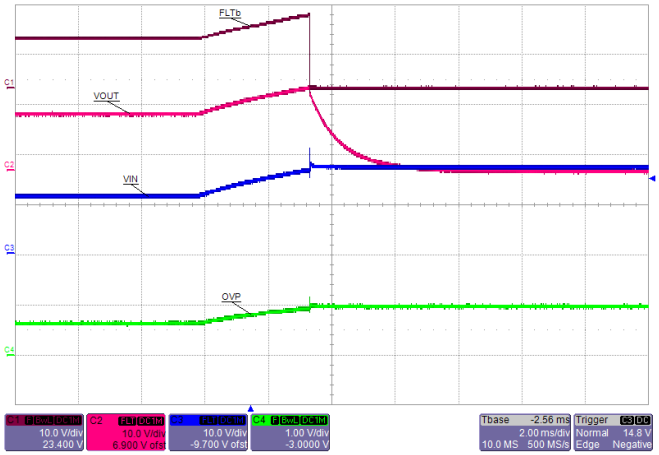


Figure 60. Overvoltage Shutdown

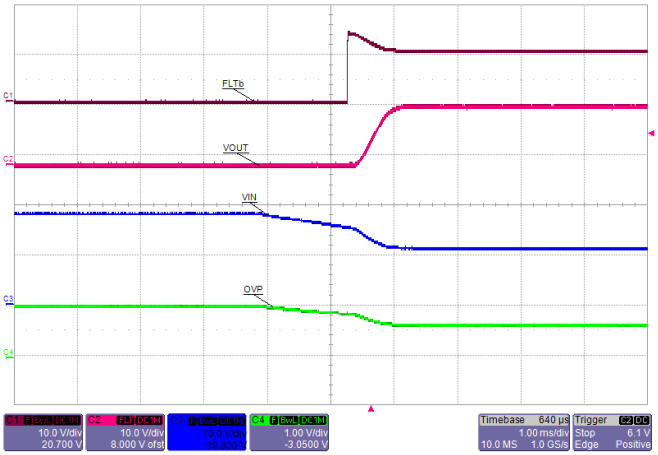


Figure 61. Overvoltage Recovery

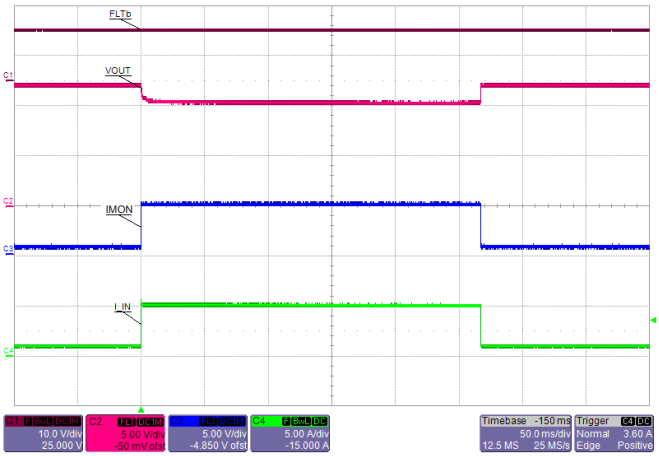


Figure 62. Over Load: Step Change in Load from 12Ω to 2Ω and Back

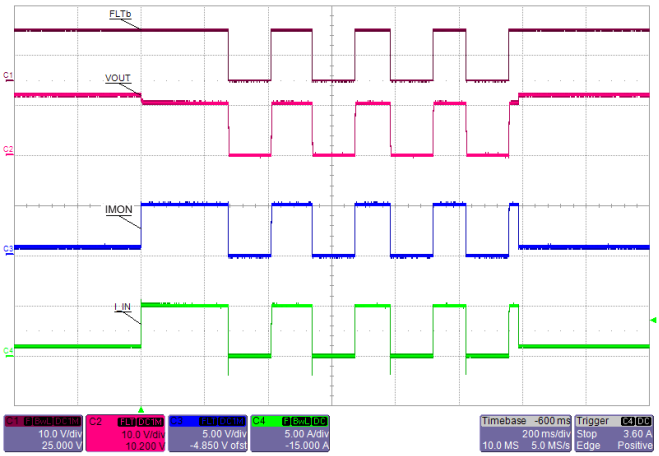


Figure 63. Overload Condition: Auto Retry and Recovery - TPS25940A

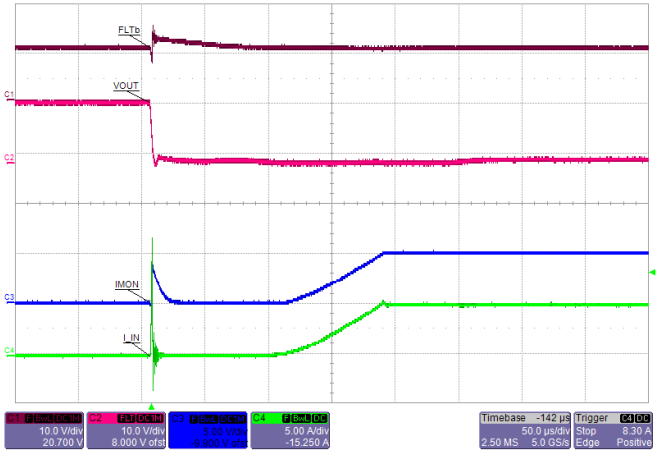


Figure 64. Hot Short: Fast Trip and Current Regulation

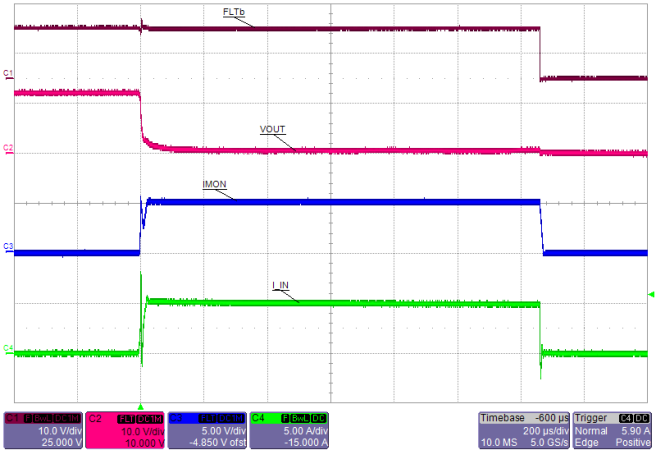


Figure 65. Hot Short: Latched - TPS25940L

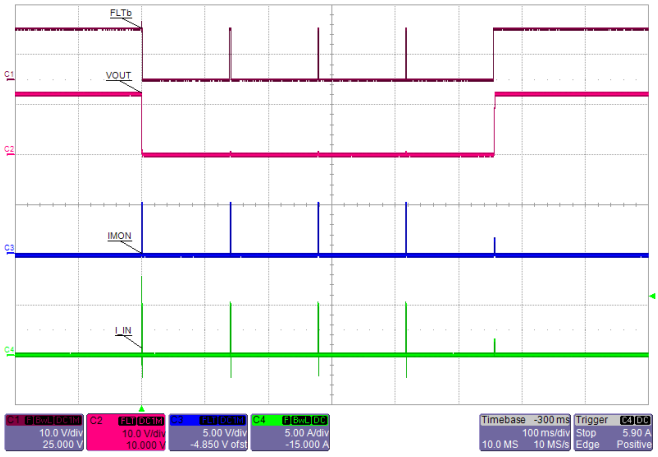


Figure 66. Hot Short: Auto-Retry and Recovery from Short Circuit - TPS25940A

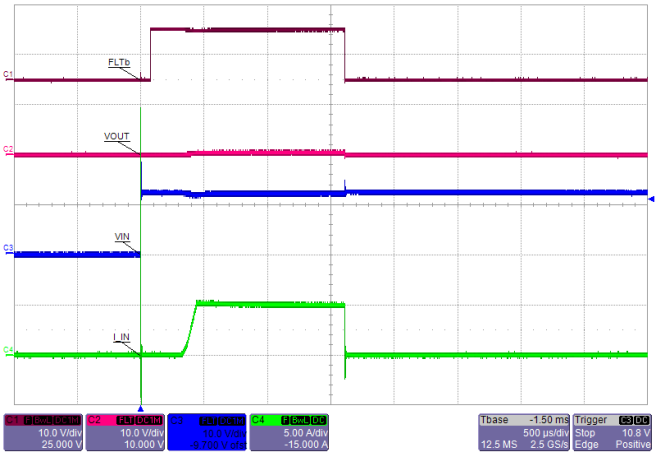


Figure 67. Hot Plug-in with Short on Output: Latched - TPS25940L

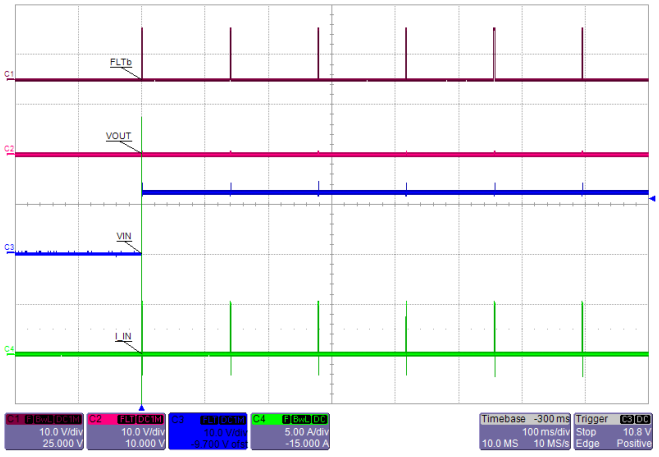


Figure 68. Hot Plug-in with Short on Output: Auto-Retry - TPS25940A

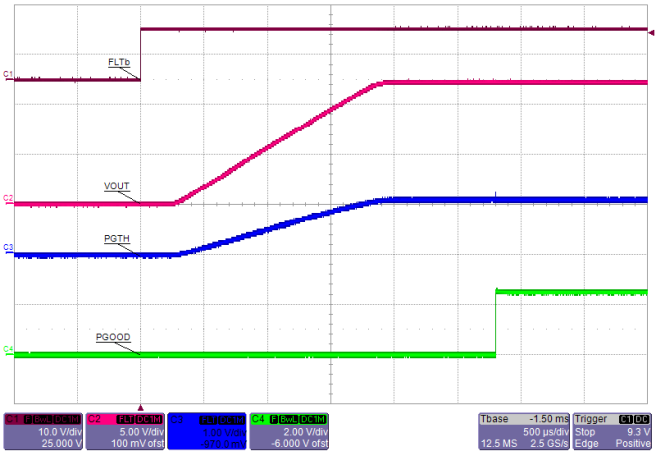


Figure 69. Power Good Response During Turn-ON

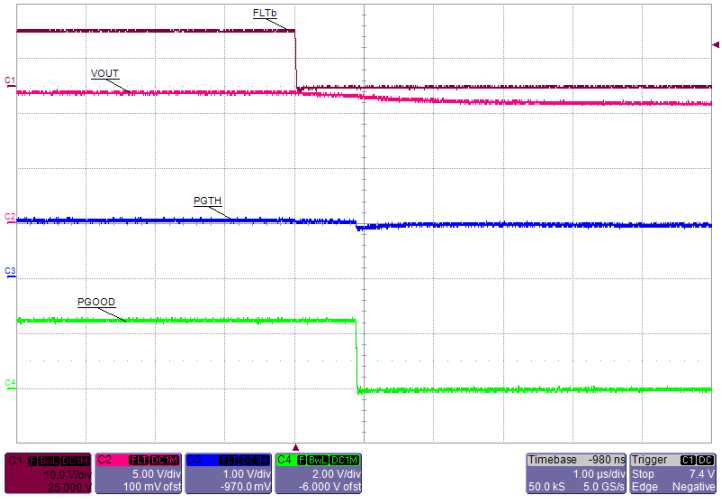


Figure 70. Power Good Response During Turn-OFF

10.3 System Examples

10.3.1 Power Failure Protection and Data Retention in SSDs

For enterprise and Industrial SSDs, it is necessary to have hold-up circuit and capacitor bank to ensure that critical user data is never lost during power-failure to the drive. The power-failure event could be due to momentary loss of power regulation (transient brown-out condition) or due to loss of power when drive is hot-plugged out.

The TPS25940 continuously monitors the supply voltage at EN/UVLO pin and swiftly disconnects the input bus from output when the voltage drops below a predefined threshold (power fail detection). The TPS25940 also monitors the reverse voltage from IN to OUT and when it exceeds -10 mV, it stops the flow of reverse current. In addition, it provides an instant warning signal ($\overline{FLT}$) to the SSD controller to initiate the data hardening process. Its swift true reverse blocking feature reacts in 1 µs (typical) ensuring that the capacitor bank charge is retained. This helps the drive to have power for longer time to harden data and reduces the capacitance required in the hold-up bank, saving system cost.

The typical application diagram and application schematic of TPS25940 usage for enterprise SSD are shown in Figure 71 and Figure 72

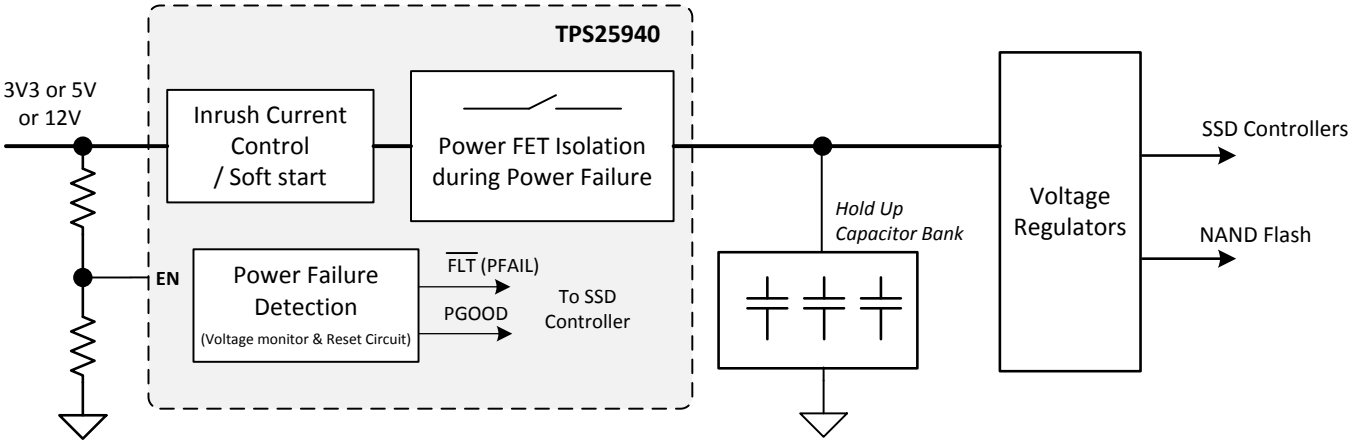
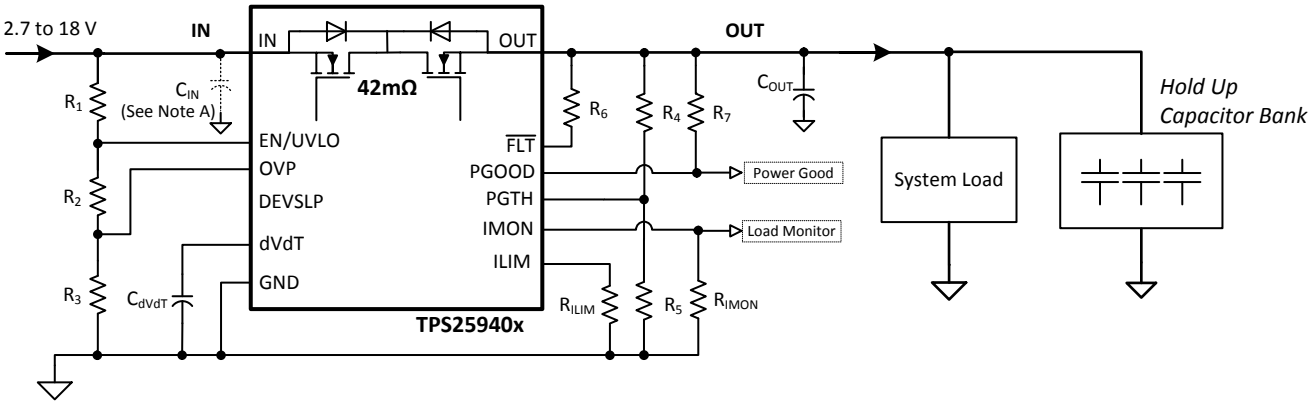


Figure 71. Power Circuit Block Diagram of Enterprise and Industrial SSDs

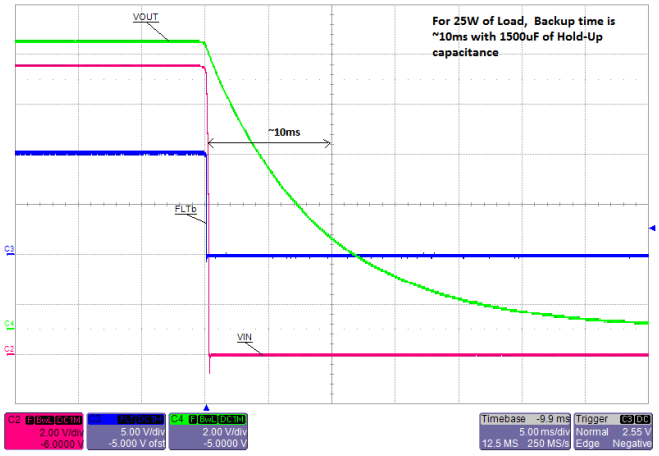


A. C_{IN}: Optional and only for noise suppression.

Figure 72. Enterprise SSD – Holdup Capacitor Implementation using TPS25940

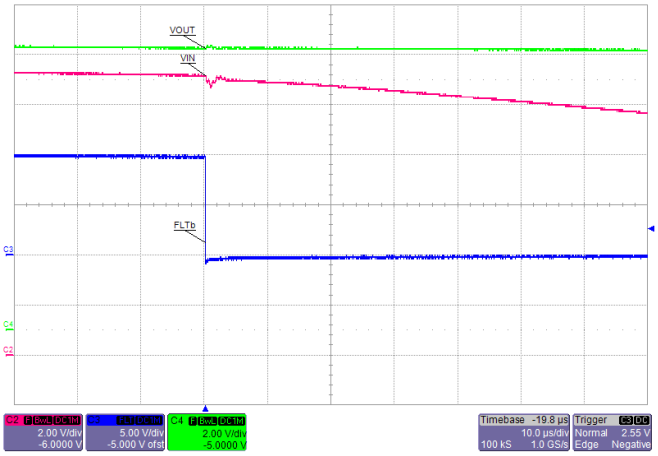
The oscilloscope plots demonstrating the true reverse blocking, fast turn-off and $\overline{FLT}$ signal delay are shown in Figure 73 through Figure 75.

System Examples (continued)



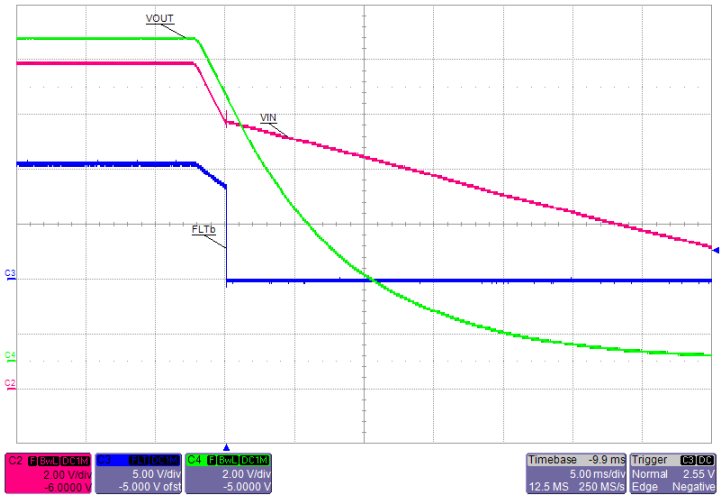
$V_{(IN)}$ = 12V $C_{(OUT)}$ = 1500 µF R_L = 5.6 Ω

Figure 73. Hot-Plug Out Condition



$V_{(IN)}$ = 12V $C_{(OUT)}$ = 1500 µF R_L = 5.6 Ω

Figure 74. Hot-Plug Out Condition: $\overline{\text{FLT}}$ Delay



$V_{(IN)}$ = 12V $C_{(OUT)}$ = 1500 µF R_L = 5.6 Ω

Figure 75. Standard Power Shutdown or Brownout Conditions

10.3.2 Boost Power Rail Configuration for Data Retention in Enterprise SSDs

In certain enterprise SSD architectures, the hold-up capacitor voltage is boosted to value higher than the input bus voltage to optimize the storage capacitor bank. A typical boosted hold-up voltage ranges from 12 V to 18 V. A typical power circuit block diagram is shown in Figure 76. For these applications, TPS25940 provides quick and smooth changeover of the power from main input bus to boosted backup voltage.

System Examples (continued)

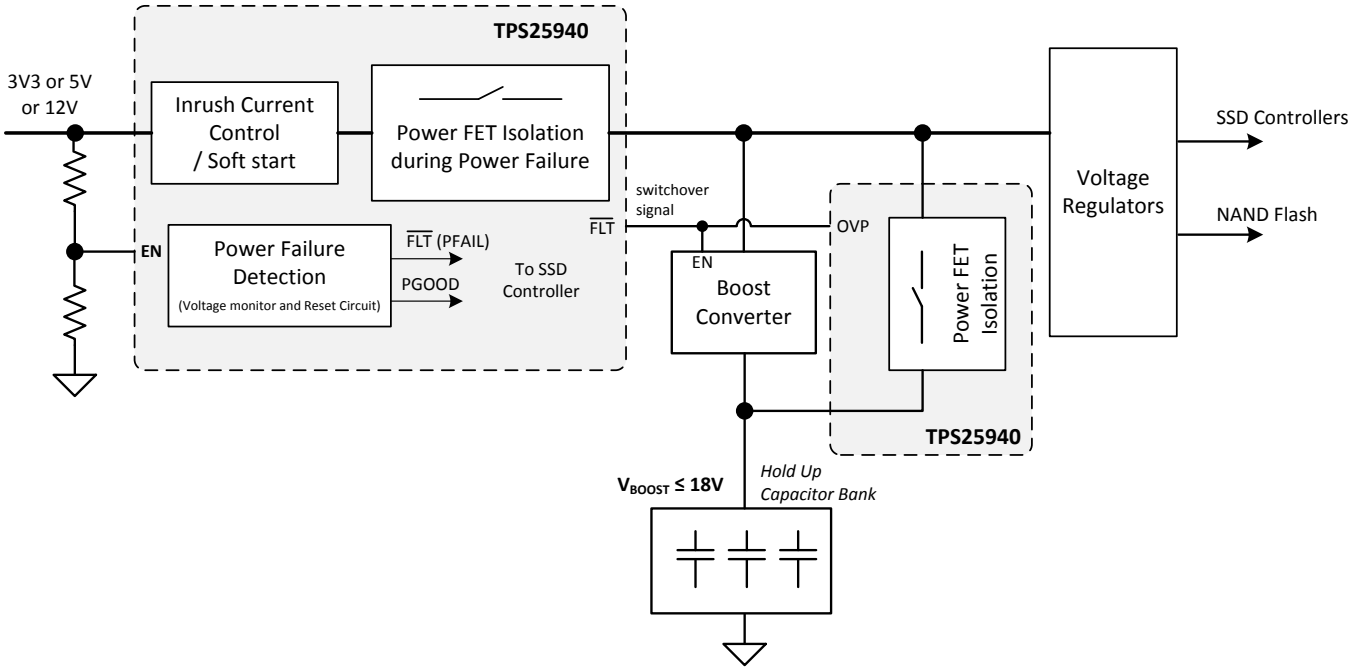
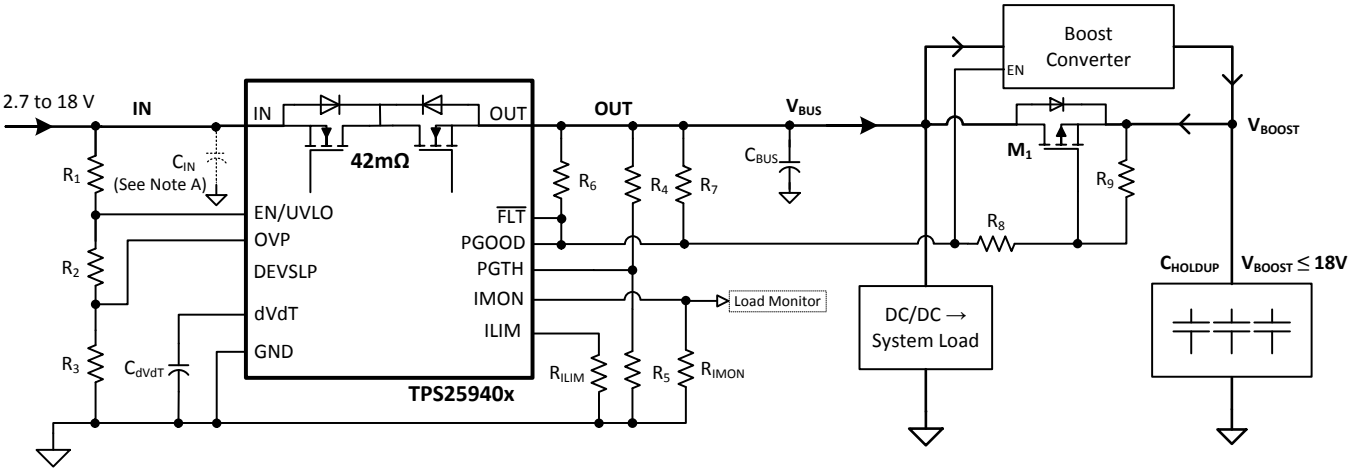


Figure 76. Power Circuit Block Diagram with Boosted Backup Power for Enterprise SSD

A typical application schematic for implementation of boosted backup power configuration is shown in Figure 77. During startup TPS25940 provides the inrush current control to charge up the $C_{(BUS)}$ as well as $C_{(HOLDUP)}$ close to $V_{(IN)}$. Once $V_{(BUS)}$ reaches the programmed PGOOD threshold, the boost converter is enabled to charge $C_{(HOLDUP)}$ to $V_{(BOOST)}$. When $V_{(IN)}$ fails, TPS25940 detects power failure and asserts the fault signal ($\overline{FLT}$), which in turn disables the boost converter and shorts $V_{(BOOST)}$ to $V_{(BUS)}$, through M_1. The $\overline{FLT}$ signal can be interfaced to SSD controller to initiate the data hardening process. If current limit protection is desired during data hardening process (when holdup capacitor is supplying system bus), M_1 can be replaced by another TPS25940.

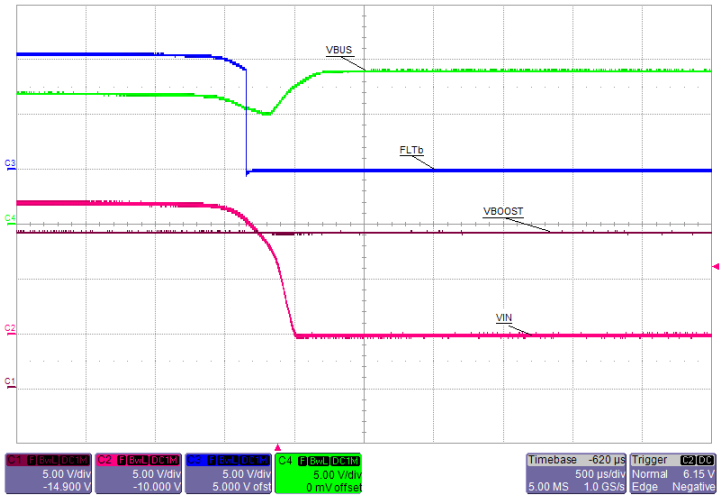
The oscilloscope plot demonstrating change over from Main (12 V) to Boosted backup power (14.5 V) is shown in Figure 78.



A. C_{IN}: Optional and only for noise suppression.

Figure 77. Enterprise SSDs: Boosted Backup Power Multiplexing Circuit Implementation

System Examples (continued)



$V_{(IN)}$ = 12 V $V_{(BOOST)}$ = 14.5 V $C_{(BUS)}$ = 150 µF

$P_{(LOAD)}$ = 12.5 W $V_{(IN-UVLO-low)}$ = 10.2 V $C_{(dVdT)}$ = 1 nF

Figure 78. Brownout (Power Fail) Condition: Switch over to Boosted Backup Power

11 Power Supply Recommendations

The TPS25940 device is designed for supply voltage range of 2.7 V ≤ V_{IN} ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with Equation 35.

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (35)$$

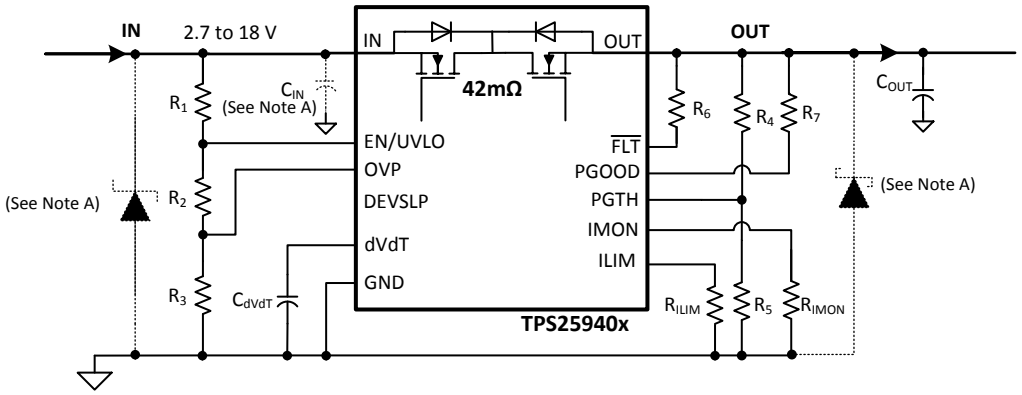
Where:

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current,
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Transient Protection (continued)

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 79.



A. Optional components needed for suppression of transients

Figure 79. Circuit Implementation With Optional Protection Components

11.2 Output Short-Circuit Measurements

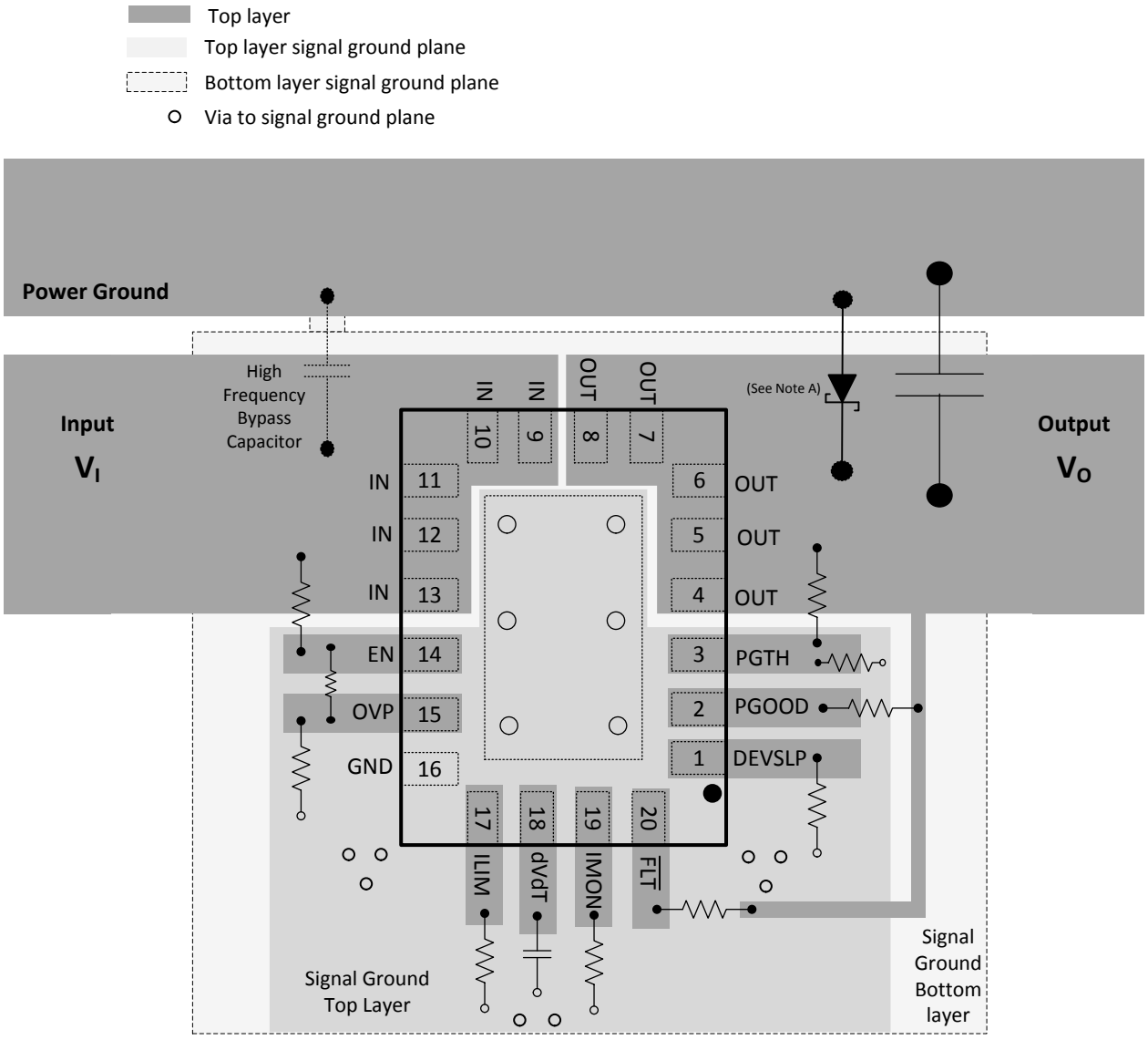
It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

12 Layout

12.1 Layout Guidelines

- For all applications, a 0.1-uF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 80 for a PCB layout example.
- High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.
- Low current signal ground (SGND), which is the reference ground for the device should be a copper plane or island.
- Locate all TPS25940 support components: $R_{(ILIM)}$, C_{dVdT}, $R_{(IMON)}$, and resistors for UVLO and OVP, close to their connection pin. Connect the other end of the component to the SGND with shortest trace length.
- The trace routing for the R_{ILIM} and $R_{(IMON)}$ components to the device should be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces should not have any coupling to switching signals on the board.
- The SGND plane must be connected to high current ground (main power ground) at a single point, that is at the negative terminal of input capacitor
- Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.
- Thermal Considerations: When properly mounted the PowerPAD™ package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. The PowerPAD is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Refer to Technical Briefs: PowerPad™ Thermally Enhanced Package (TI literature Number SLMA002) and PowerPAD™ Made Easy (TI Literature Number SLMA004) or more information on using this PowerPAD™ package
- The thermal via land pattern specific to TPS25940 can be downloaded from device webpage
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

12.2 Layout Example



A. Optional: Needed only to suppress the transients caused by inductive load switching

Figure 80. Board Layout

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS25940A	Click here	Click here	Click here	Click here	Click here
TPS25940L	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

DevSleep, SATA are trademarks of The Serial ATA International Organization (SATA-IO).
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

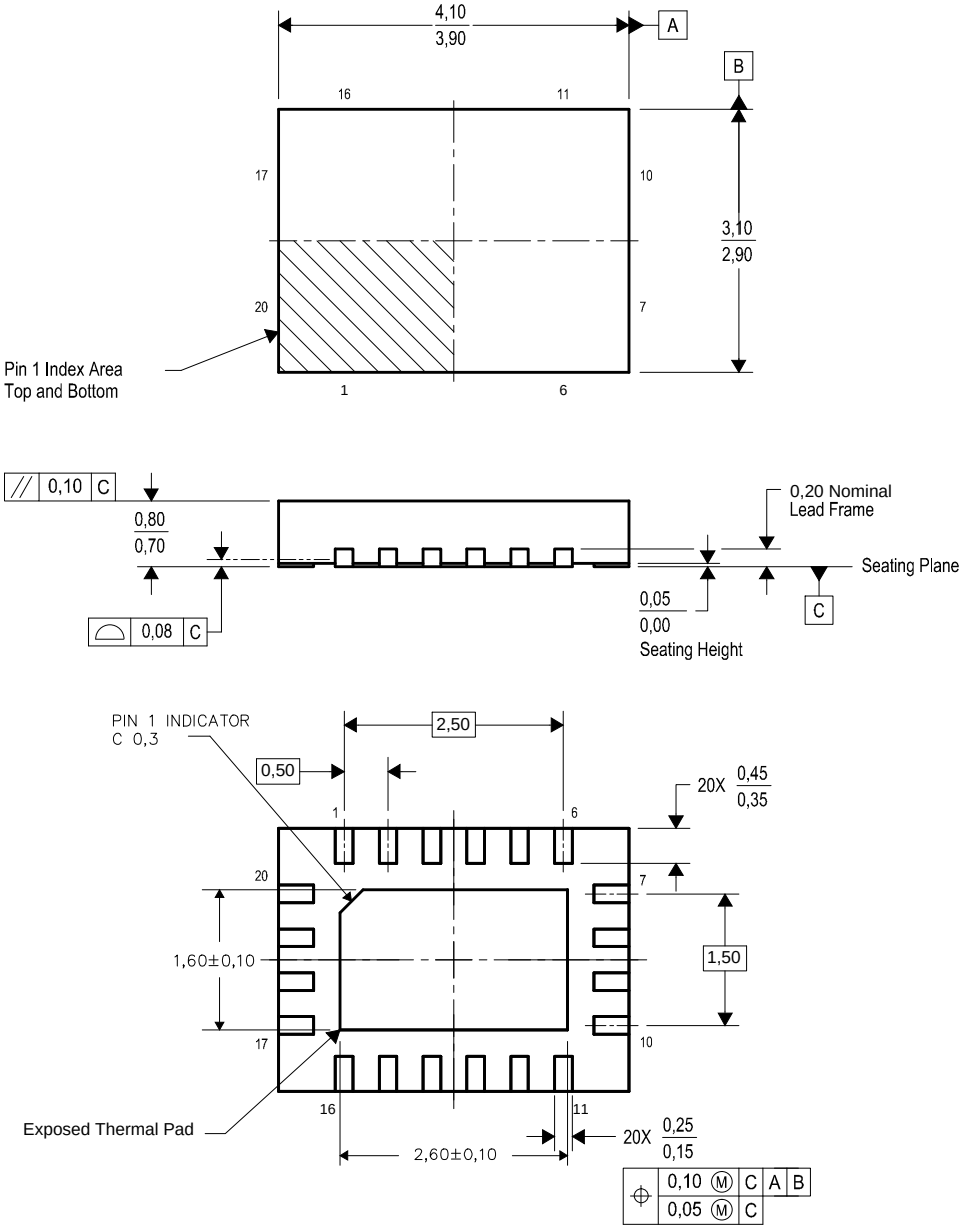
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RVC0020A

WQFN - 0.8 mm max height

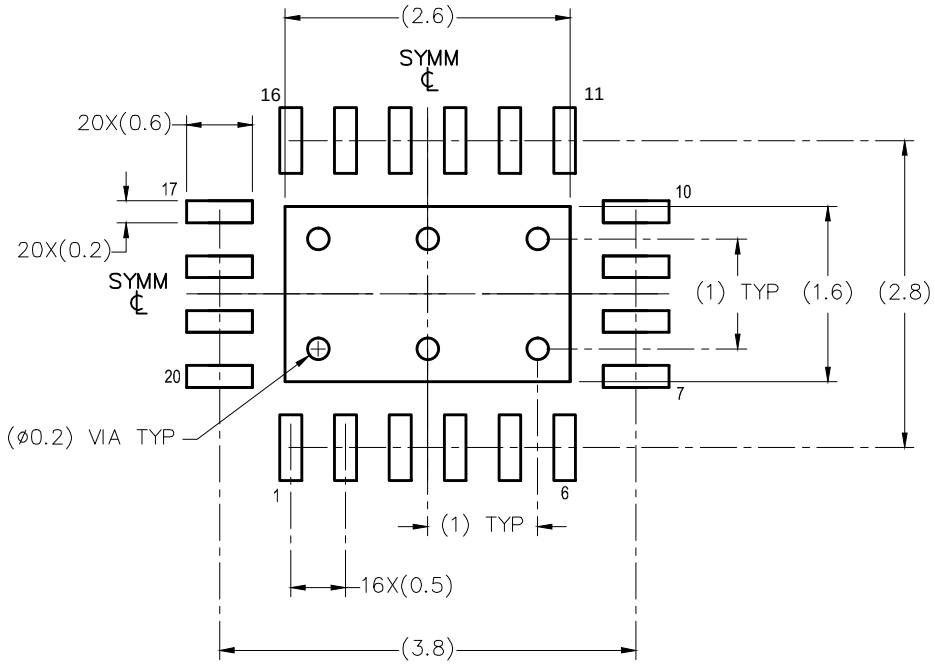
WQFN



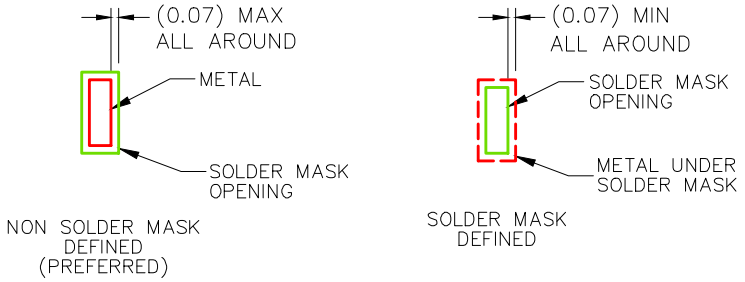
4219150/A 07/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE : 15X

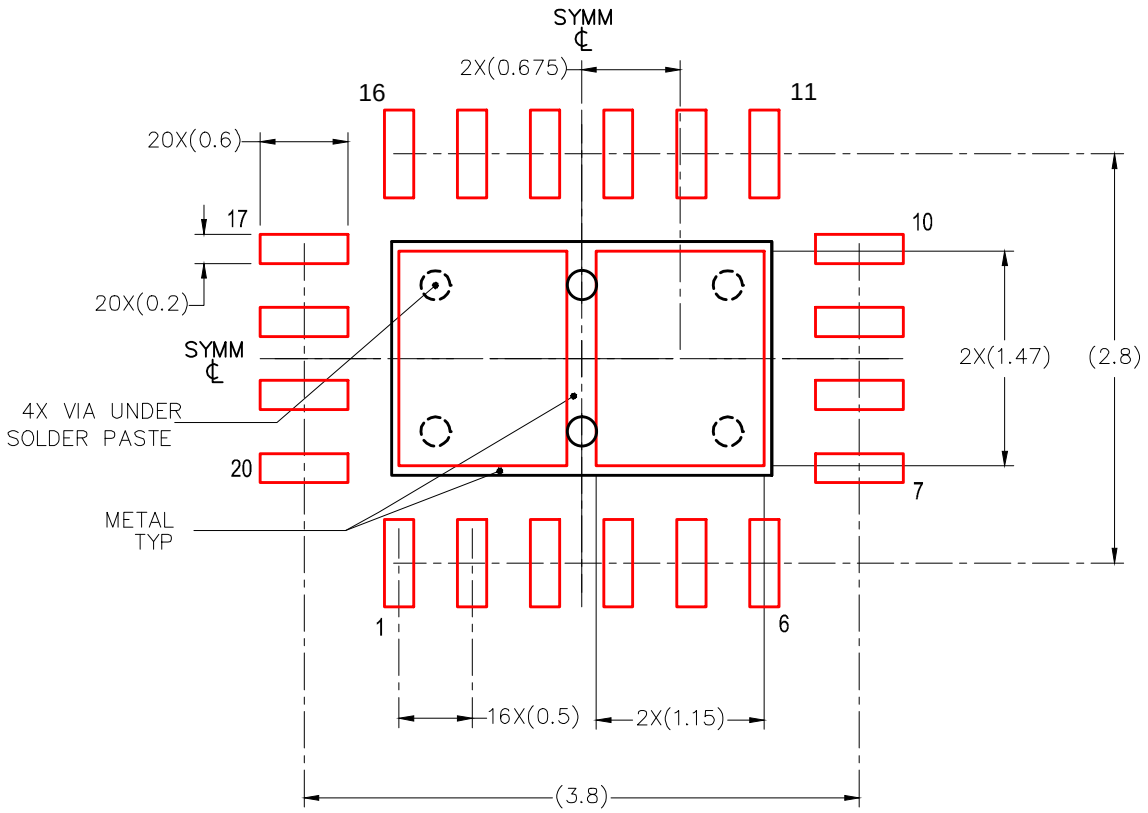


SOLDER MASK DETAILS

4219150/A 07/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE : 20X

4219150/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

3-Dec-2015

PACKAGING INFORMATION

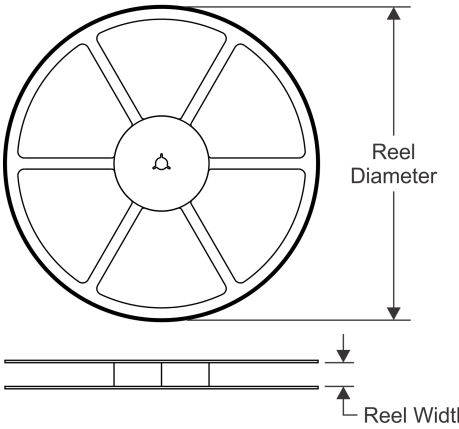
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25940ARVCR	ACTIVE	WQFN	RVC	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25940A	Samples
TPS25940ARVCT	ACTIVE	WQFN	RVC	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25940A	Samples
TPS25940LRVCR	ACTIVE	WQFN	RVC	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25940L	Samples
TPS25940LRVCT	ACTIVE	WQFN	RVC	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25940L	Samples
TPS25940XEVM-635	PREVIEW			0	1	TBD	Call TI	Call TI			

PACKAGE MATERIALS INFORMATION

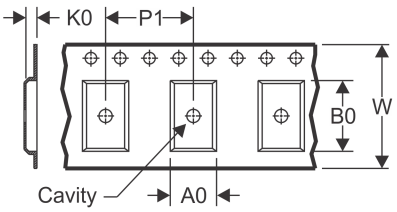
23-Mar-2015

TAPE AND REEL INFORMATION

REEL DIMENSIONS

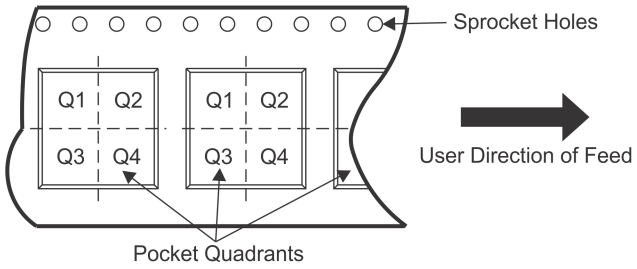


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



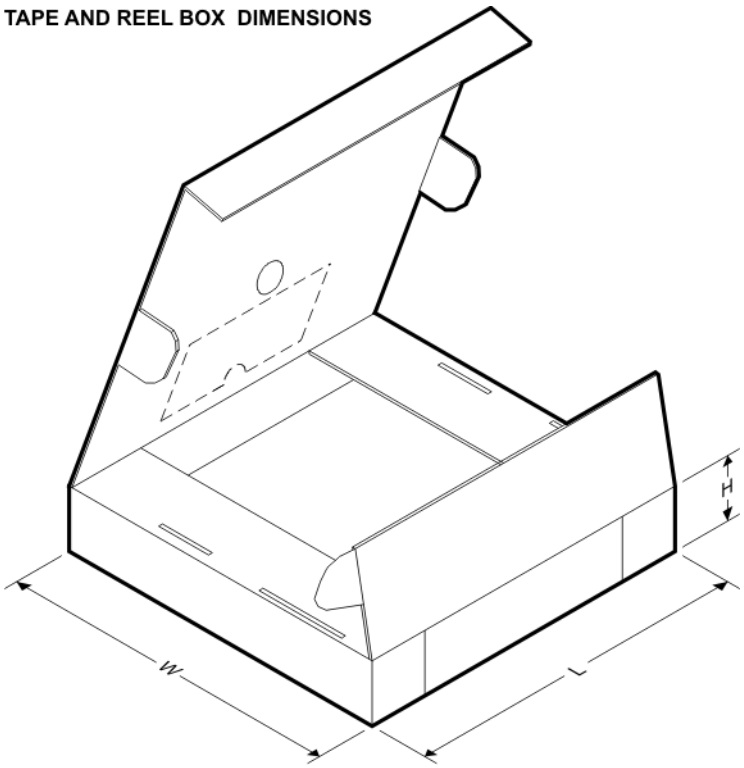
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25940ARVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25940ARVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25940LRVCR	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS25940LRVCT	WQFN	RVC	20	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

23-Mar-2015

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25940ARVCR	WQFN	RVC	20	3000	367.0	367.0	35.0
TPS25940ARVCT	WQFN	RVC	20	250	210.0	185.0	35.0
TPS25940LRVCR	WQFN	RVC	20	3000	367.0	367.0	35.0
TPS25940LRVCT	WQFN	RVC	20	250	210.0	185.0	35.0