APPROVAL SHEET

RF Switch Series – RoHS Compliance

DP10T MIPI Switch

Halogens Free Product

Any 2G/3G/4G Band for TRx System

P/N: RFASWY581CTF03

Approval Sheet

FEATURES

- Low Insertion Loss and Low Distortion
- Broadband frequency range：0.4 to 2.7 GHz
- High Isolation and linearity
- Integrated MIPI RFFE Slave Controller
- High ESD tolerance of 2kV HBM at all pins
- Small LGA package(18-pin, 2.4 x 2.0 x 0.64 mm^3)
- **M**oisture **S**ensitive **L**evel 3 (MSL3)
- High ESD tolerance of 2kV HBM at all pins

Description

- The RFASWY581CTF03 is a dual Single Pole, Five Throw (2XSP5T) antenna switch with an integrated Mobile Industry Processor Interface (MIPI) controller. Using an advanced switching technology, the RFASWY581CTF03 maintains low insertion and high isolation, which makes it an ideal choice for UMTS, CDMA2000, EDGE, GSM, and LTE applications.

- The design integrated five low loss TRX ports. The switch also has an excellent $2^{nd}/3^{rd}$ Order Intermodulation Distortion (IMD2/IMD3) performance.

- Switching is controlled by the MIPI decoder and High ESD tolerance of 2kV HBM at all pins.

- No blocking capacitor requirements on the RF paths as long as no DC voltage are applied. The RFASWY581CTF03 is manufactured in a compact, 2.4 x 2.0 x 0.64 mm^3 package.

- The functional block diagram is shown in Figure 1. The pin assignment and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Application

- 2G/3G/4G multimode cellular handsets (LTE, UMTS, CDMA2000, EDGE, GSM, TDD-LTE, TD-SCDMA)
- Carrier aggregation diversity

Block Diagram and Pin Out (Top View)

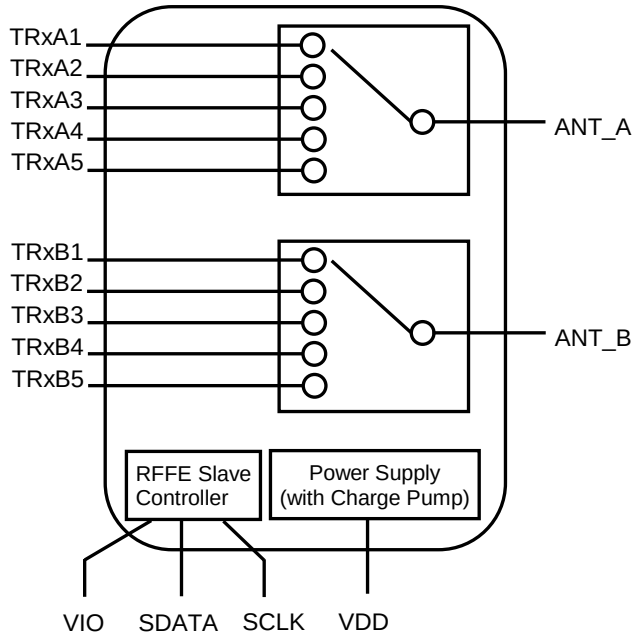


Figure 1. RFASWY581CTF03 Block Diagram

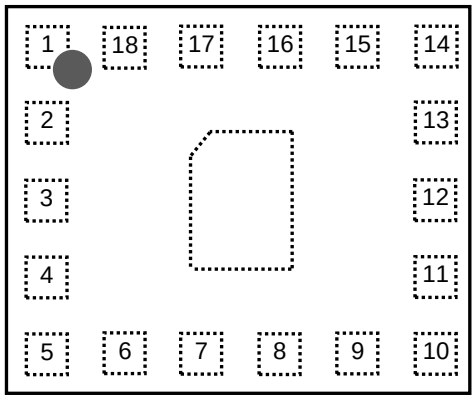


Figure 2. RFASWY581CTF03 Pin assignment

Approval Sheet

Table 1. RFASWY581CTF03 Pin Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	TRxB2	Bank B RF path 2	10	NC	Not Connected
2	TRxB3	Bank B RF path 3	11	TRxA5	Bank A RF path 5
3	TRxB4	Bank B RF path 4	12	TRxA4	Bank A RF path 4
4	TRxB5	Bank B RF path 5	13	TRxA3	Bank A RF path 3
5	NC	Not Connected	14	TRxA2	Bank A RF path 2
6	VDD	DC power supply	15	TRxA1	Bank A RF path 1
7	VIO	RFFE Interface Power Supply	16	ANT_A	Bank A Antenna port
8	SDATA	RFFE Data input/output	17	ANT_B	Bank B Antenna port
9	SCLK	RFFE Clock Input	18	TRxB1	Bank B RF path 1

Note 1：Bottom ground paddles must be connected to ground.

Application Circuit

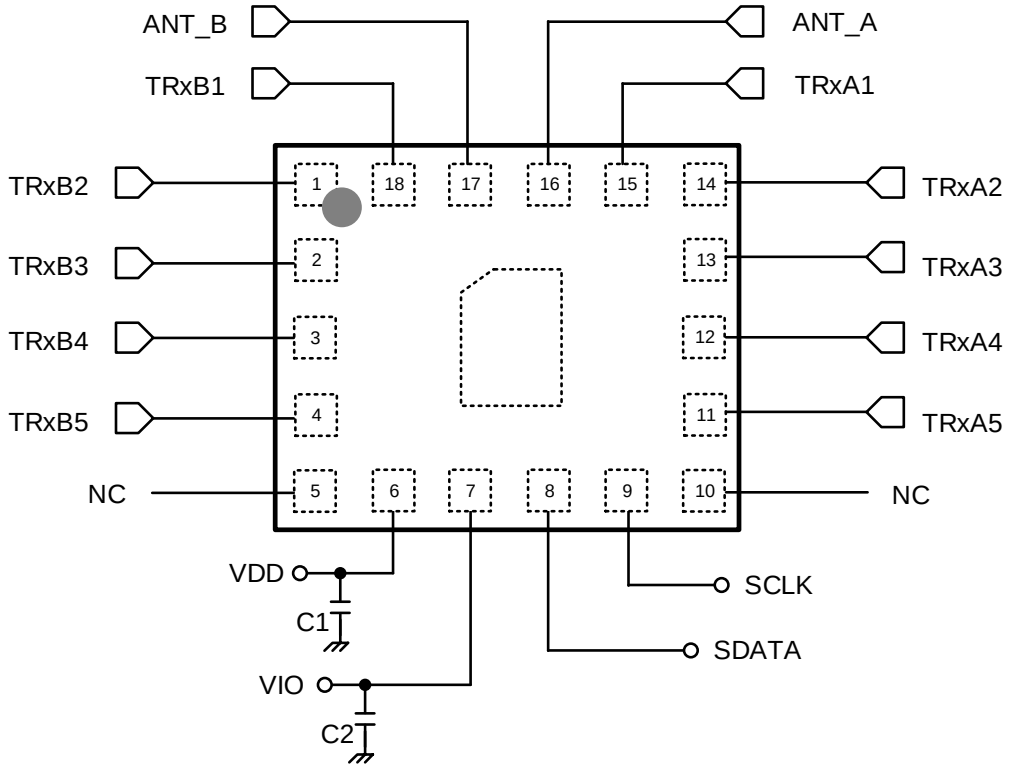


Figure 3. RFASWY581CTF03 Application Circuit

Note: No DC Blocking capacitors are required for all RF ports unless DC is biased externally.

Parts List

Parts No.	Value
C1-C2	0.1 μF

Table 2. RFASWY581CTF03 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	VDD	-0.3	5.5	V
Interface Supply Voltage	VIO	-0.3	2.0	V
Control Input/ Output Voltage Range (SDATA, SCLK)	V_{IN_OUT}	-0.3	2.0	V
Maximum Control Output Current (SDATA)	I_{OUT}	-5	+5	mA
TRXx Input Power (f = 698 ~ 2690 MHz, 50Ω, CW)	PIN	-	30	dBm
Storage temperature	T_{STG}	-45	+125	°C
Operating temperature	T_{OP}	-30	+90	°C
HBM ESD Voltage, All Pins	V_{ESD}[1]	-	2000	V
MM ESD Voltage, All Pins	V_{ESD}[2]	-	190	V

Note 1 : Human Body Model ESD Voltage (HBM, JEITA EIAJ ED-4701)
Note 2 : Machine Model ESD Voltage (MM, JEITA EIAJ ED-4701)
Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrical and Mechanical Specifications

- The absolute maximum ratings of the RFASWY581CTF03 are provided in Table 2. Electrical specifications are provided in Tables 3 and 5.
- Figure 4, 5 and Table4 describes the RFASWY581CTF03 has four operating states.
- IMD2 and IMD3 test conditions for various frequencies are listed in Tables 6 and 7, respectively.
- Figure 6, 7, 8, 9 and Table8 show the important parameters for SCLK and SDATA required for proper operations of the Toshiba MIPI RFFE slave interface.
- Table 9 register mapping shows the list of the registers inside the RFASWY581CTF03.
- Table 10, 11 provides the switch control register.
- Table 12, 3 and 14 describes the detail information of RFFE status, power mode and trigger states, respectively.
- Figure 10 and Table 15 describes the solder land pad and dimensions.

Table 3. RFASWY581CTF03 DC Electrical Specifications (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD			4.8	V
Supply current, active mode (VDD=2.85V)	IDD		80		μA
Supply current, low power mode (VDD=2.85V)	IDD		9		μA
Interface supply voltage	VIO	1.65	1.80	1.95	V
Interface signal: High Low	SDATA	 0.8 × VIO 0		 VIO 0.2 × VIO	 V V
Control current: High Low		 -3 -3	 1 1	 10 3	 μA μA

Note 1 : Performance is guaranteed only under the conditions listed in this Table.

Operating States

The RFASWY581CTF03 has four operating states, which are ACTIVE, SHUTDOWN, STATUP and LOW POWER. The transitions between these four states are set writing the PWR_MODE register or VIO as shown in Figure 4. The internal circuit operations in each operating state are shown in Table 4.

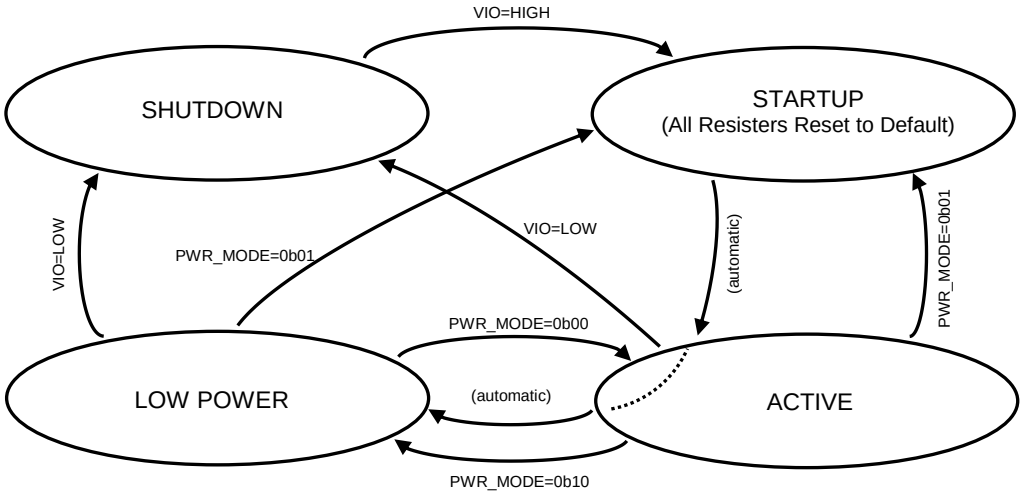


Figure 4. Slave State Diagram

Table 4. RFASWY581CTF03 Internal Operations (Note 1)

Operating State	RFFE Slave Controller	RF Switch Core	Charge Pump
SHUTSOWN	Inactive	Undetermined (Note1)	Off
STARTUP	All registers are set to Default value	Undetermined (Note1)	Off
ACTIVE	Active	Controllable by mipi-command	On
LOW POWER	Active	Undetermined (Note1)	Off

Note 1 : All switch are insufficiently On or Off as the Charge pump is not powered up.

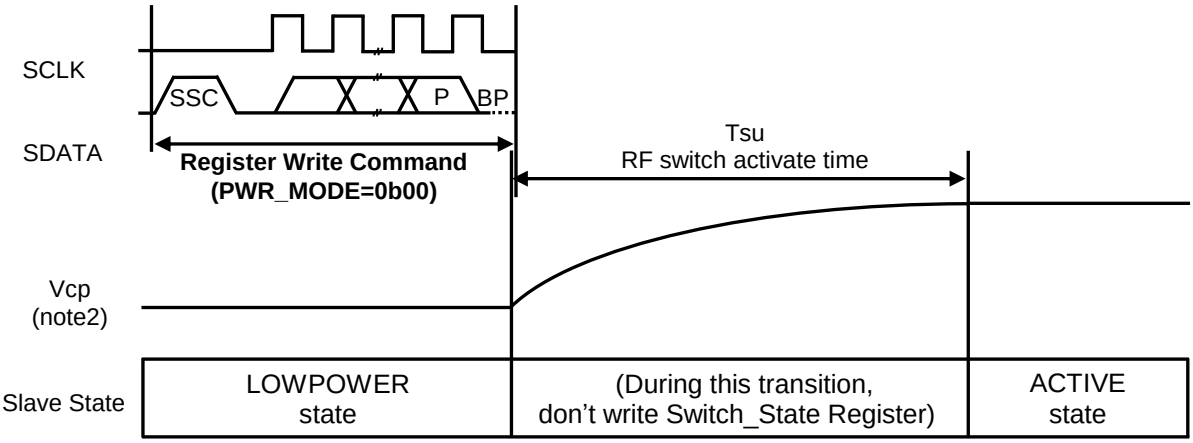


Figure 5. LOW POWER to AVTIVE Process

Note 2 : Vcp is the output voltage of internal charge-pump circuit. The Vcp traces in above figure are only image for illustrative purpose.

Table 5. RFASWY581CTF03 RF Electrical Specifications (Note 1)

(T_{op}= 25°C, VDD = 2.85 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
Operating frequency	f		0.4		2.7	GHz
Insertion loss (ANT_A to TRxA Ports ANT_B to TRxB Ports)	IL	400 to 960 MHz 1710 to 2170 MHz 2170 to 2700 MHz	- - -	0.45 0.60 0.75	0.65 0.80 0.95	dB dB dB
Isolation (ANT_A to TRxA Ports ANT_B to TRxB Ports)	Iso	400 to 960 MHz 1710 to 2170 MHz 2170 to 2700 MHz	28 20 17	32 24 21	- - -	dB dB dB
Isolation (ANT_A to TRxB Ports ANT_B to TRxA Ports)	Iso	400 to 960 MHz 1710 to 2170 MHz 2170 to 2700 MHz	36 28 25	41 33 29	- - -	dB dB dB
On state match	VSWR	Up to 2.7 GHz	-	1.5	2.0	-
TRXx harmonics	2fo, 3fo	PIN = +26 dBm, 5:1 VSWR, f = 400 to 2700 MHz	-	-	-90	dBc
2nd Order Intermodulation Distortion	IMD2	See test conditions in Table 6	-	-105	-	dBm
3rd Order Intermodulation Distortion	IMD3	See test conditions in Table 7	-	-110	-	dBm
Turn-on time	t_{ON}	From application of VDD and VIO	-	10	-	µs
Switching speed	t_S	Port to port	-	2	-	µs

Note 1 : Performance is guaranteed only under the conditions listed in this Table.

Table 6. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 7. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 8. Digital Interface Timing Specifications

(T_{op}= 25°C, VDD = 2.8 V, VIO=1.8V, Characteristic Impedance Z_O= 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Condition	Min.	Max.	Unit
Data Setup Time (Note 1)	T_S	See the Figure 6, input Tr/Tf = 3.5 to 6.5ns	1	-	ns
Data Hold Time (Note 1)	T_H	See the Figure 6, input Tr/Tf = 3.5 to 6.5ns	5	-	ns
Time for Data Output Valid from SCLK rising edge (Note 2)	T_D	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	0	22	ns
SDATA Output Transition (Rise/Fall) Time	$T_{SDATAOTR}$	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	2.1	10	ns
Data Drive Release Time	T_{SDATAZ}	Half Speed Read See the Figure 6 and 7, input Tr/Tf = 3.5 to 10ns	-	18	ns
Vio Supply Rise Time	T_{VIO-R}	See the Figure 8	-	400	µs
RFFE I/O Voltage Reset Timing	$T_{VIO-RST}$	See the Figure 8	10	-	µs
Signal Reset Delay Time	T_{SIGOL}	See the Figure 8	120	-	µs
RF Switching Time	T_{SW}	See the Figure 9	-	5	µs
Switching Interval (Note 3)	T_{int}	See the Figure 9	20	-	µs
Startup Time (Note 4)	T_{SU}	See the Figure 4	-	20	µs

Note 1 : Input SDATA is sampled at the falling edge of the SCLK.
Note 2 : Output SDATA changes at the rising edge of the SCLK.
Note 3 : The time between the consecutive Register Write Command Sequences for the Switch State register.
Note 4 : The time for the switch to reach Active State.

Note : The table of input SCLK signal conditions as below.

Parameter	Symbol	Ratings		Unit
SCLK Frequency	F_{SCLK}	Full Speed	0.032 to 26	MHz
		Half Speed	0.032 to 13	
SCLK Period	T_{SCLK}	Full Speed	0.038 to 32	µs
		Half Speed	0.077 to 32	
SCLK Rise/Fall Time	$T_{SCLKITR}$	Full/Half Speed	3.5 to 6.5	ns
SCLK Input Duty Cycle, High/Low Time	$T_{SCLKDCH}$ $T_{SCLKDCL}$	50		%

AC Waveforms

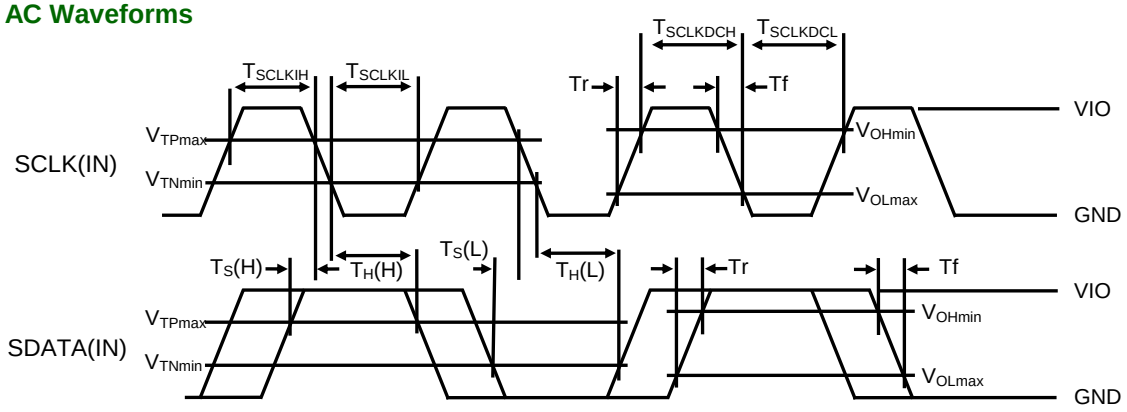


Figure 6. T_{SCLKDH}, $T_{SCLKDCL}$, T_{SCLKIH}, T_{SCLKIL}, T_S, T_H

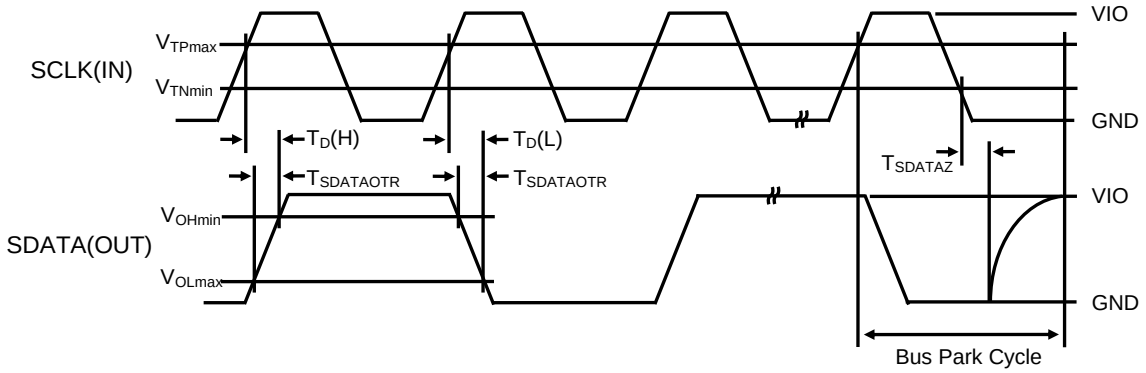


Figure 7. T_D, $T_{SDATAOTR}$, T_{SDATAZ}

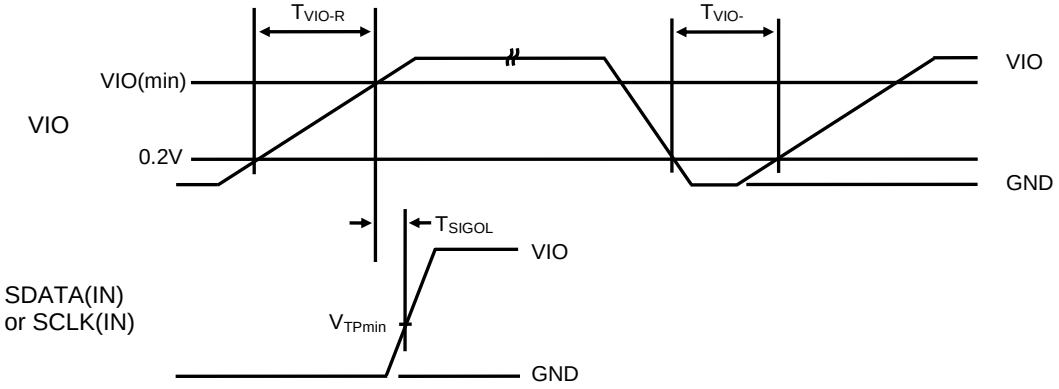


Figure 8. T_{VIO-R}, $T_{VIO-RST}$, T_{SIGOL}

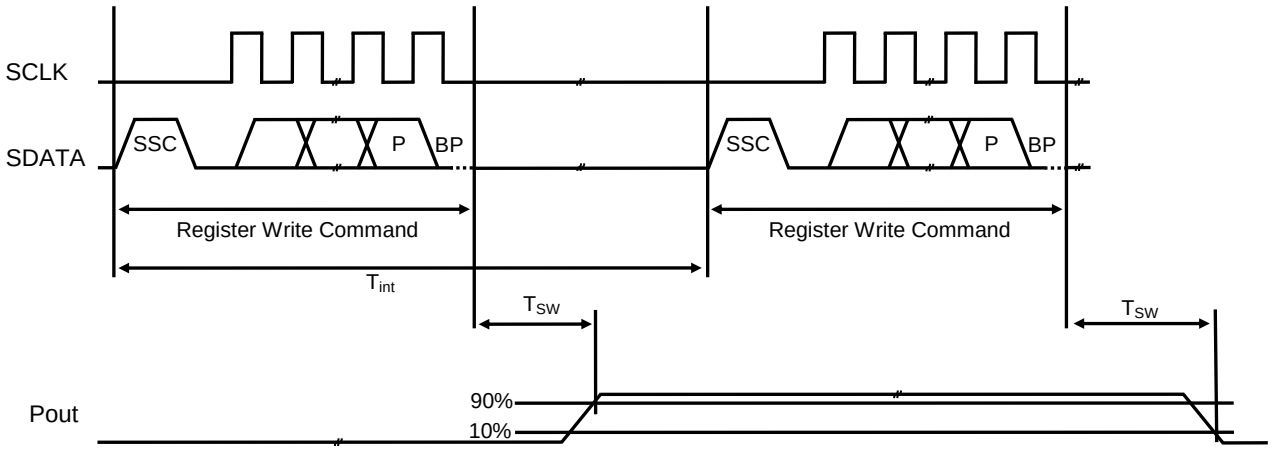


Figure 9. RF Switch Timing

Table 9. Register Mapping

Table 9. shows the list of the registers inside the RFASWY581CTF03.

Register Address		Bits	Read/Write	Description	Default Value (binary)
Hex	Binary				
0x01	00001	[7:0]	R/W	Bank A Switch Control Register	See Table 10
0x00	00000	[7:0]	R/W	Bank B Switch Control Register	See Table 11
0x1A	11010	[7:0]	R/W	RFFE Status (see Table 12)	0000 0000
0x1B	11011	[3:0]	R/W	GSID	0000 0000
0x1C	11100	[7:6] [5:0]	R/W	Power Mode (see Table 13) Triggers (see Table 14)	00 000000
0x1D	11101	[7:0]	R	Product ID	0100 0111
0x1E	11110	[7:0]	R	Manufacturer ID [7:0]	0010 0110
0x1F	11111	[7:6]	R	SPARE	00
		[5:4]	R	Manufacturer ID [9:8]	01
		[3:0]	R/W	USID	1010

Note : The RFASWY581CTF03 start-up procedure as below description.
The RFASWY581CTF03 requires to be disabled the triggers before programming the switch control registers when RFASWY581CTF03 operating in the active mode. The table of register address setup as below.

Register Address		Bits	Read/Write	Value (binary)
Hex	Binary			
0x1C	11100	[7:6] [5:0]	R/W	00 111000

Table 10. Switch Control Register

Bank A Antenna Path	Register_1 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
TRxA1	X	X	x	0	0	0	0	1
TRxA2	X	X	X	0	0	0	1	0
TRxA3	X	X	X	0	0	1	0	0
TRxA4	X	X	X	0	0	1	1	1
TRxA5	X	X	X	0	1	0	1	1
Isolation mode	X	X	X	0	0	0	0	0
	Define: X= not used							

Table 11. Switch Control Register

Bank B Antenna Path	Register_0 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
TRxB1	X	X	X	0	0	0	0	1
TRxB2	X	X	X	0	0	0	1	0
TRxB3	X	X	X	0	0	1	0	0
TRxB4	X	X	X	0	0	1	1	1
TRxB5	X	X	X	0	1	0	1	1
Isolation mode	X	X	X	0	0	0	0	0
	Define: X= not used							

Table 12. RFFE Status

D[7:0]	Read/Write	Description
D[7]	R/W	SOFTWARE RESET
D[6]	R	COMMAND_FRAME_ PARITY_ERR
D[5]		COMMAND_LENGTH_ERR
D[4]		ADDRESS_FRAME_PARITY_ERR
D[3]		DATA_FRAME_PARITY_ERR
D[2]		READ_UNUSED_REG
D[1]		WRITE_UNUSED_REG
D[0]		BID_GID_ERR

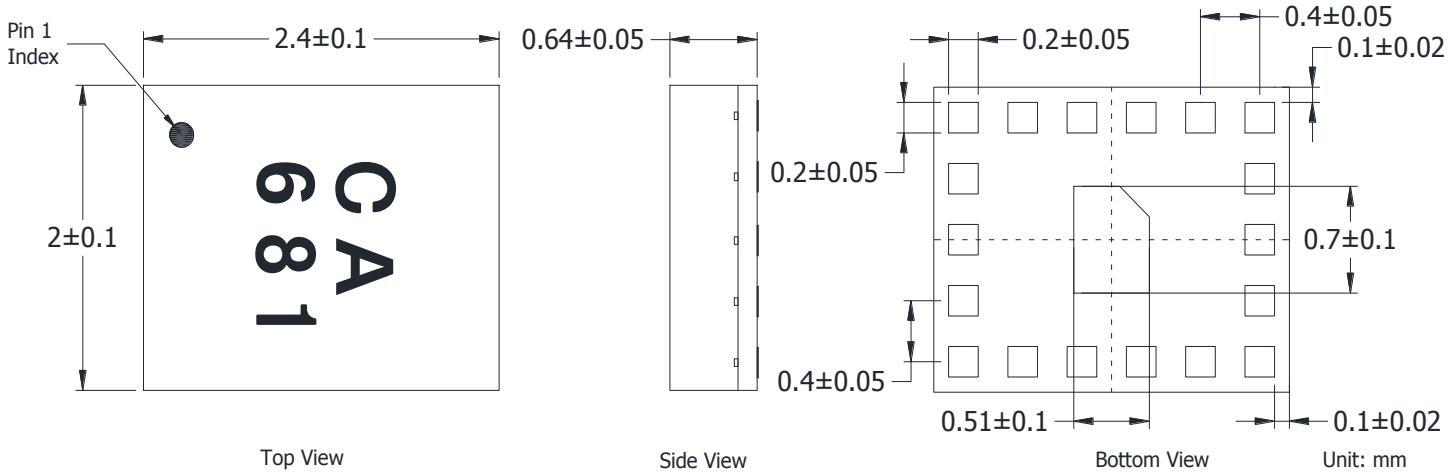
Table 13. Power Mode

D[7:6]	Read/Write	Status
00b	W	Part enters Active mode
	R	Part is in Active mode
01b	W	Part enters Start Up mode - part is reset
	R	Start Up mode will immediately transition to Low Power mode
10b	W	Part enters Low Power mode
	R	Part is in Low Power mode
11b	N/A	Will not occur - The state is discarded
		Will not occur - The state is discarded

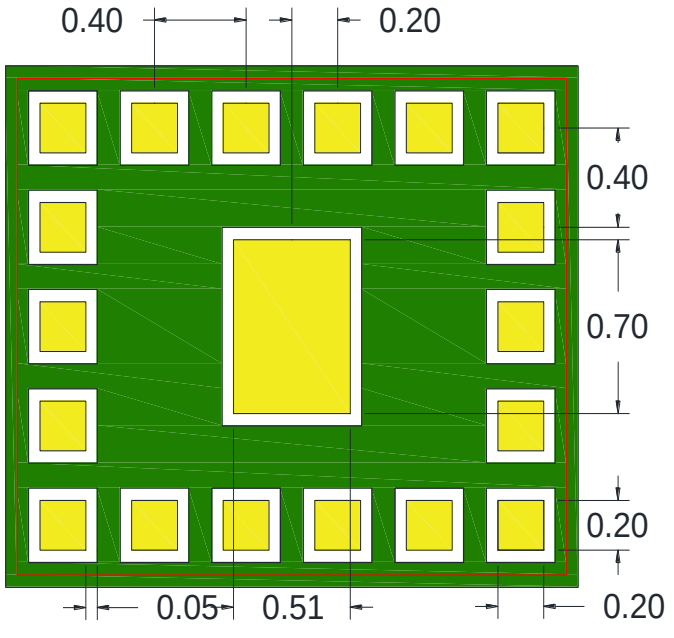
Table 14. Trigger States

D[5:0]	Read/Write	Status
D[5]	R/W	1 = Trigger 2 Disabled, 0 = Trigger 2 Enabled
D[4]		1 = Trigger 1 Disabled, 0 = Trigger 1 Enabled
D[3]		1 = Trigger 0 Disabled, 0 = Trigger 0 Enabled
D[2]	W	1 = Load Bits to Trigger 2, Trigger 2 states is Disabled
D[1]		1 = Load Bits to Trigger 1, Trigger 1 states is Disabled
D[0]		1 = Load Bits to Trigger 0, Trigger 0 states is Disabled

Table 15. Dimensions



Solder land pattern for reference only



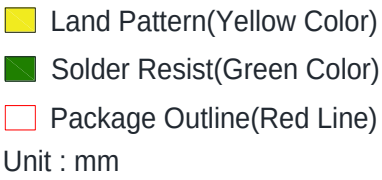


Figure 10. Solder Land Pattern Top View

Approval Sheet

Reliability test

TEST	PROCEDURE / TEST METHOD	REQUIREMENT
Solderability JIS C 0050-4.6 JESD22-B102D	*Solder bath temperature：255 ± 5°C *Immersion time：5 ± 0.5 sec Solder：Sn3Ag0.5Cu for lead-free	At least 95% of a surface of each terminal electrode must be covered by fresh solder.
High temperature JIS C 0021	*Temperature：90°C±2°C *Test duration：1000+24/-0 hours Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
Low temperature JIS C 0020	*Temperature：-30°C±2°C *Test duration：1000+24/-0 hours Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
Temperature cycle JIS C 0025	1. 30±3 minutes at -30±3°C, 2. 10~15 minutes at room temperature, 3. 30±3 minutes at +90±3°C, 4. 10~15 minutes at room temperature, Total 100 continuous cycles Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.
High temperature operation life (HTOL)	*Temperature：90°C *VDD = 4.8V *Time：1000+24/-0 hrs. Measurement to be made after keeping at room temperature for 24±2 hrs	No mechanical damage. Electrical specification shall satisfy the descriptions in electrical characteristics under the operational temperature range within -30 ~ 90°C.

Soldering condition

Typical examples of soldering processes that provide reliable joints without any damage are given in Figure 11.

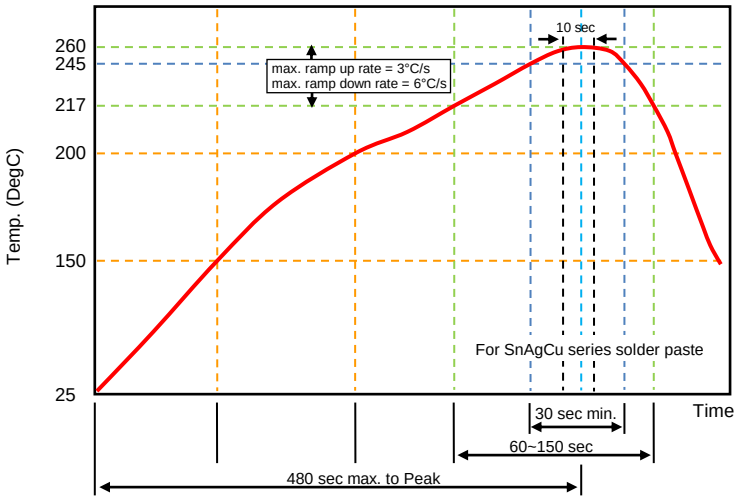


Figure 11. Infrared soldering profile

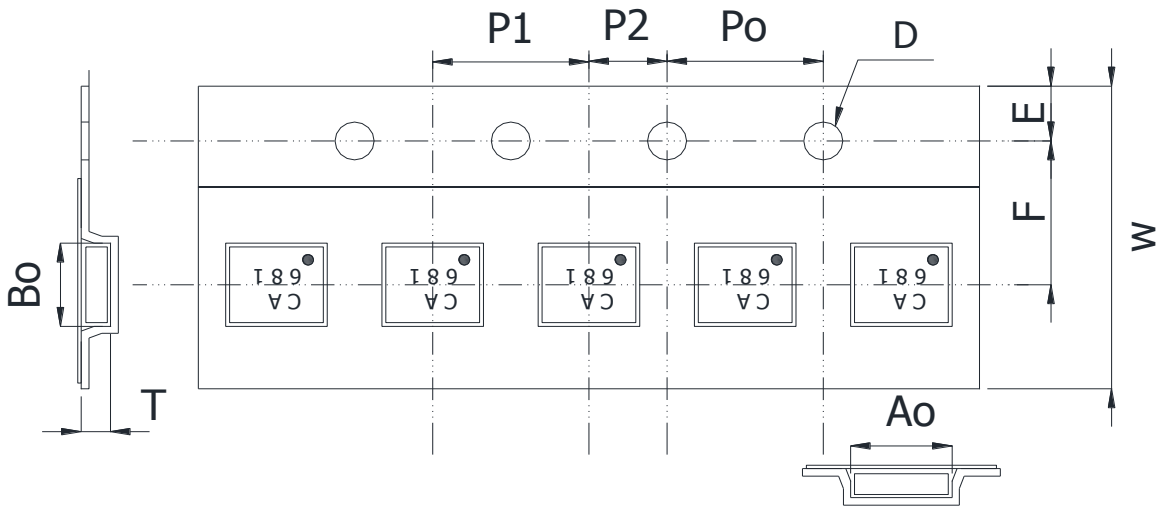
Approval Sheet

Ordering code

RF	ASW	Y	581C	T
RF module RF: Walsin RF Switch Device	**Module type** ASW: Antenna Switch	**Application** Y : DP10T	**Design Code**	**Packing** T: Taping

Minimum Ordering Quantity: 3000 pcs per reel.

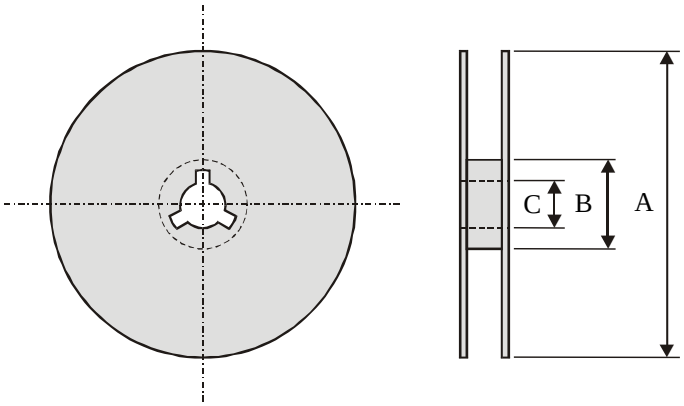
Packaging



Plastic Tape specifications (unit :mm)

Index	Ao	Bo	ΦD	T	W
Dimension (mm)	2.20 ± 0.05	2.60 ± 0.05	1.50 ± 0.10	1.2 ± 0.05	8.0 ± 0.20
Index	E	F	Po	P1	P2
Dimension (mm)	1.75 ± 0.10	3.50 ± 0.05	4.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.10

Reel dimensions



Index	A	B	C
Dimension (mm)	Φ178.0	Φ60.0	Φ13.0

Taping Quantity : 3000 pieces per 7” reel

Approval Sheet

Caution of handling

Limitation of Applications

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects, which might directly cause damage to the third party's life, body or property.

(1) Aircraft equipment
(2) Aerospace equipment
(3) Undersea equipment
(4) Medical equipment
(5) Disaster prevention / crime prevention equipment
(6) Traffic signal equipment
(7) Transportation equipment (vehicles, trains, ships, etc.)
(8) Applications of similar complexity and /or reliability requirements to the applications listed in the above.

Storage condition

(1) Products should be used in 6 months from the day of WALSIN outgoing inspection, which can be confirmed.

(2) Storage environment condition.

- Products should be storage in the warehouse on the following conditions.
- Temperature : -10 to +40°C
- Humidity : 30 to 70% relative humidity
- Don't keep products in corrosive gases such as sulfur. Chlorine gas or acid or it may cause oxidization of electrode, resulting in poor solderability.
- Products should be storage on the palette for the prevention of the influence from humidity, dust and son on.
- Products should be storage in the warehouse without heat shock, vibration, direct sunlight and so on.
- Products should be storage under the airtight packaged condition.