SLVSBB4 – AUGUST 2012

60 V Input, 3.5 A, Step Down Converter with Eco-mode™

Check for Samples: TPS54360

FEATURES

- **4.5 V to 60 V (65 V Abs Max) Input Range**
- **Current Mode Control Converter**
- **92-mΩ High-Side MOSFET**
- **High Efficiency at Light Loads with a Pulse Skipping Eco-mode™**
- **146 µA Operating Quiescent Current**
- **1 µA Shutdown Current**
- **100 kHz to 2.5 MHz Fixed Switching Frequency**
- **Synchronizes to External Clock**
- **Adjustable UVLO Voltage and Hysteresis**
- **Internal Soft-Start**
- **Accurate Cycle-by-Cycle Current Limit, Thermal, OVP, and Frequency Foldback Protection**
- **0.8-V 1% Internal Voltage Reference**
- **8-Pin HSOIC with PowerPAD™ Package**
- **–40°C to 150°C T_J Operating Range**
- **Supported by WEBENCH™ Software Tool**

APPLICATIONS

- **12-V, 24-V and 48-V Industrial, Automotive and Communications Power Systems**

DESCRIPTION

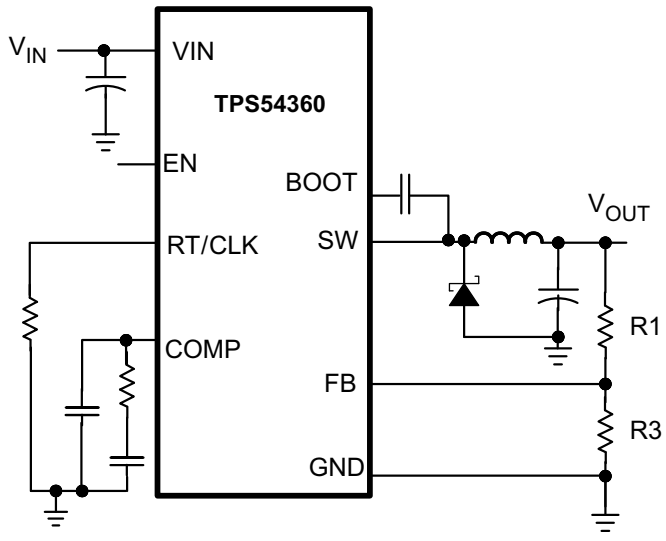
The TPS54360 is a 60 V, 3.5 A, step down regulator with an integrated high side MOSFET. Current mode control provides simple external compensation and flexible component selection. A low ripple pulse skip mode reduces the no load supply current to 146 µA. Shutdown supply current is reduced to 1 µA when the enable pin is pulled low.

Under voltage lockout is internally set at 4.3 V, but can be increased using the enable pin. The output voltage startup ramp is internally controlled to allow a controlled start-up and eliminate overshoot.

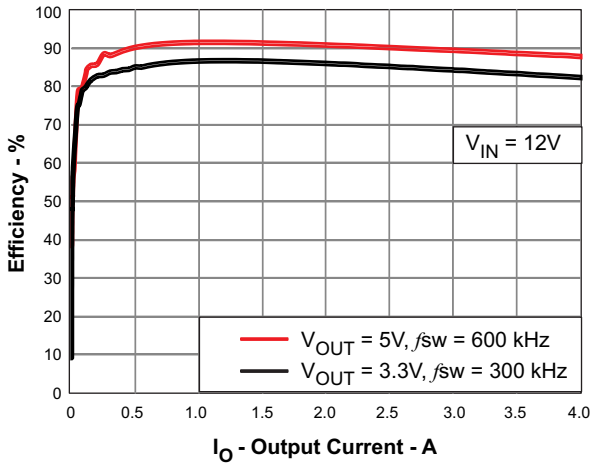
A wide switching frequency range allows either efficiency or external component size to be optimized. Frequency foldback and thermal shutdown protects internal and external components during an overload condition.

The TPS54360 is available in an 8-pin thermally enhanced HSOIC PowerPAD™ package.

SIMPLIFIED SCHEMATIC



EFFICIENCY vs LOAD CURRENT



PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

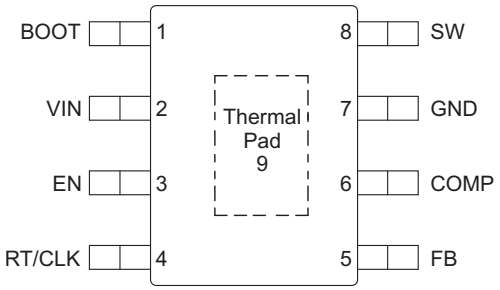
T_J	PACKAGE	PART NUMBER(2)
–40°C to 150°C	8 Pin HSOIC	TPS54360DDA

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The DDA package is also available in tape and reel packaging. Add an R suffix to the device type (that is TPS54360DDAR).

DEVICE INFORMATION

PIN CONFIGURATION

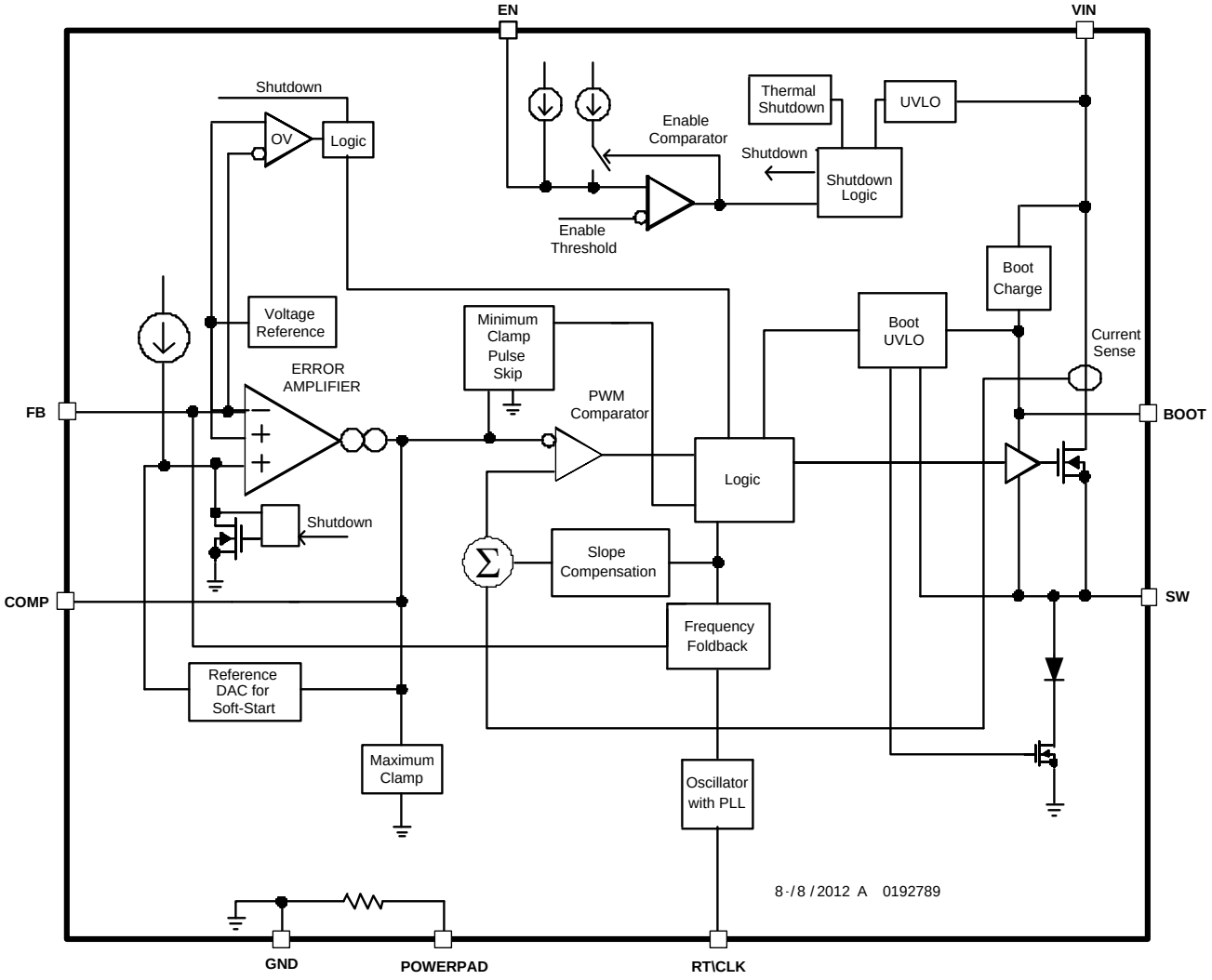
HSOIC PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high side MOSFET, the output is switched off until the capacitor is refreshed.
VIN	2	I	Input supply voltage with 4.5 V to 60 V operating range.
EN	3	I	Enable pin, with internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the Enable and Adjusting Undervoltage Lockout section.
RT/CLK	4	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
FB	5	I	Inverting node of the transconductance (gm) error amplifier.
COMP	6	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
GND	7	–	Ground
SW	8	I	The source of the internal high-side power MOSFET and switching node of the converter.
Thermal Pad	9	–	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage	VIN	–0.3	65	V
	EN	–0.3	8.4	
	BOOT		73	
	FB	–0.3	3	
	COMP	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT-SW		8	V
	SW	–0.6	65	
	SW, 10-ns Transient	–2	65	
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating junction temperature			–40 to 150	°C
Storage temperature			–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS54360	UNITS
		DDA (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance (standard board)	42.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	
ψ_{JB}	Junction-to-board characterization parameter	23.4	
θ_{JCtop}	Junction-to-case(top) thermal resistance	45.8	
θ_{JCbot}	Junction-to-case(bottom) thermal resistance	3.6	
θ_{JB}	Junction-to-board thermal resistance	23.4	

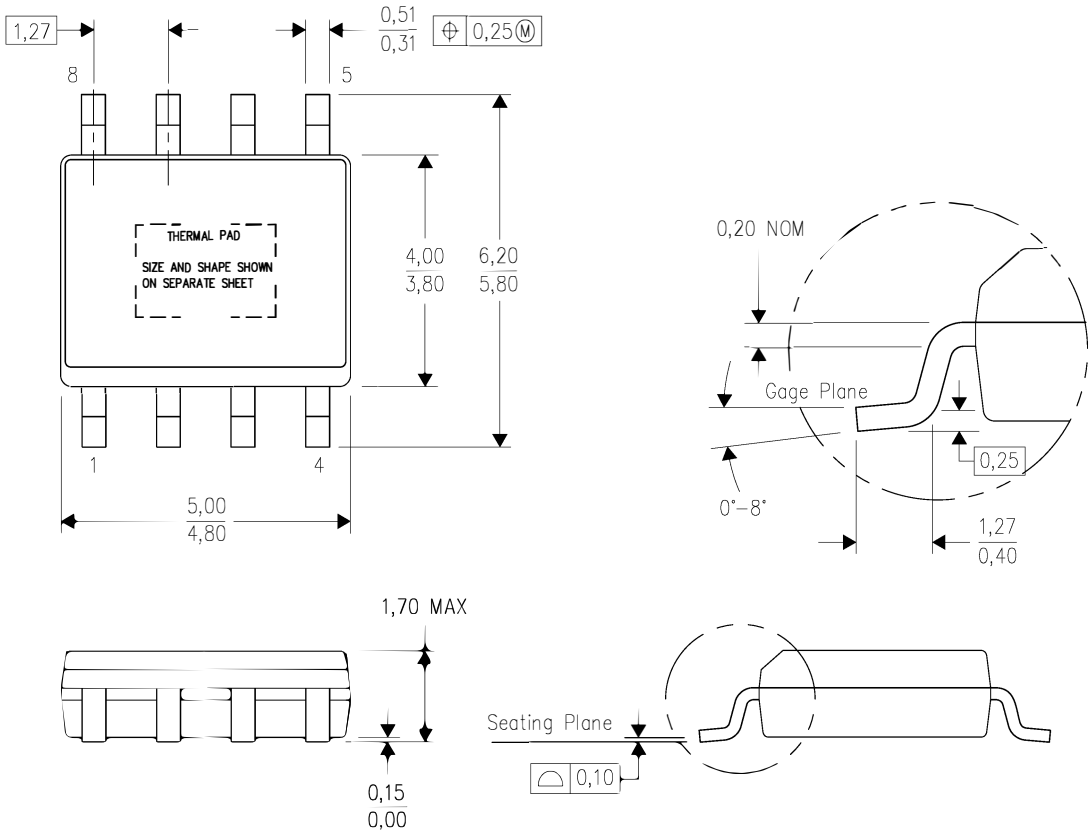
(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Power rating at a specific ambient temperature TA should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 150°C, VIN = 4.5 to 60V (unless otherwise noted)

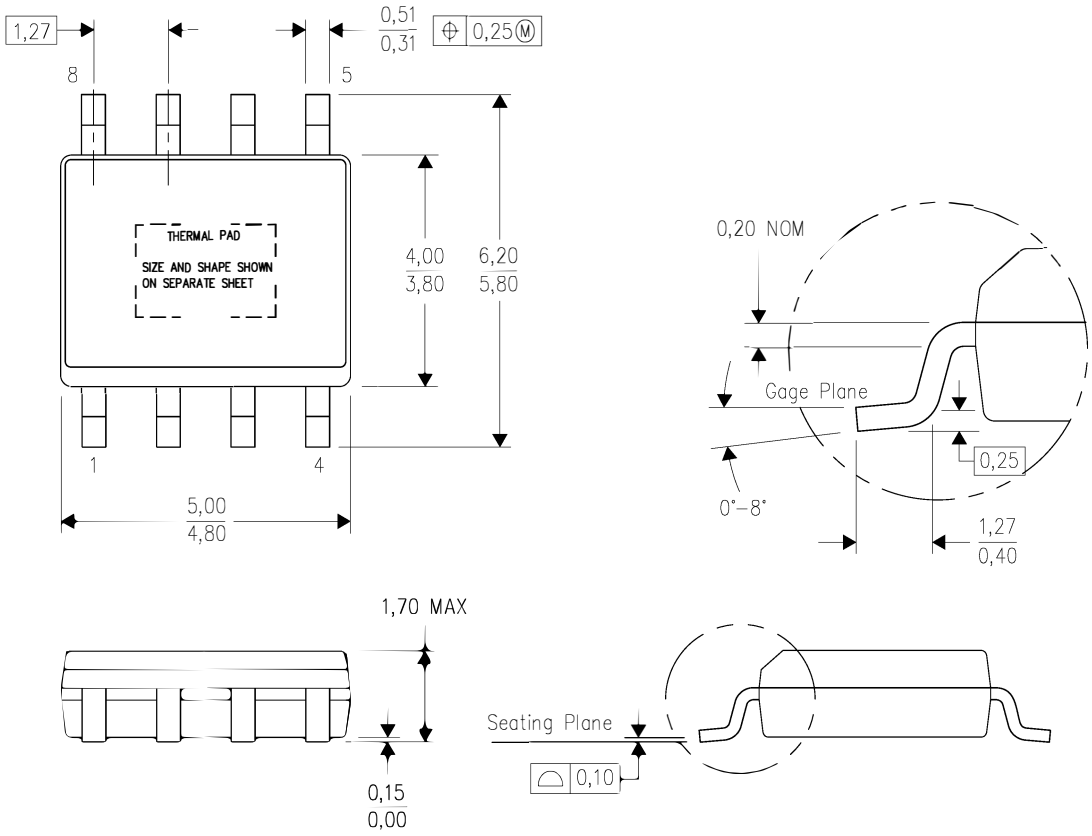
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
	Operating input voltage		4.5		60	V
	Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
	Internal undervoltage lockout threshold hysteresis			325		mV
	Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 60 V		1.3	3.5	µA
	Operating: nonswitching supply current	FB = 0.83 V, T_A = 25°C		146	175	
ENABLE AND UVLO (EN PIN)						
	Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
	Input current	Enable threshold +50 mV		–4.6		µA
		Enable threshold –50 mV	–0.58	–1.2	-1.8	
	Hysteresis current		–2.2	–3.4	-4.5	µA
INTERNAL SOFT-START TIME						
	Soft-Start Time	f_{SW} = 500 kHz, 10% to 90%		1.5		ms
	Soft-Start Time	f_{SW} = 2.5 MHz, 10% to 90%		0.42		ms
VOLTAGE REFERENCE						
	Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET						
	On-resistance	VIN = 12 V, BOOT-SW = 6 V		92	190	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
	Error amplifier transconductance (g_M)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		350		µMhos
	Error amplifier transconductance (g_M) during soft-start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		µMhos
	Error amplifier dc gain	V_{FB} = 0.8 V		10,000		V/V
	Min unity gain bandwidth			2500		kHz
	Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±30		µA
	COMP to SW current transconductance			12		A/V
CURRENT LIMIT						
	Current limit threshold	All VIN and temperatures, Open Loop	4.5	5.5	6.8	A
		All temperatures, VIN = 12 V, Open Loop	4.5	5.5	6.25	
		VIN = 12 V, T_A = 25°C, Open Loop	5.2	5.5	5.85	
	Current limit threshold delay			60		ns
THERMAL SHUTDOWN						
	Thermal shutdown			176		°C
	Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	Minimum CLK input pulse width			15		ns
	RT/CLK high threshold			1.55	1.7	V
	RT/CLK low threshold		0.5	1.2		V
	RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with RT resistor in series		55		ns
	PLL lock in time	Measured at 500 kHz		78		µs

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



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