SGM2048
1A, Low Noise, Wide Bandwidth, High PSRR, Low Dropout Linear Regulator

GENERAL DESCRIPTION

The SGM2048 is a low noise, high PSRR, low dropout voltage linear regulator. It is capable of supplying 1A output current with typical dropout voltage of only 150mV. The operating input voltage range is from 2.2V to 7V. The SGM2048 is available in fixed output voltage versions and an adjustable version that allows the output voltage range from 0.8V to 6V.

Other features include logic-controlled shutdown mode, short-circuit current limit and thermal shutdown protection. The SGM2048 has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2048 is available in a Green TDFN-3×3-8CL package. It operates over an operating temperature range of -40℃ to +125℃.

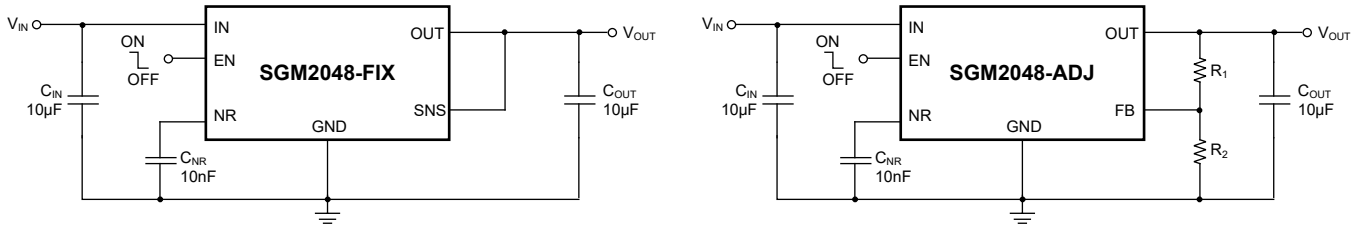
FEATURES

- **Operating Input Voltage Range: 2.2V to 7V**
- **Fixed Outputs of 1.2V, 1.8V, 2.8V, 3.0V, 3.3V, 5.0V**
- **Adjustable Output from 0.8V to 6V**
- **Output Voltage Accuracy: ±1% at +25℃**
- **Low Dropout Voltage: 150mV (TYP) at 1A**
- **Low Noise: 30μV_{RMS} (TYP)**
- **Power Supply Rejection Ratio at V_{OUT} = 3.3V:**
  - **75dB at 1kHz**
  - **65dB at 100kHz**
  - **55dB at 1MHz**
- **Current Limiting and Thermal Protection**
- **Excellent Load and Line Transient Responses**
- **With Output Automatic Discharge**
- **Stable with Small Case Size Ceramic Capacitors**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TDFN-3×3-8CL Package**

APPLICATIONS

Wireless Basestation
PLL/VCO/RF Circuit
Audio Equipment

TYPICAL APPLICATION



Fixed Voltage Typical Application Circuit

Adjustable Voltage Typical Application Circuit

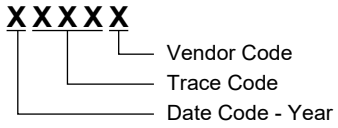
Figure 1. Typical Application Circuits

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2048-1.2	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-1.2XTEK8G/TR	SGMSXU XTEK8 XXXXX	Tape and Reel, 4000
SGM2048-1.8	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-1.8XTEK8G/TR	SGMSXV XTEK8 XXXXX	Tape and Reel, 4000
SGM2048-2.8	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-2.8XTEK8G/TR	SGMSXW XTEK8 XXXXX	Tape and Reel, 4000
SGM2048-3.0	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-3.0XTEK8G/TR	SGMSXX XTEK8 XXXXX	Tape and Reel, 4000
SGM2048-3.3	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-3.3XTEK8G/TR	SGMSXY XTEK8 XXXXX	Tape and Reel, 4000
SGM2048-5.0	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-5.0XTEK8G/TR	SGMRB0 XTEK8 XXXXX	Tape and Reel, 4000
SGM2048-ADJ	TDFN-3×3-8CL	-40℃ to +125℃	SGM2048-ADJXTEK8G/TR	SGMRAF XTEK8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, OUT to GND ..... -0.3V to 8V
FB, NR to GND ..... -0.3V to 3.6V
EN to GND ..... -0.3V to 7V
Package Thermal Resistance
TDFN-3×3-8CL, θ_{JA} ..... 53℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Input Voltage Range, V_{IN} ..... 2.2V to 7V
Adjustable Output Voltage Range ..... 0.8V to 6V
Fixed Output Voltage Range ..... 1.2V to 5V
Enable Voltage Range ..... 0V to 7V
Input Effective Capacitance, C_{IN} ..... 4μF (MIN)
Output Effective Capacitance, C_{OUT} ..... 4μF to 100μF
Noise Reduction Capacitance, C_{NR} ..... 1nF (MIN)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

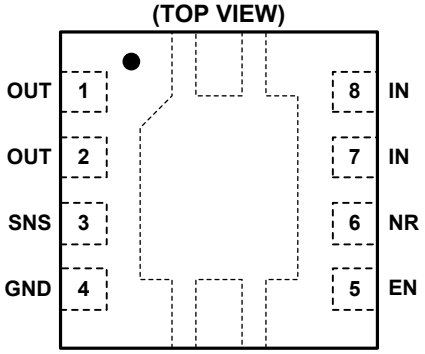
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

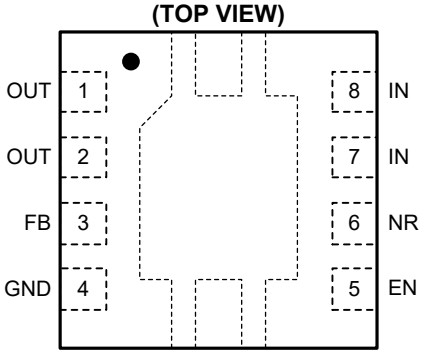
PIN CONFIGURATIONS

SGM2048-Fixed Output
(TOP VIEW)



TDFN-3×3-8CL

SGM2048-ADJ
(TOP VIEW)



TDFN-3×3-8CL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 4μF to 100μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
3	FB	Feedback Voltage Input Pin (adjustable voltage version only). Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
	SNS	Output Voltage Sense Input Pin (fixed voltage version only). Connect this pin to the load side of the output trace only in the fixed voltage version.
4	GND	Ground.
5	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. The EN pin has an internal pull-down current source which ensures that the device is turned off when the EN pin is floated. This pin must be pulled high by an external resistor connected to IN pin if EN pin is not used.
6	NR	Noise-Reduction Pin. Using an external capacitor C_{NR} to decouple this pin to GND can not only reduce output noise to very low level but also slow down the V_{OUT} rise like a soft-start behavior.
7, 8	IN	Input Supply Voltage Pin. It is recommended to use a 4.7μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
Exposed Pad	_	Exposed Pad. Connect it to a large ground plane to maximize thermal performance; this pad is not an electrical connection point.

ELECTRICAL CHARACTERISTICS

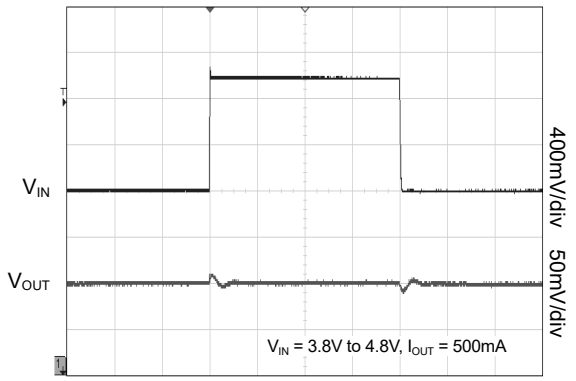
(V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2.2V (whichever is greater), V_{EN} = 2.2V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 4.7μF and C_{NR} = 10nF. For SGM2048-ADJ, tested at V_{OUT} = 0.8V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Range	V_{OUT}	Adjustable voltage version		0.8		6	V
		Fixed voltage version		1.2		5	
Internal Reference Voltage	V_{NR}	Adjustable and Fixed voltage versions, V_{OUT} < 1.8V		0.789	0.8	0.824	V
		Fixed voltage version, V_{OUT} ≥ 1.8V		1.183	1.2	1.236	
Under-Voltage Lockout Thresholds	V_{UVLO}	V_{IN} rising, R_L = 1kΩ		1.9	2	2.1	V
		Hysteresis			150		mV
Output Voltage Accuracy	V_{OUT}	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 7V, V_{IN} ≥ 2.2V, I_{OUT} = 1mA to 1A	T_J = +25℃	-1		1	%
			T_J = -40℃ to +125℃	-2		2	
Shutdown Current	I_{SHDN}	V_{EN} ≤ 0.4V, V_{IN} ≥ 2.2V, R_L = 1kΩ	T_J = -40℃ to +85℃		1	2.5	μA
			T_J = -40℃ to +125℃			6	
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) to 7V, V_{IN} ≥ 2.2V, I_{OUT} = 100mA			0.004	0.029	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1mA to 1A			1	15	μV/mA
Dropout Voltage	V_{DROP}	V_{FB} = GND or V_{SNS} = GND	V_{IN} ≥ 2.2V, I_{OUT} = 500mA		80	130	mV
			V_{IN} ≥ 2.5V, I_{OUT} = 750mA		115	200	
			V_{IN} ≥ 2.5V, I_{OUT} = 1A		150	260	
Output Current Limit	I_{LIMIT}	V_{OUT} = 90% × $V_{OUT(NOM)}$, V_{IN} = ($V_{OUT(NOM)}$ + 1V)		1.05	1.6	2.15	A
Short Current Limit	I_{SHORT}	V_{OUT} = 0V			1.6		A
Ground Pin Current	I_{GND}	I_{OUT} = 1mA, adjustable voltage version			80	115	μA
		I_{OUT} = 1mA, fixed voltage version			100	150	
		I_{OUT} = 1A			1100	1450	
Feedback Pin Current	I_{FB}	V_{IN} = 6.5V, V_{FB} = 0.85V			0.001	0.1	μA
EN Pin High-Level Input Voltage	$V_{EN(H)}$	2.2V < V_{IN} ≤ 7V, R_L = 1kΩ		1.2			V
EN Pin Low-Level Input Voltage	$V_{EN(L)}$					0.4	V
EN Pin Current	I_{EN}	V_{IN} = 7V, V_{EN} = 0V			0.001	1	μA
		V_{IN} = V_{EN} = 7V			0.13	1	
Start-Up Time	t_{STR}	$V_{OUT(NOM)}$ = 3.3V, from assertion of V_{EN} to 90% × $V_{OUT(NOM)}$, R_L = 3.3kΩ	C_{NR} = 1nF		0.2		ms
			C_{NR} = 10nF		1.8		
Power Supply Rejection Ratio	PSRR	V_{IN} = 4.3V, $V_{OUT(NOM)}$ = 3.3V, I_{OUT} = 750mA, C_{NR} = 10nF	f = 100Hz		78		dB
			f = 1kHz		75		
			f = 10kHz		75		
			f = 100kHz		65		
			f = 1MHz		55		
Output Voltage Noise	e_n	V_{IN} = 4.3V, $V_{OUT(NOM)}$ = 3.3V, I_{OUT} = 100mA, f = 10Hz to 100kHz	C_{NR} = 1nF		60		μV_{RMS}
			C_{NR} = 10nF		36		
			C_{NR} = 100nF		30		
Output Discharge Resistance	R_{DIS}				105		Ω
Thermal Shutdown Temperature	T_{SHDN}				170		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		℃

TYPICAL PERFORMANCE CHARACTERISTICS

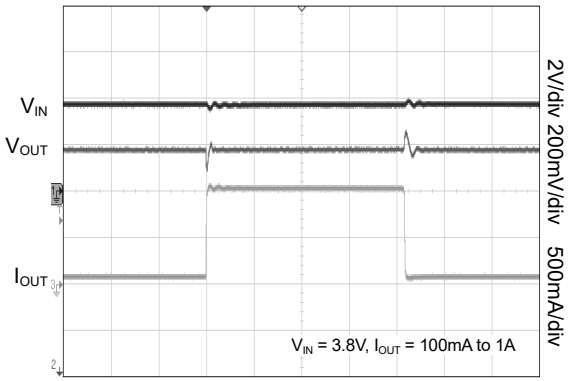
T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2.2V (whichever is greater), $V_{OUT(NOM)}$ = 3.3V, V_{EN} = V_{IN}, I_{OUT} = 100mA, C_{IN} = C_{OUT} = 4.7μF, C_{NR} = 10nF, unless otherwise noted.

Line Transient Response



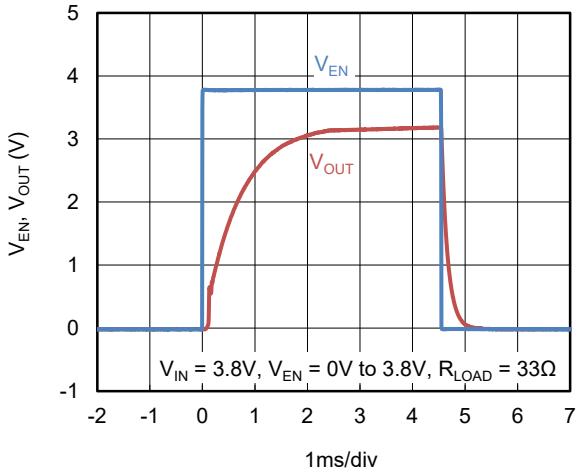
Time (50μs/div)

Load Transient Response

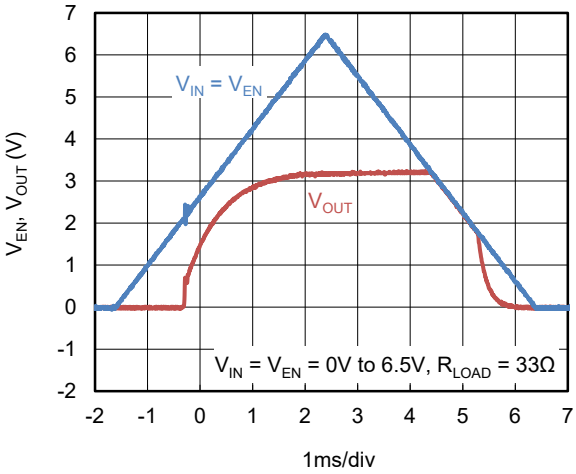


Time (50μs/div)

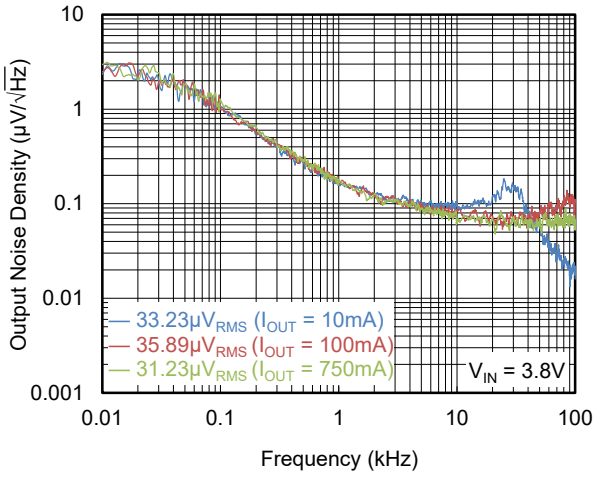
Enable Pulse Response



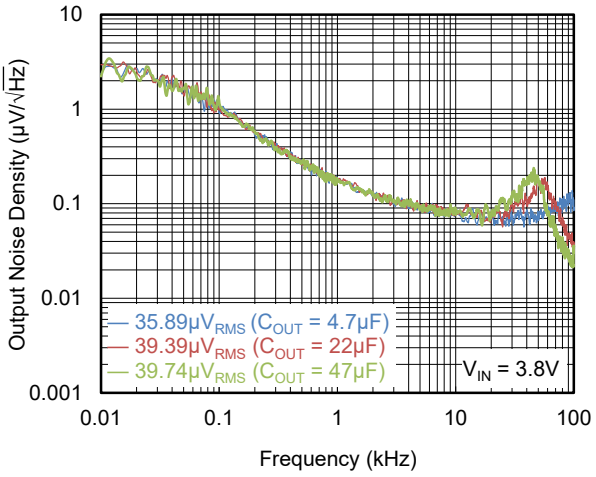
Power-Up and Power-Down Response



Output Noise Density vs. Frequency



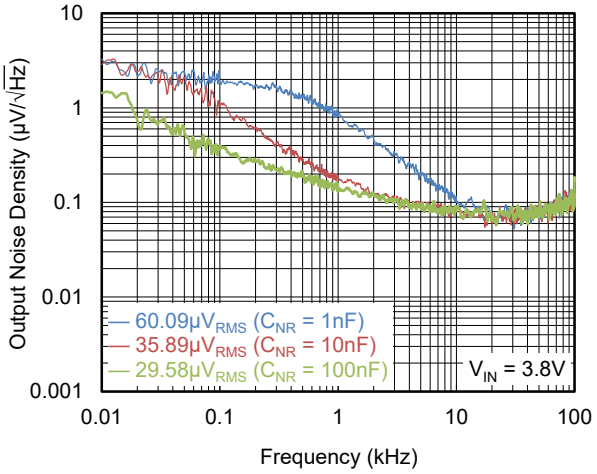
Output Noise Density vs. Frequency



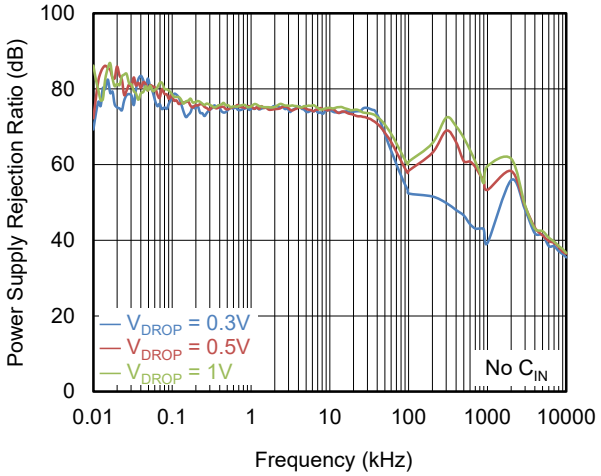
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2.2V (whichever is greater), $V_{OUT(NOM)}$ = 3.3V, V_{EN} = V_{IN}, I_{OUT} = 100mA, C_{IN} = C_{OUT} = 4.7μF, C_{NR} = 10nF, unless otherwise noted.

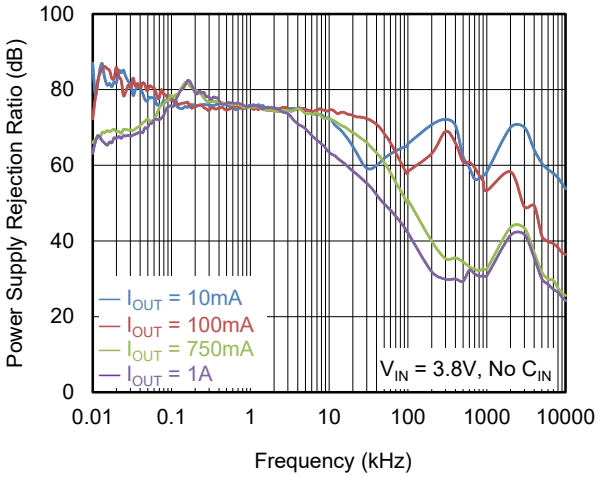
Output Noise Density vs. Frequency



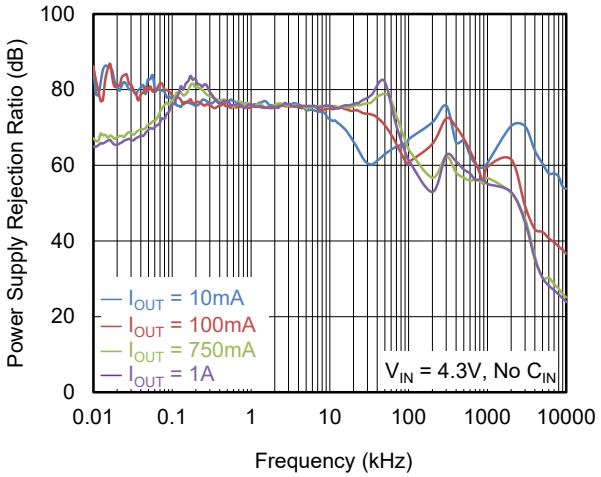
Power Supply Rejection Ratio vs. Frequency



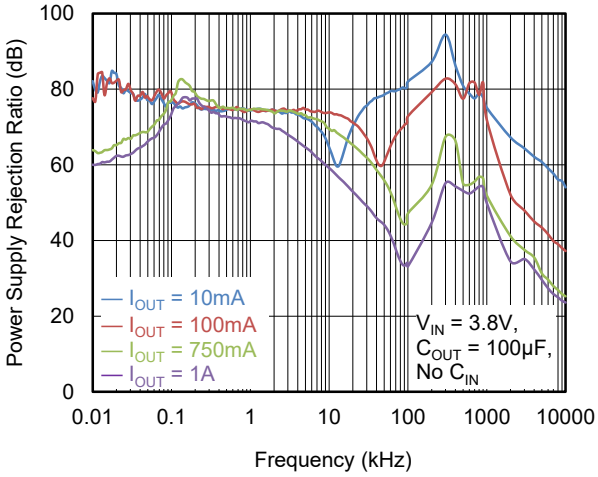
Power Supply Rejection Ratio vs. Frequency



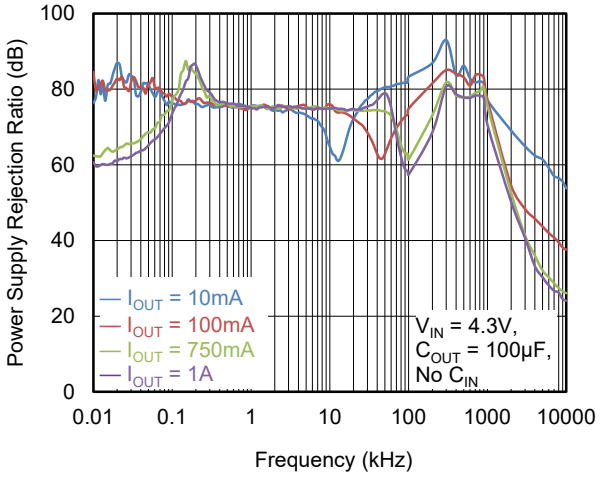
Power Supply Rejection Ratio vs. Frequency



Power Supply Rejection Ratio vs. Frequency



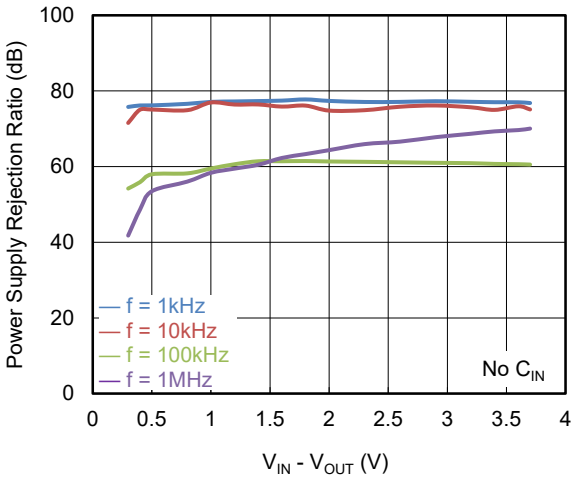
Power Supply Rejection Ratio vs. Frequency



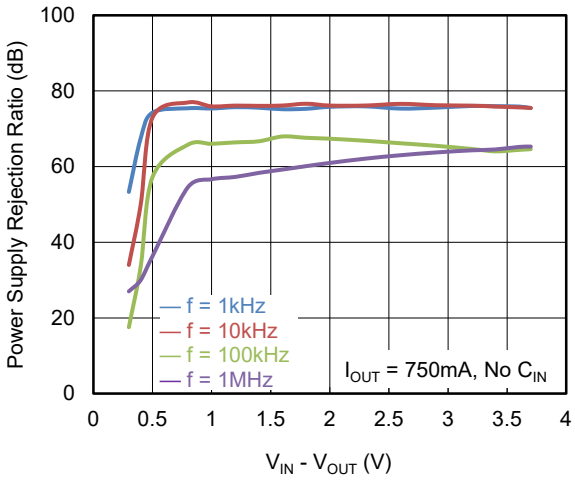
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2.2V (whichever is greater), $V_{OUT(NOM)}$ = 3.3V, V_{EN} = V_{IN}, I_{OUT} = 100mA, C_{IN} = C_{OUT} = 4.7μF, C_{NR} = 10nF, unless otherwise noted.

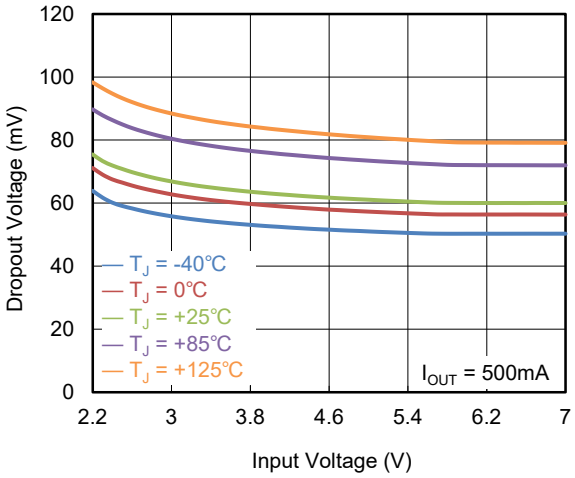
Power Supply Rejection Ratio vs. (V_{IN} - V_{OUT})



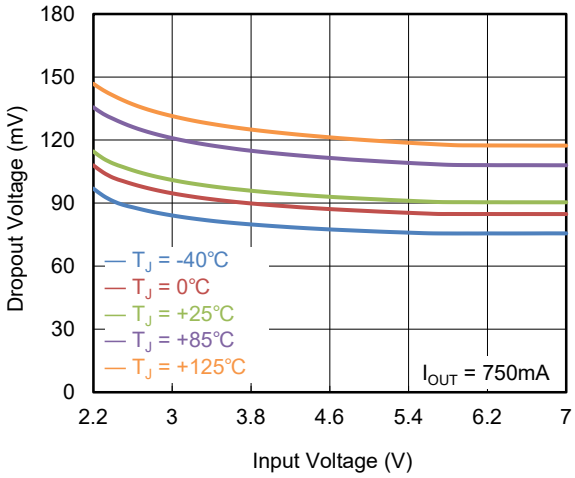
Power Supply Rejection Ratio vs. (V_{IN} - V_{OUT})



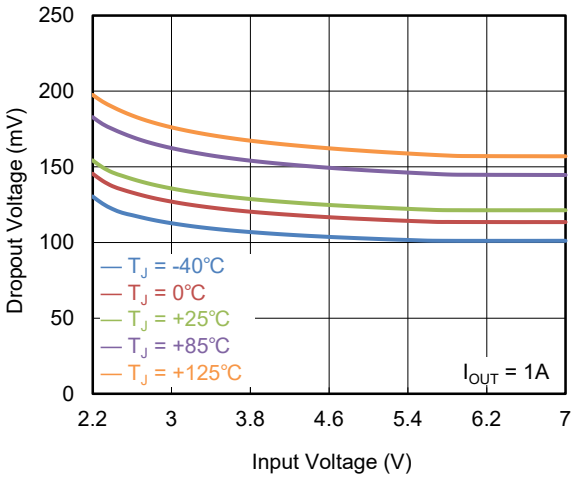
Dropout Voltage vs. Input Voltage



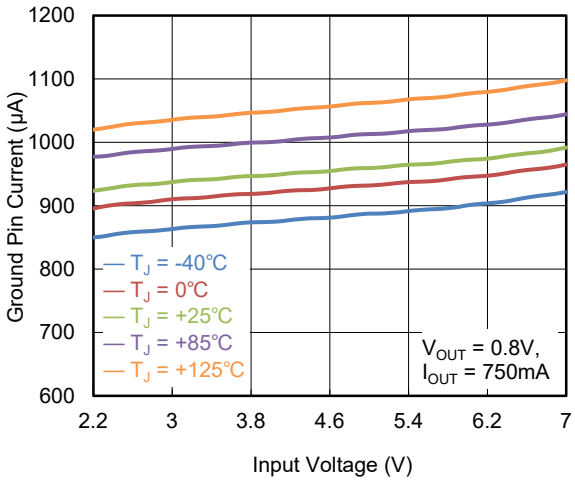
Dropout Voltage vs. Input Voltage



Dropout Voltage vs. Input Voltage



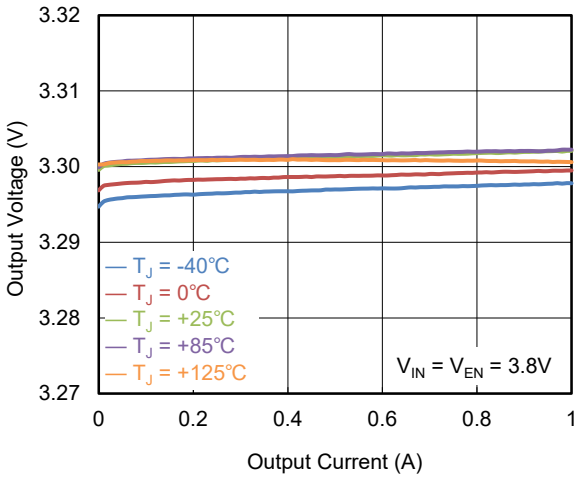
Ground Pin Current vs. Input Voltage



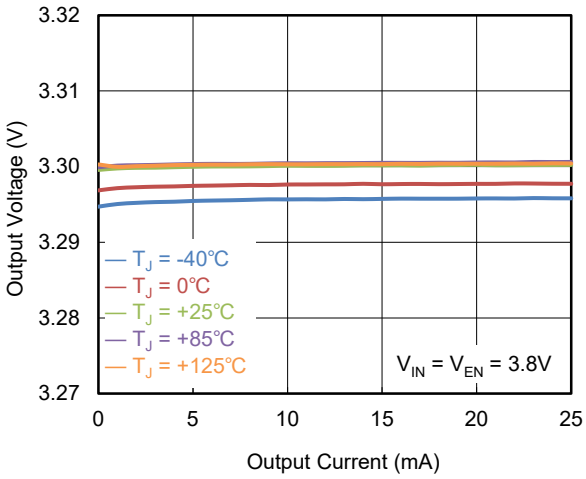
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2.2V (whichever is greater), $V_{OUT(NOM)}$ = 3.3V, V_{EN} = V_{IN}, I_{OUT} = 100mA, C_{IN} = C_{OUT} = 4.7μF, C_{NR} = 10nF, unless otherwise noted.

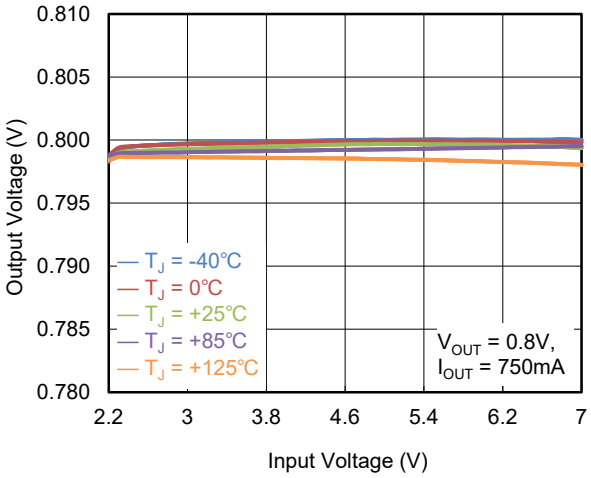
Load Regulation



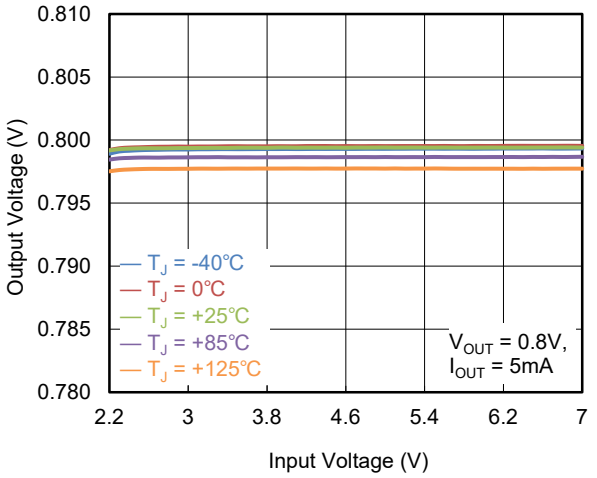
Load Regulation Under Light Loads



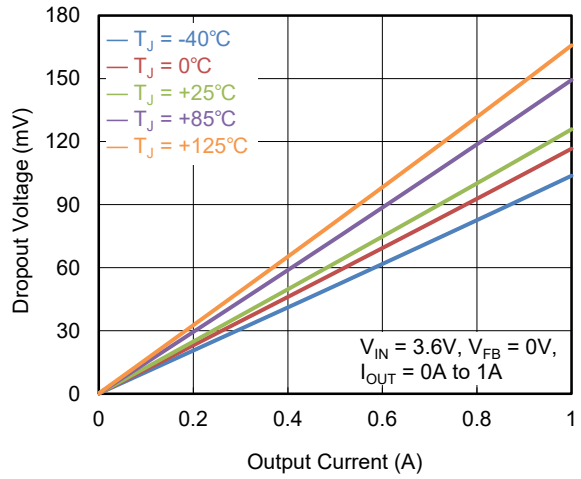
Line Regulation



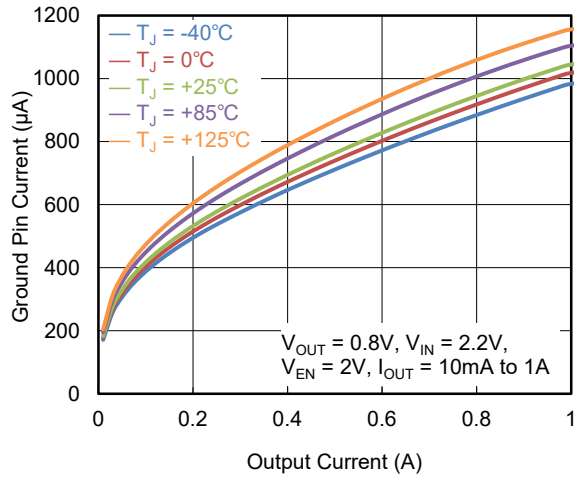
Line Regulation Under Light Loads



Dropout Voltage vs. Output Current



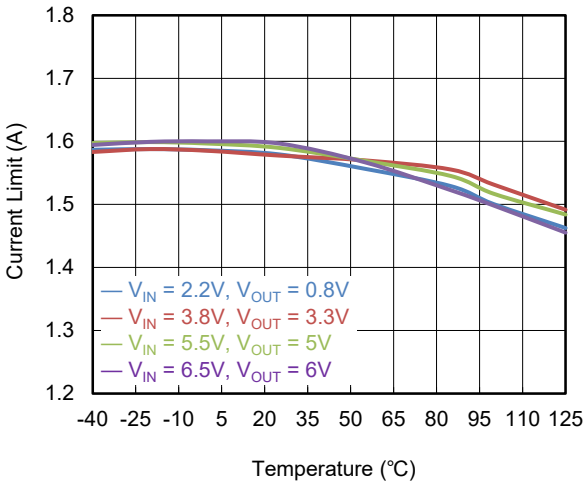
Ground Pin Current vs. Output Current



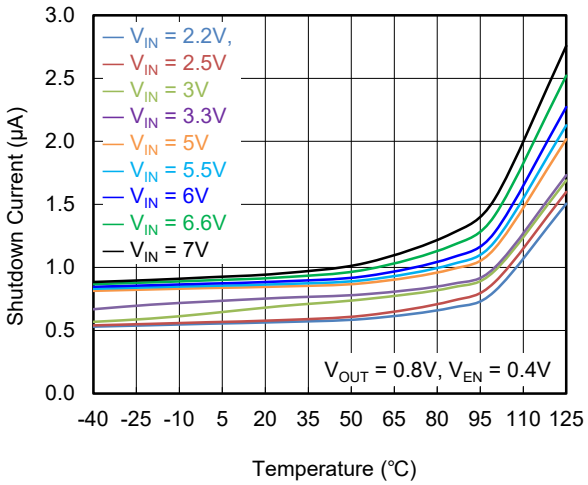
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 0.5V) or 2.2V (whichever is greater), $V_{OUT(NOM)}$ = 3.3V, V_{EN} = V_{IN}, I_{OUT} = 100mA, C_{IN} = C_{OUT} = 4.7μF, C_{NR} = 10nF, unless otherwise noted.

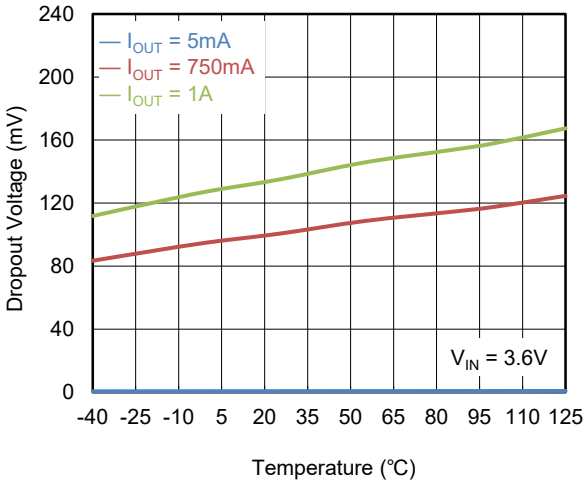
Current Limit vs. Temperature



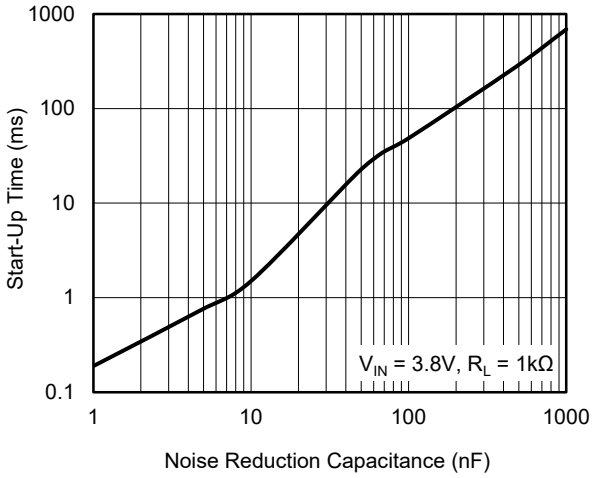
Shutdown Current vs. Temperature



Dropout Voltage vs. Temperature



Start-Up Time vs. Noise Reduction Capacitance



FUNCTIONAL BLOCK DIAGRAMS

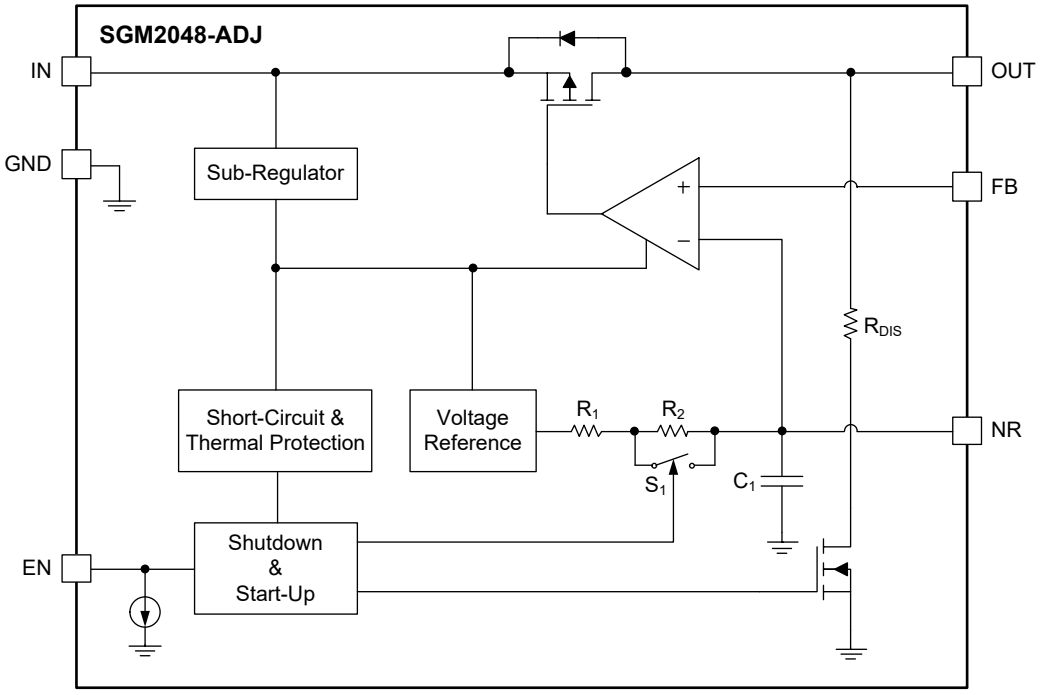


Figure 2. Adjustable Output Voltage Internal Block Diagram

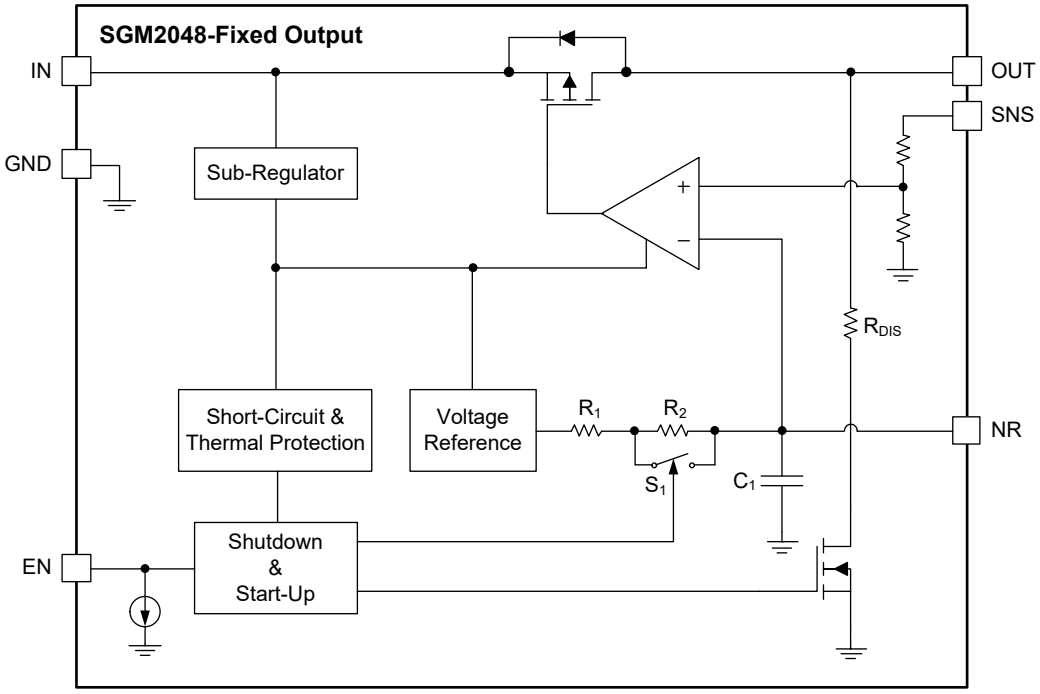


Figure 3. Fixed Output Voltage Internal Block Diagram

APPLICATION INFORMATION

The SGM2048 is a low noise, high PSRR and fast transient response LDO and provides 1A output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2048 useful in a variety of applications. The SGM2048 provides the protection function for output overload, output short-circuit condition and overheating.

The SGM2048 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 1μA (TYP).

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the IN pin for ensuring the device stability. 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and keep it below the device absolute maximum ratings.

Output Capacitor Selection (C_{OUT})

The output decoupling capacitor should be placed as close as possible to the OUT pin. 10μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of C_{OUT} that SGM2048 can remain stable is 4.7μF. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of C_{OUT} must be considered in design. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Noise-Reduction Capacitor (C_{NR})

A 10nF C_{NR} is used to minimize the noise of LDO in application. V_{REF}, output resistor divider and error amplifier are the dominant noise source of LDO in application, but for the SGM2048, the V_{REF} does not contribute significantly to noise due to noise-reduction capacitor C_{NR}. On the contrary, the dominant noise sources are the output resistor divider and the error amplifier.

Dropout Voltage and V_{IN}

The SGM2048 features low dropout voltage due to low $R_{DS(ON)}$ PMOSFET power transistor. For Linear regulator, when (V_{IN} - V_{OUT}) < dropout voltage (V_{DROP}), the PMOSFET power transistor will be turned on like a switch, the parameter of linear regulator, such as PSRR, load and input transient responses, will be degraded so much. To get good performance in application, the V_{IN} must be larger than (V_{OUT} + V_{DROP}).

Adjustable Regulator

The output voltage of the SGM2048-ADJ can be adjusted from 0.8V to 6V. The FB pin will be connected to two external resistors as shown in Figure 4. The output voltage is determined by the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

V_{OUT} is output voltage and V_{FB} is the internal voltage reference, V_{FB} = 0.8V.

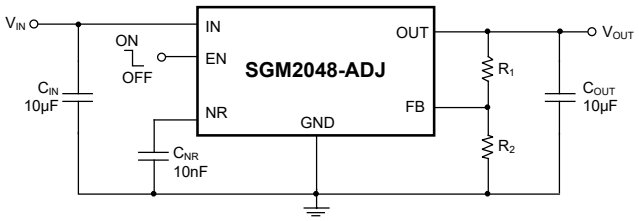


Figure 4. Adjustable Output Voltage Application

R_1 and R_2 can be calculated for any output voltage range using Equation 1. Choose R_2 = 10kΩ to maintain an 80μA minimum load.

Enable Control

The EN pin of the SGM2048 is used to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than $V_{EN(L)}$, the device is in shutdown state, there is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 105Ω (TYP) resistor.

When the EN pin voltage is higher than $V_{EN(H)}$, the device is in active state, the input voltage is regulated to the output voltage and the automatic discharge transistor is turned off.

APPLICATION INFORMATION (continued)

Start-Up

In Figure 2 and Figure 3, a low-pass (RC) filter is used to reduce the noise of bandgap voltage reference, the external C_{NR} and the resistance controlled by the quick-start circuit consists of this filter. The switch for quick-start is closed at start-up, C_{NR} will be charged by V_{REF} circuit and there is only 33kΩ resistance between bandgap circuit output and the NR pin. It's about 2ms after the device is enabled that the switch for quick-start will be turned off, the resistance between the NR pin and bandgap circuit output will be changed to about 265kΩ. This low-pass filter helps LDO achieve very good noise-reduction after start-up due to resistance is changed from 33kΩ to 265kΩ. Generally, low leakage ceramic capacitor is used and the value of C_{NR} is larger than 10nF. Larger C_{NR} is better to reduce the noise of LDO, but it prolongs the start-up time of LDO, the value of C_{NR} must be the trade-off between noise and start-up time.

Under-Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{IN} rises above the V_{UVLO} threshold. The UVLO circuit responds quickly to glitches on the IN pin and attempts to disable the output of the device if any of these rails collapses. The local input capacitance prevents severe brownouts in most applications.

Minimum Load

The SGM2048 fixed voltage versions can remain stable when there is no output load.

Input Power Supply

The input power supply range is from 2.2V to 7V. V_{IN} must be larger than (V_{OUT} + V_{DROP}) in application. The input ceramic capacitor must be placed as close as possible to the IN pin, this C_{IN} can help improve the output noise performance of LDO.

Reverse Current Protection

The pass transistor has an inherent body diode which will be forward biased in the case when V_{OUT} > (V_{IN} + 0.3V). If extended reverse voltage operation is anticipated, external limiting might be appropriate.

Negatively Biased Output

When the output voltage is negative, the chip may not start up due to parasitic effects. Ensure that the output is greater than -0.3V under all conditions. If negatively biased output is excessive and expected in the application, a Schottky diode can be added between the OUT pin and GND pin.

Output Current Limit and Short-Circuit Protection

When overload events happen, the output current is internally limited to 1.6A (TYP). When the OUT pin is shorted to ground, the short-circuit protection will limit the output current to 1.6A (TYP).

Thermal Shutdown

The SGM2048 can detect the temperature of die. When the die temperature exceeds the threshold value of thermal shutdown, the SGM2048 will be in shutdown state and remain in this state until the die temperature decreases to +150℃.

Power Dissipation (P_D)

Thermal protection limits power dissipation in the SGM2048. When power dissipation on pass element (P_D = (V_{IN} - V_{OUT}) × I_{OUT}) is too much that raise the operation junction temperature exceeds +170℃, the OTP circuit starts the thermal shutdown function and turns the pass element off.

Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. To guarantee reliable operation, the junction temperature of the SGM2048 must not exceed +125℃.

The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction temperature and ambient temperature. The maximum power dissipation can be approximated using the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (2)$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

Layout Guidelines

To get good PSRR, low output noise and high transient response performance, the input and output bypass capacitors must be placed as close as possible to the IN pin and OUT pin separately. V_{IN} and V_{OUT} had better use separate ground planes and these ground planes are single point connected to the GND pin.

REVISION HISTORY

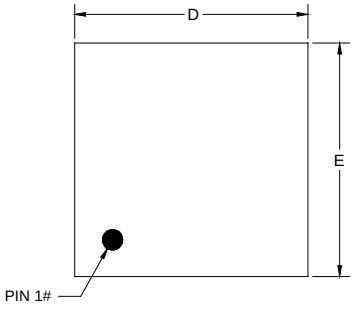
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MAY 2022 – REV.A to REV.A.1	Page
Updated Application Information section	13

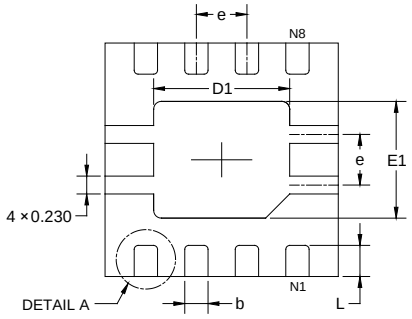
Changes from Original (JANUARY 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

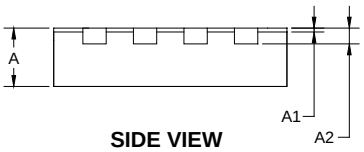
TDFN-3×3-8CL



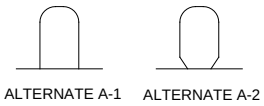
TOP VIEW



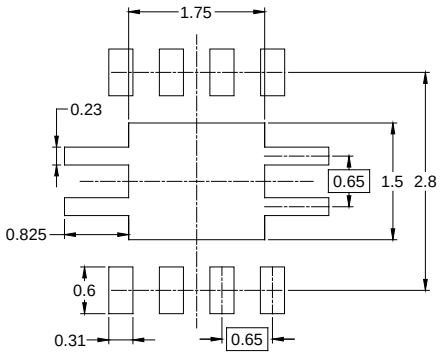
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



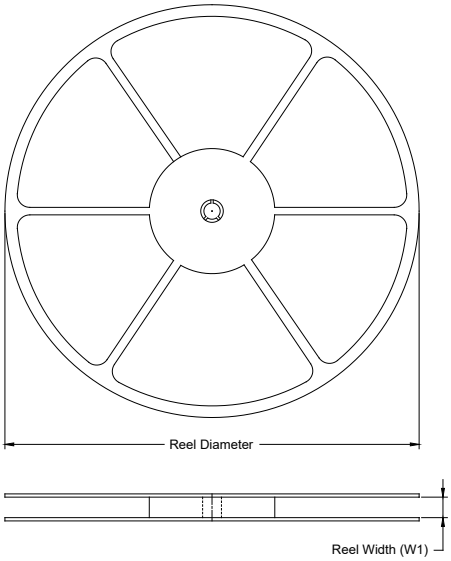
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	2.950	3.000	3.050
D1	1.700	1.750	1.800
E	2.950	3.000	3.050
E1	1.450	1.500	1.550
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.350	0.400	0.450

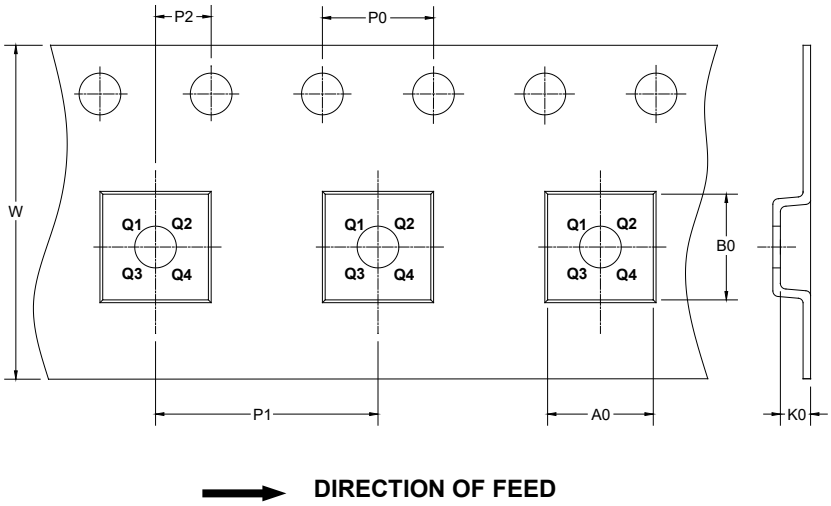
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



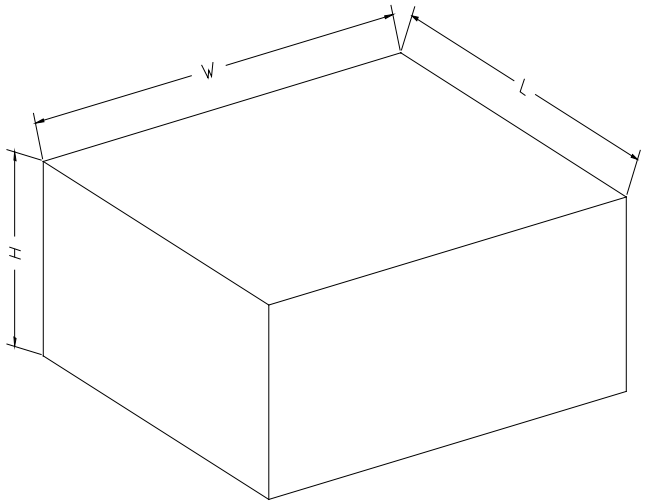
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-8CL	13″	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002