SGM61230
4.5V to 28V Input, 3A Output, Synchronous Step-Down Converter

GENERAL DESCRIPTION

The SGM61230 is a synchronous step-down converter with a wide input voltage range of 4.5V to 28V. This device can deliver up to 3A to the output over a wide input voltage. It is an easy-to-use device with power switches and peak current mode control compensation all integrated in a small 6-pin package. A typical 5ms soft-start ramp is also included to minimize the inrush current.

This device employs cycle-by-cycle peak current limit, output over-voltage protection and thermal shutdown with auto recovery. The current limit is implemented for both switches and has foldback feature to prevent overheating (and thermal shutdown) when an output short is detected. Auto recovery after over-current, output short, overheating or over-voltage fault maintains the system operational with no shutdown.

This converter has a fixed 410kHz switching frequency that minimizes the EMI noise problems. However the actual frequency drops during PSM (pulse skip mode) to maximize efficiency at light load. It also drops in some fault conditions.

The SGM61230 is available in a Green TSOT-23-6 package.

FEATURES

- **Wide 4.5V to 28V Input Voltage Range**
- **3A Continuous Output Current**
- **Integrated 66mΩ/36mΩ Power MOSFETs**
- **Low Quiescent Current: 25μA (TYP)**
- **Shutdown Current: 2μA (TYP)**
- **5ms Internal Soft-Start Time**
- **Fixed 410kHz Switching Frequency**
- **Pulse Skip Mode and PWM Mode**
- **Peak Current Mode Control**
- **Internal Loop Compensation**
- **Over-Current Protection for Both MOSFETs**
- **Output Over-Voltage Protection**
- **Adjustable Input Under-Voltage Lockout**
- **Thermal Shutdown with Auto Recovery**
- **Available in a Green TSOT-23-6 Package**

APPLICATIONS

12V Distributed Power Supply Buses
Industrial and Consumer Applications
White Goods
Audio Equipment
Set Top Boxes
Digital Television Printers

TYPICAL APPLICATION

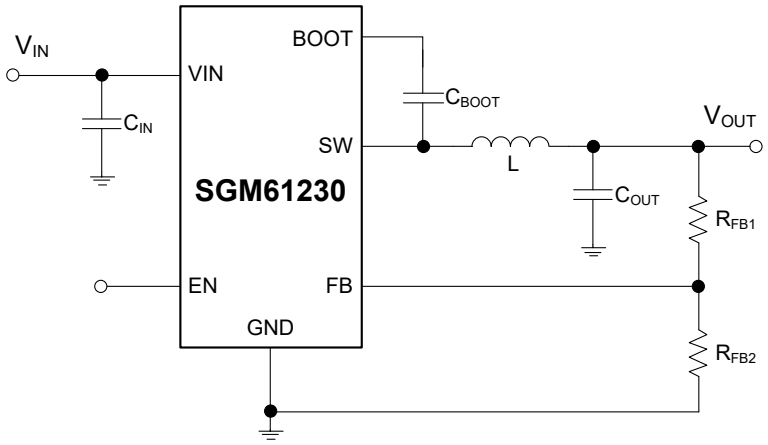


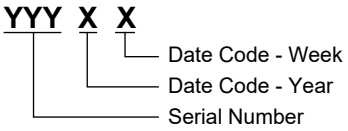
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61230	TSOT-23-6	-40℃ to +125℃	SGM61230XTN6G/TR	CE9XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.3V to 30V
EN and BOOT-SW Voltages ..... -0.3V to 6V
SW Voltage ..... -0.3V to 30V
SW (20ns transient) Voltage ..... -5V to 30V
FB Voltage ..... -0.3V to 3.5V
Package Thermal Resistance
TSOT-23-6, θ_{JA} ..... 123℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1500V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 4.5V to 28V
EN and BOOT-SW Voltages ..... -0.1V to 5.5V
SW Voltage ..... -0.1V to 28V
FB Voltage ..... -0.1V to 3V
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

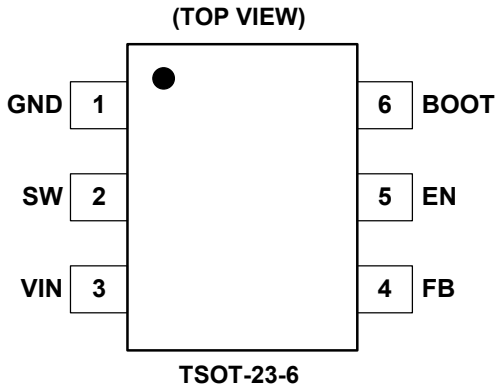
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	GND	–	Device Ground Reference Pin.
2	SW	O	Switching Node. Connection point of the internal converter lower and upper power MOSFETs. Connect this pin to the output inductor and the bootstrap capacitor.
3	VIN	–	Input Supply Voltage Pin. VIN powers the internal control circuitry and the power converter. Decouple this pin for very high frequency and high di/dt transitions, with small and high frequency ceramic capacitors placed as close as possible between VIN and GND pins. Input under-voltage is protected by a UVLO comparator.
4	FB	I	Feedback (Sense) Pin for Output Voltage and Programming. It is normally regulated at 0.603V. Tap an output feedback resistor divider to this pin.
5	EN	I	Device Enable Pin. Device will operate if EN voltage is high and will shut down if it is low. Device will be enabled if this pin is left float. EN pin can be used to increase the UVLO thresholds.
6	BOOT	O	Bootstrap Pin. Place a 0.1μF capacitor (C_{BOOT}) between BOOT and SW pins close to the device to provide the required drive voltage for the high-side switch. Do not place any series resistor with C_{BOOT}.

NOTE: O = Output, I = Input.

ELECTRICAL CHARACTERISTICS

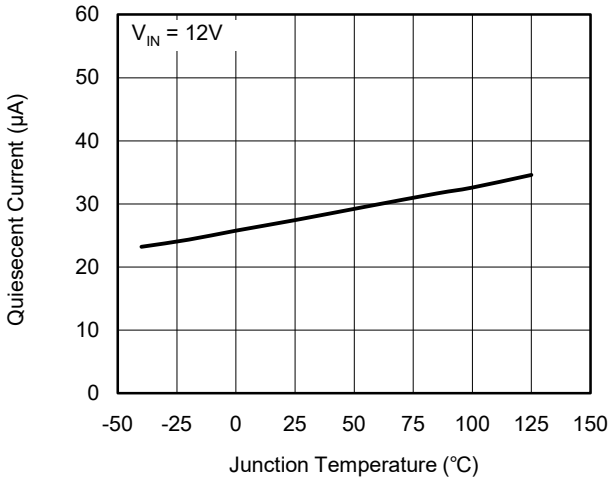
(T_J = -40℃ to +125℃, V_{IN} = 4.5V to 28V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		4.5		28	V
Non-Switching Quiescent Current	I_Q	V_{EN} = 5V, V_{FB} = 1V		25		μA
Shutdown Supply Current	I_{SD}	EN = GND		2		μA
EN Terminal Input Threshold	V_{IH}	Rising		1.19	1.33	V
	V_{IL}	Falling	0.93	1.10		
EN Terminal Leakage Current	I_{IL}	V_{EN} = 0.5V		0.45		μA
	I_{IH}	V_{EN} = 1.5V		1.44		
Feedback and Error Amplifier						
Feedback Voltage	V_{FB}	V_{IN} = 12V, T_J = +25℃	0.585	0.603	0.620	V
Power Stage						
High-side FET On-Resistance	R_{DSON_HS}	V_{BOOT} - V_{SW} = 5V		66	116	mΩ
Low-side FET On-Resistance	R_{DSON_LS}	V_{IN} = 12V		36	63	mΩ
Current Limit						
High-side Current Limit	I_{LIM_HS}	Maximum inductor peak current, T_J = +25℃	3.4	4.0	4.6	A
Low-side Current Limit	I_{LIM_LS}	Maximum inductor valley current, T_J = +25℃		3.4		A
Input Under-Voltage Lockout						
UVLO Threshold Voltage	V_{UVLO}	Rising V_{IN}		4.1	4.5	V
		Falling V_{IN}	3.4	3.7		
UVLO Hysteresis	V_{UVLO_HYS}			400		mV
Over-Temperature Protection						
Thermal Shutdown	T_{SHDN}	Rising Temperature		165		℃
Thermal Shutdown Hysteresis	T_{HYS}			10		℃
Oscillator						
Switching Frequency	f_{SW}		340	410	480	kHz
Timing Requirements						
Soft-Start Time	t_{SS}			5		ms

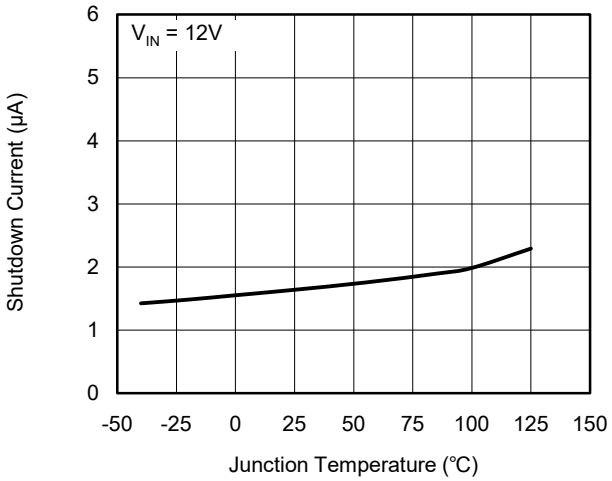
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN} = 4.5V to 28V, unless otherwise noted.

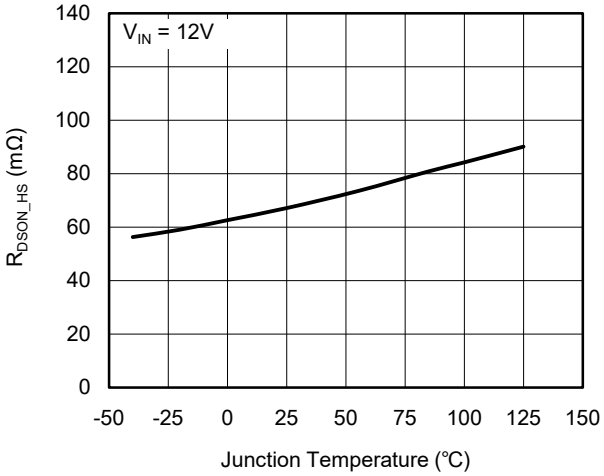
Quiescent Current vs. Junction Temperature



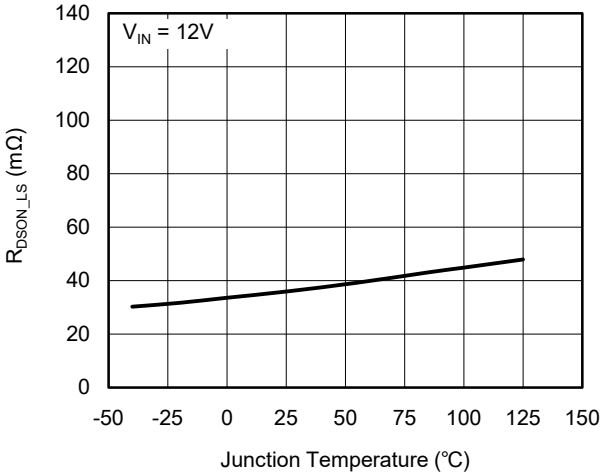
Shutdown Current vs. Junction Temperature



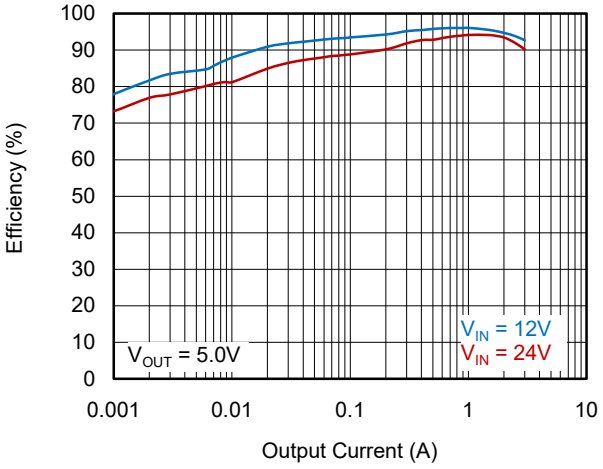
R_{DSON_HS} vs. Junction Temperature



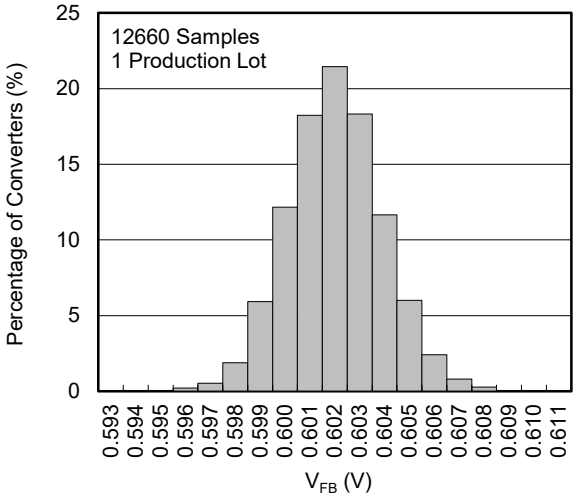
R_{DSON_LS} vs. Junction Temperature



Efficiency vs. Output Current



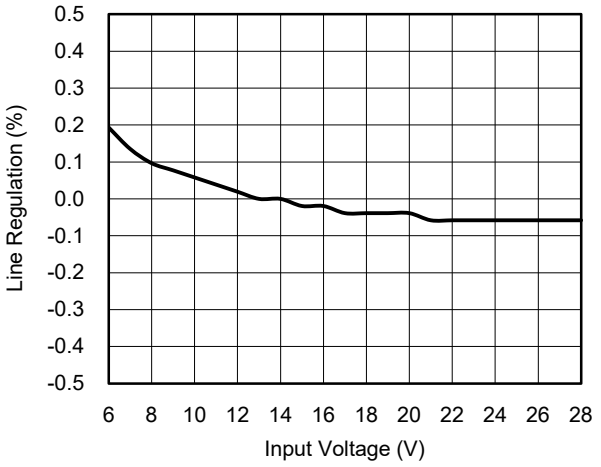
Feedback Voltage Production Distribution



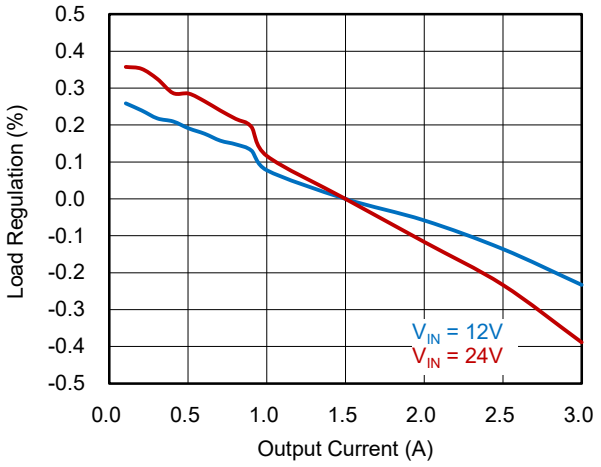
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 4.5V to 28V, unless otherwise noted.

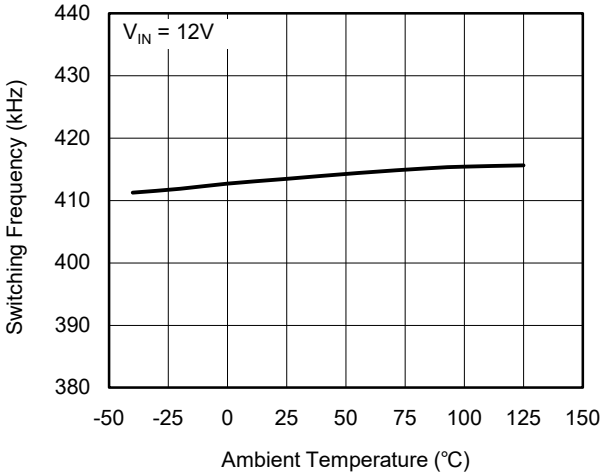
Line Regulation



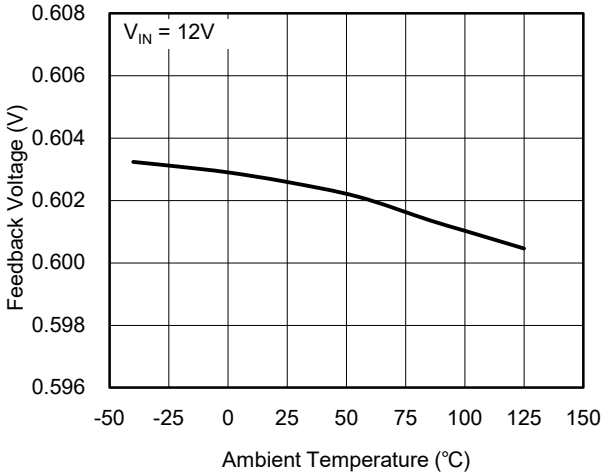
Load Regulation



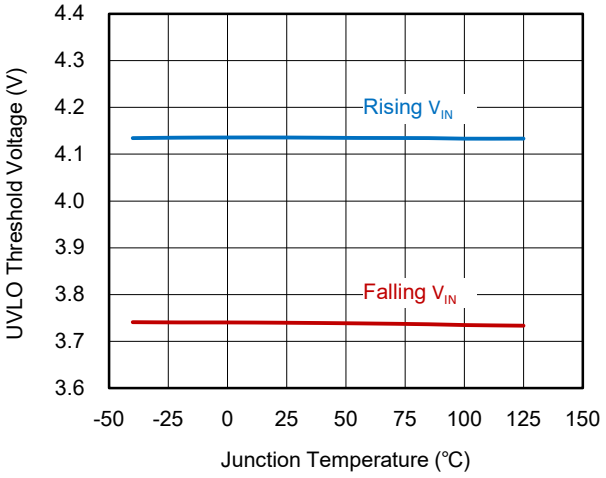
Switching Frequency vs. Ambient Temperature



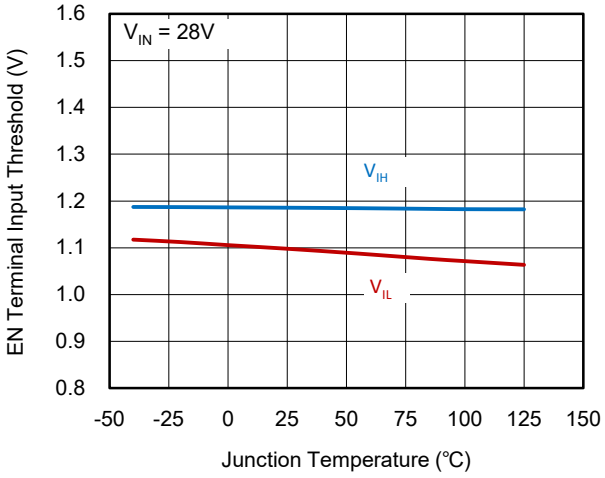
Feedback Voltage vs. Ambient Temperature



UVLO Threshold Voltage vs. Junction Temperature



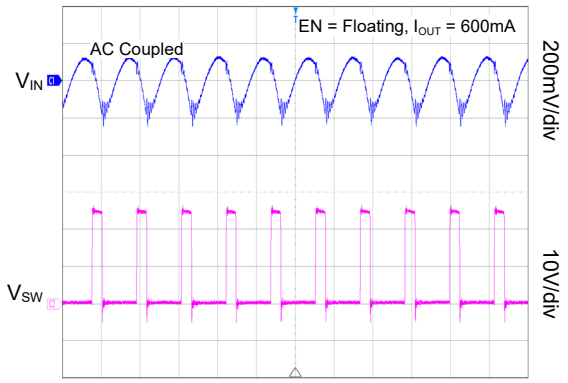
EN Terminal Input Threshold vs. Junction Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

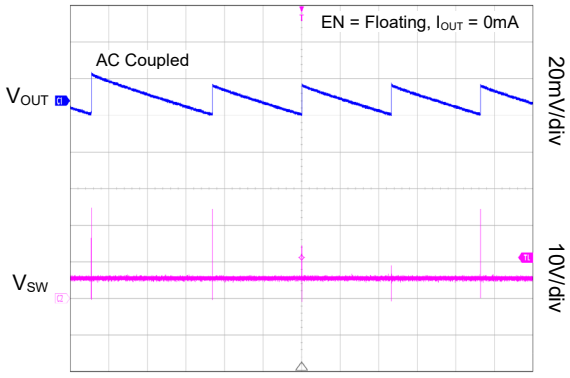
T_J = +25℃, V_{IN} = 24V, V_{OUT} = 5V, C_{IN} = 10μF, C_{OUT} = 2 × 22μF, unless otherwise noted.

Input Voltage Ripple



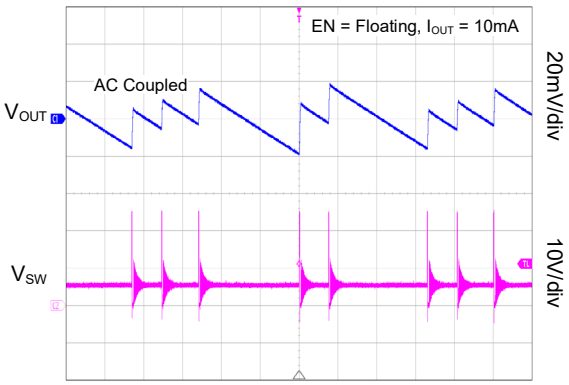
Time (2μs/div)

Output Voltage Ripple



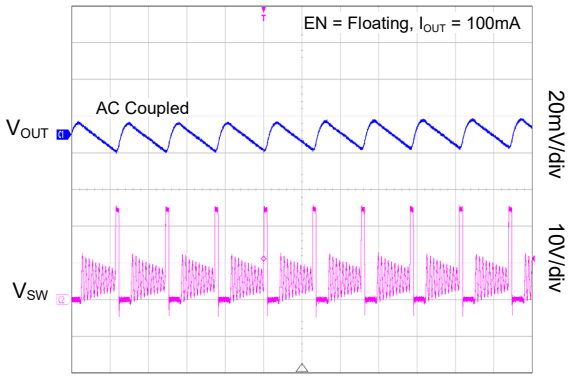
Time (4ms/div)

Output Voltage Ripple



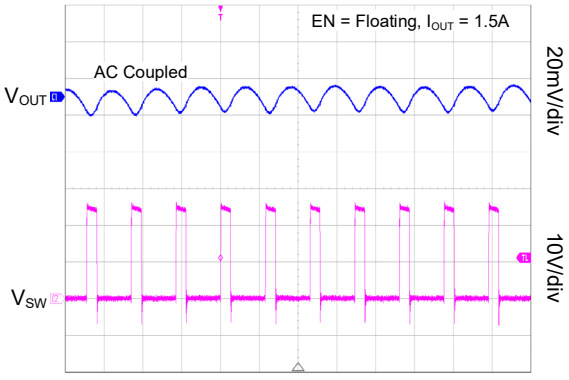
Time (40μs/div)

Output Voltage Ripple



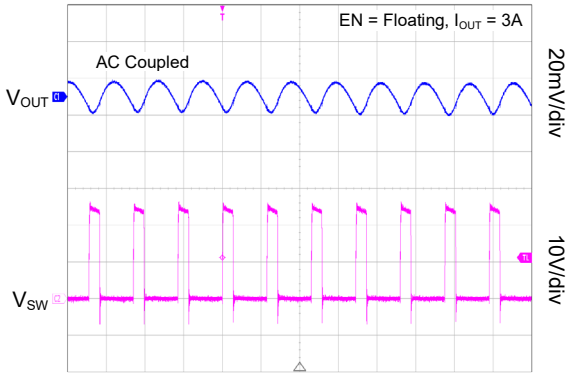
Time (4μs/div)

Output Voltage Ripple



Time (2μs/div)

Output Voltage Ripple

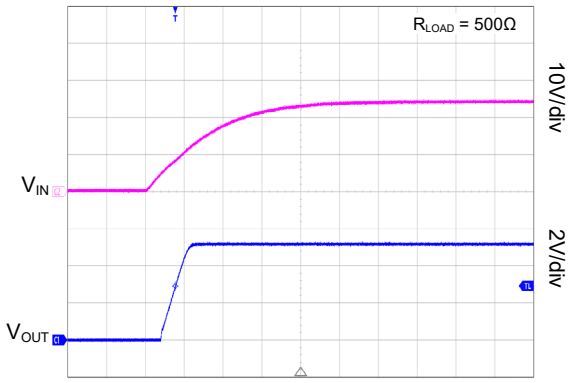


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

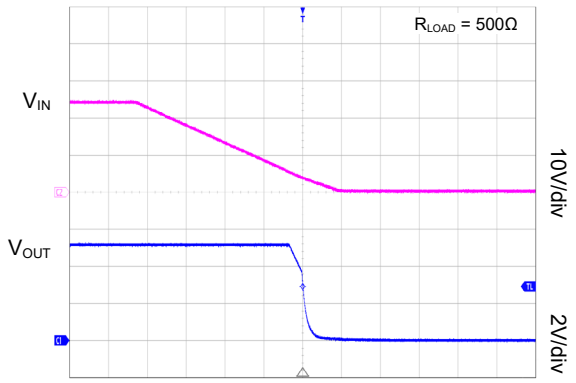
T_J = +25℃, V_{IN} = 24V, V_{OUT} = 5V, C_{IN} = 10μF, C_{OUT} = 2 × 22μF, unless otherwise noted.

Power On



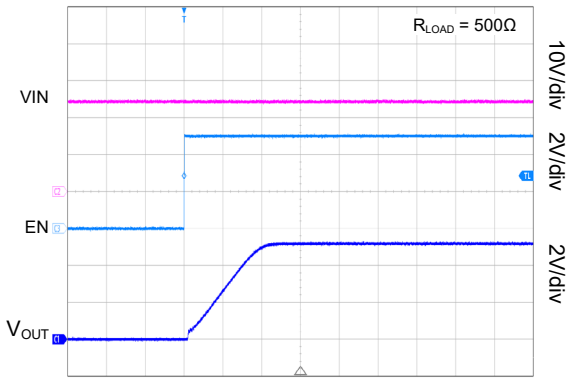
Time (5ms/div)

Power Off



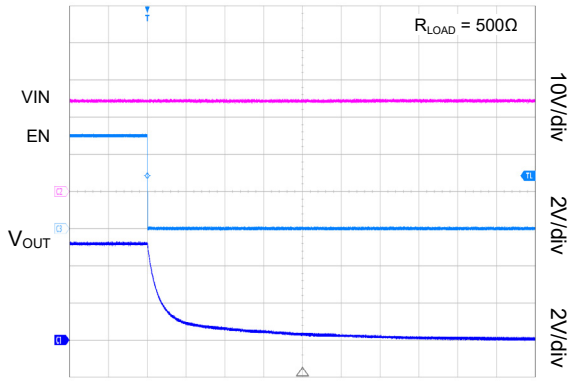
Time (50ms/div)

Turn On



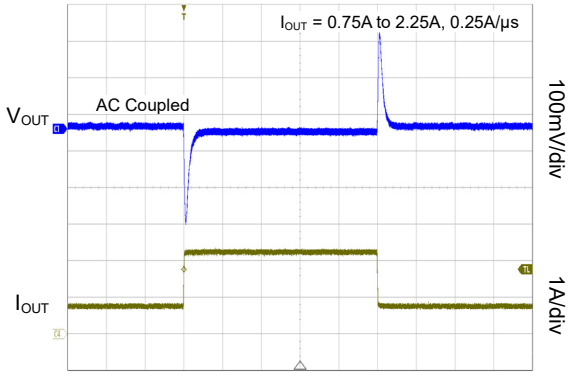
Time (2ms/div)

Turn Off



Time (10ms/div)

Load Transient Response



Time (200μs/div)

FUNCTIONAL BLOCK DIAGRAM

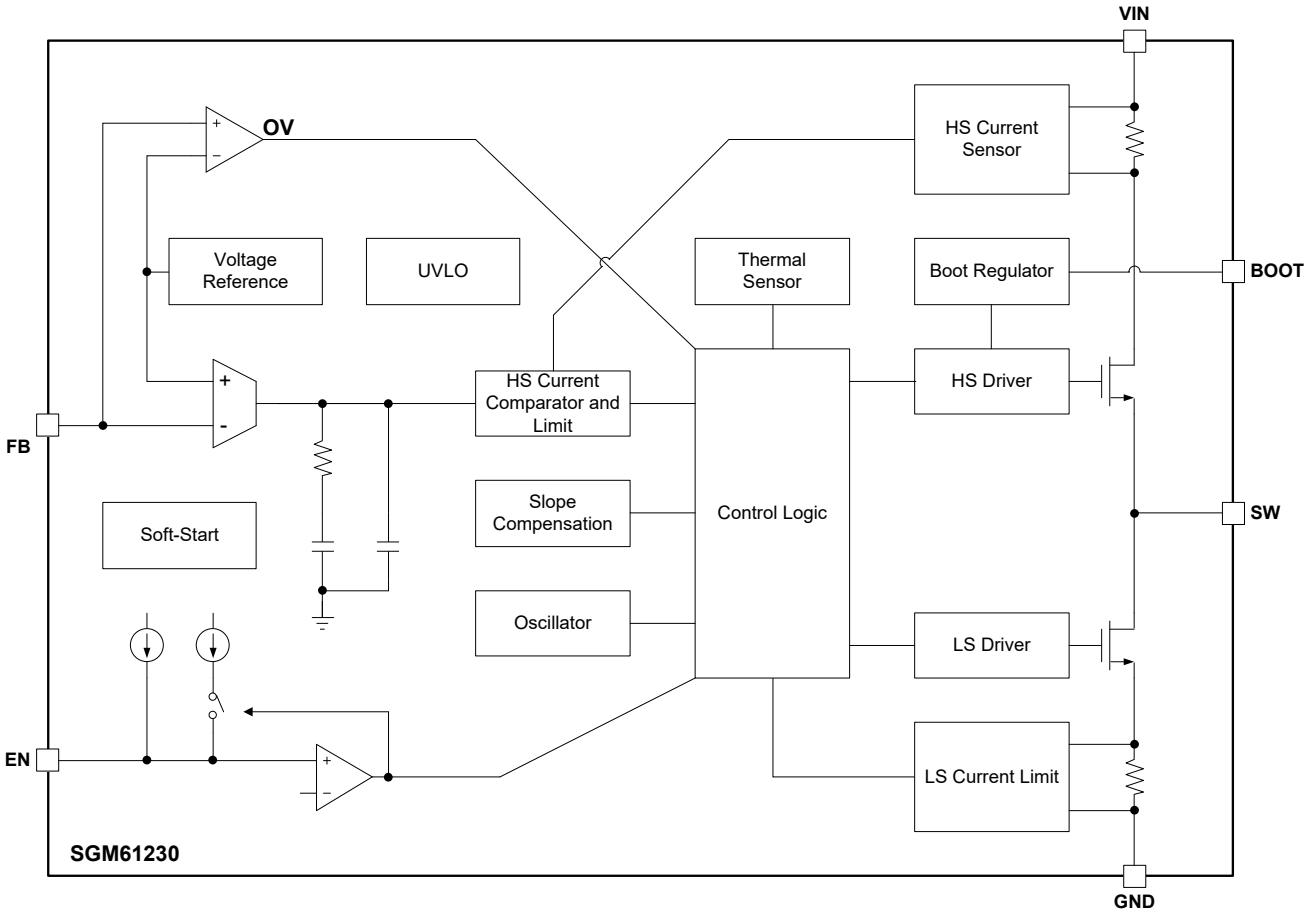


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61230 is a 28V/3A synchronous step-down converter with over-current, short-circuit and thermal shutdown with auto recovery. Figure 2 shows the simplified block diagram of the SGM61230. The two integrated MOSFET switches of the power stage (66mΩ high-side and 36mΩ low-side) can provide up to 3A of continuous current with high efficiency.

The device is powered up when V_{IN} exceeds the UVLO threshold (4.1V TYP). At no load and with no switching, the typical operating current is 25μA and when the device is disabled by EN pin, it is only 2μA (TYP). The internal loop compensation minimizes the BOM cost and simplifies the design. The inrush current is also limited by an internal 5ms soft-start ramp.

Operating Principle

Peak current mode (PCM) control is used in the SGM61230 to regulate the output voltage. V_{OUT} is sensed by the external resistor divider on the FB pin and compared to the internal 0.603V reference voltage by a trans-conductance error amplifier. The error amplifier (EA) output (current) is fed to the internal compensation components between the EA output and GND to generate a voltage that is used as the peak current reference for comparing with the sensed high-side switch current. The output of this comparator (COMP) can reset the flipflop that controls the switches. This flipflop receives fixed frequency clock pulses from the internal 410kHz oscillator. In the normal operation the high-side switch is turned on in the beginning of each switching cycle. The current in the high-side switch starts to rise until the peak current reference is reached that resets the flipflop. This will turn off the high-side switch and turn on the low-side switch. The low-side switch stays on until the end of the cycle.

Slope Compensation

Peak current mode-controlled devices in general are subject to sub-harmonic oscillation instability at higher duty cycles (typically > 50%). To avoid this instability a compensating ramp signal is used. The ramp starts from zero in the beginning of each cycle with a specific slop and is added to the sensed high-side switch current before it is compared to the peak current reference.

Anti-High-Overload Mode

The SGM61230 supports overload mode. When the output current continues overload while the system power up or in turbo mode, the SGM61230 exports the maximize power and limit the maximum peak current in high-side and valley current in low-side, the device keeps in cycle-by-cycle limit to obtain the system's power request. The SGM61230 does not shut down until the device heats and then goes to thermal shutdown. The load increase, the output voltage goes low, if the output voltage drops to 20%, the device will go into short protection. It reduces current limit threshold and the switching frequency goes down due to reduce power dissipation and device goes into thermal shutdown. When the output current is low enough, the device goes into PFM mode.

Pulse Skip Mode (PSM) and PWM Mode

In light load, OVP does not occur and the device can operate in the normal PWM mode, but to improve light load efficiency, the device is designed to skip some pulses by entering to the PSM mode. When the peak current is lower than 500mA typically, the device enters PSM. In PSM, when the output voltage is detected to be above the internal voltage reference level of the error amplifier, the high-side MOSFET is kept off for a few cycles (skipping clock pulses) by clamping current reference until the output voltages are discharged below the internal voltage reference level. Note that the integrated current comparator operates based on the peak inductor current and the average load current may vary depending on the output filters and load type.

Enable Pin and UVLO Adjustment

The EN pin can be used to turn the device on and off or to change the UVLO thresholds. The device is enabled when the EN pin voltage exceeds its high threshold. A low EN voltage disables the device brings it to the low-quiescent (I_Q) state.

The EN pin is internally pulled up by a small current source (I_P) so the device is enabled if EN pin is floated. An open drain or open collector output can be used to control the EN pin.

V_{IN} is monitored by the internal under-voltage lockout circuit and if it is below UVLO threshold, the device is disabled. The internal UVLO has a 400mV hysteresis. If higher thresholds are needed, EN pin can be used as shown in Figure 3.

The EN pull-up current is used to set the hysteresis. The pull-up current is increased by I_{IH} - I_{IL} when the EN pin exceeds its high threshold. Use Equations 1 and 2 to calculate the R_1 and R_2 values for the desired UVLO low (V_{UV_L}) and high (V_{UV_H}) thresholds.

DETAILED DESCRIPTION (continued)

$$R_1 = \frac{V_{UV_H} \times V_{IL} - V_{UV_L} \times V_{IH}}{I_{IH} \times V_{IH} - I_{IL} \times V_{IL}} \quad (1)$$

$$R_2 = \frac{R_1 \times V_{IL}}{V_{UV_L} - V_{IL} + R_1 \times I_{IH}} \quad (2)$$

where:
I_{IL} = 0.45μA (TYP)
I_{IH}= 1.44μA (TYP)
V_{IL} = 1.10V (TYP)
V_{IH} = 1.19V (TYP)

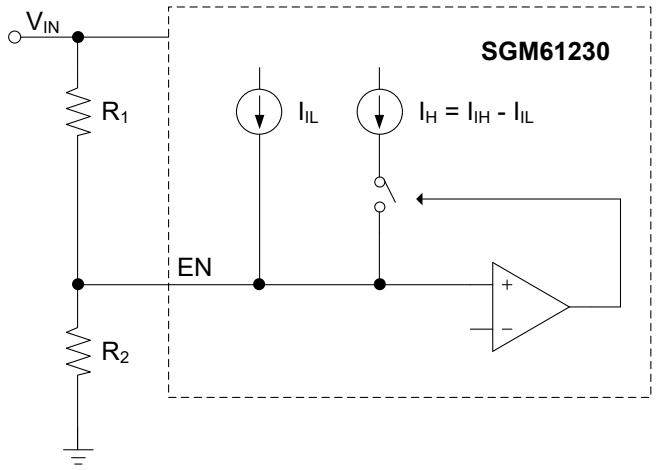


Figure 3. Adjustable VIN Under-Voltage Lockout

Output Voltage Programming

The output voltage is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use resistors with 1% tolerance or better because it directly affects the output accuracy. Use Equation 3 and Figure 1 to calculate the output voltage. To improve efficiency at light load consider larger resistors. Start with 100kΩ for the upper resistor (R_{FB1}). Note that if $R_{FB1}||R_{FB2}$ is too high, the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{FB} \times \left[\frac{R_{FB1}}{R_{FB2}} + 1\right] \quad (3)$$

Internal Voltage Reference and Soft-Start

The SGM61230 device has an internal 0.603V reference (V_{REF}) to program the output at the desired level. The output voltage is determined by the reference voltage seen by the error amplifier. When the converter starts (or is enabled), an internal ramp voltage begins to rise from near 0V to slightly above 0.603V with a ramp time of 5ms. The lower of V_{REF} and this ramp is used as reference for the error amplifier, therefore during startup the ramp provides a soft-start for the output. The soft-start is needed to avoid high inrush currents caused by rapid increase of output voltage across output capacitors and the load. Without a soft-start the current limiting protections could trigger that interrupts the monotonic rising of the load voltage that may result in instability or improper system initialization.

Bootstrap Voltage (BOOT)

To power the upper switch gate driver, a voltage higher than V_{IN} is needed. Bootstrapping technique is used to provide this voltage from the switching node by using a 0.1μF bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode. The voltage is internally regulated for driving the high-side switch. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations. To improve drop out, the device is designed to operate at 100% duty cycle.

Output Short-Circuit Protection

When the output voltage down to 20% of set value, the device goes into short-circuit mode, and a foldback mode will limit the current output. The high-side peak current limit to 2.4A (TYP) and the valley current limit to 1.4A (TYP), then it avoids the device thermal shutdown by the power dissipation.

A short-circuit is detected when V_{FB} falls below 0.12V (TYP). In this condition the current limits of both switches are internally reduced to less than half of the normal value (foldback). This will reduce the constant output current during an output short and prevents overheating. During the soft-start period there is no foldback and the current limits are normal.

Output Over-Voltage Protection (OVP)

An over-voltage protection is included in the device to minimize the output voltage overshoots that may occur after recovery from an output fault or a large unloading transient. The FB pin voltage is compared with the OVP thresholds. If the V_{FB} exceeds 108% of the V_{REF}, the high-side switch is forced to turn off. When the V_{FB} falls below 104%, the high-side switch is allowed to turn on again.

DETAILED DESCRIPTION (continued)

Over-Current Protection (OCP)

The device is protected from over-current conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs.

High-side MOSFET Over-Current Protection

The internal peak current mode controller provides an inherent current limiting capability for the high-side switch on a cycle-by-cycle basis. When high-side switch current exceeds peak current limit threshold, high-side switch is turned off, until the next cycle.

Low-side MOSFET Over-Current Protection

The low-side MOSFET current is also monitored for over-current protection. Normally this MOSFET sources current to the load (source to drain direction) while the inductor current is decreasing. At the end of each cycle, this current is compared to the preset low-side current-limit (I_{LIM_LS}). If the inductor valley current exceeds the low-side current limit, the high-side MOSFET will not turn on in the next cycle and the low-side MOSFET continues to conduct (cycle skipped). The high-side switch turns on again when the valley current falls below I_{LIM_LS} at the start of another cycle (Figure 4).

During an over-current fault, the above limits cause cycle skipping that slows down the switching frequency and reduces the output voltage (due to reduced duty cycle).

Thermal Shutdown

If the junction temperature exceeds +165℃ (TYP), the device is forced to stop switching. It will recover automatically when T_J falls below the recovery threshold.

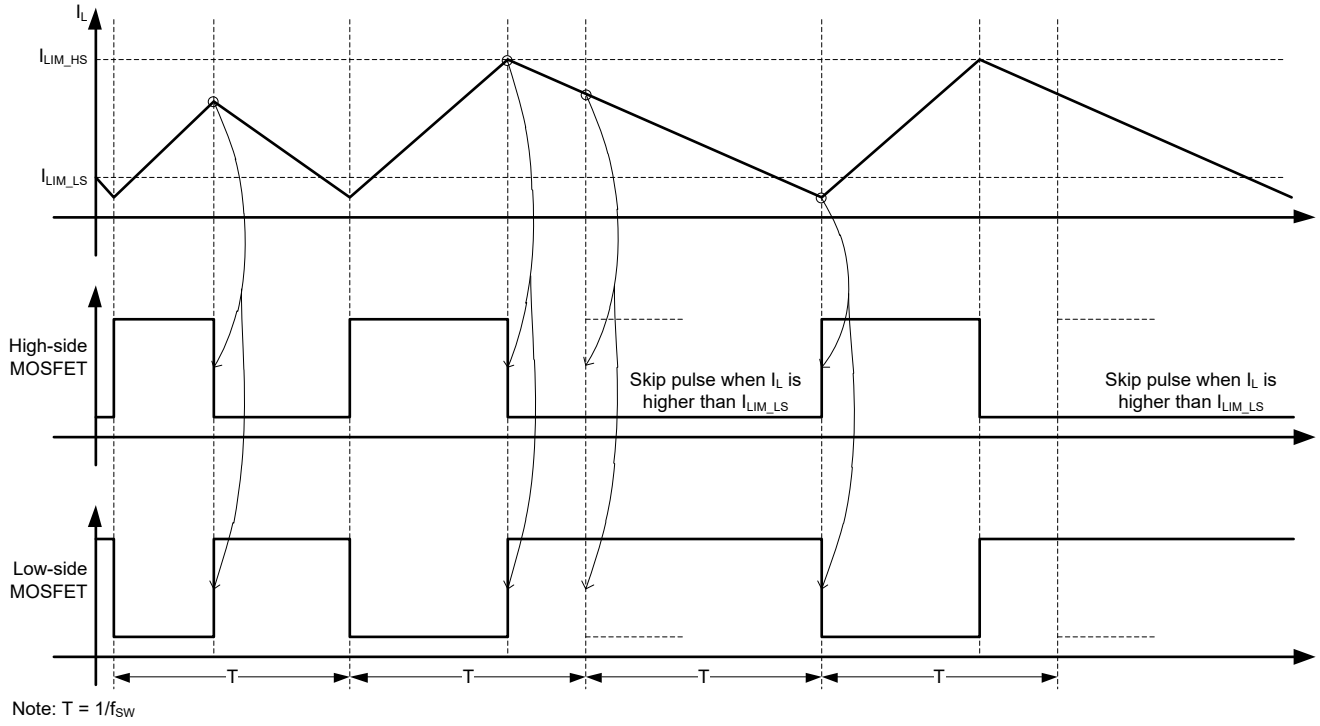


Figure 4. Over-Current Protection for MOSFETs

APPLICATION INFORMATION

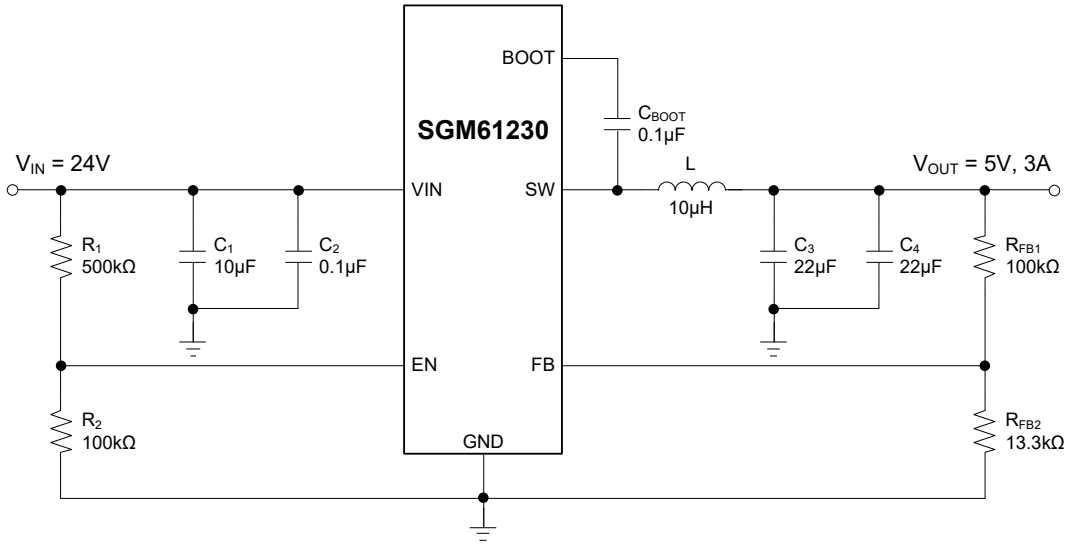


Figure 5. A Reference Design for 5V, 3A Application

Design Requirements

- A 10pF feedforward capacitor is optioned to improve the response.
- When the output is shorted, a large input capacitor is required to ensure that the output voltage ripple is lower than 1V, otherwise the device may not be stable.
- To reduce the output ripple and keep the device stable, the output capacitor must be large. The recommended value should not be lower than 22μF + 22μF, and a 100μF output capacitor will be very helpful for reducing ripple.
- 0.1% R_{FB1}, R_{FB2} will be chosen to improve the output voltage precision, if it is needed.
- In order to obtain a small V_{OUT} ripple, it is recommended that the V_{IN} is higher than 7V when the V_{OUT} is 5V, and the V_{IN} is lower than 20V when the V_{OUT} is 1.8V.

Layout Guide

Layout guide schematic for PCB Layout.

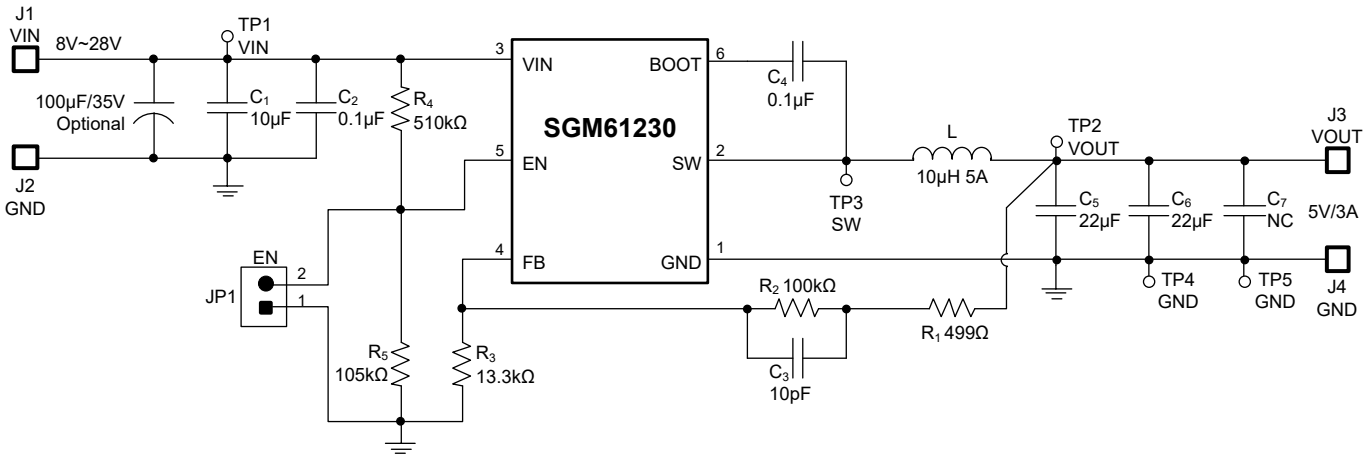


Figure 6. Schematic for PCB Layout

APPLICATION INFORMATION (continued)

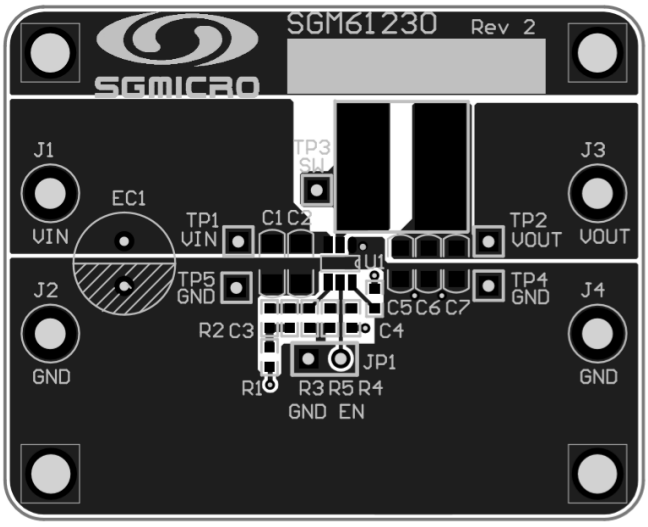


Figure 7. PCB Top Layer

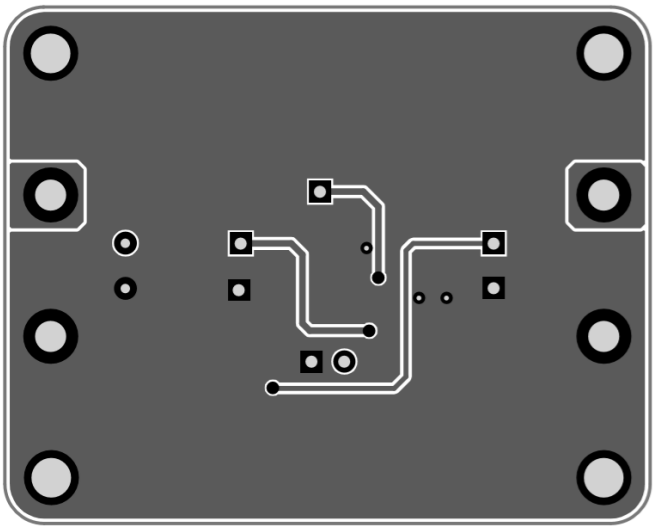


Figure 8. PCB Bottom Layer

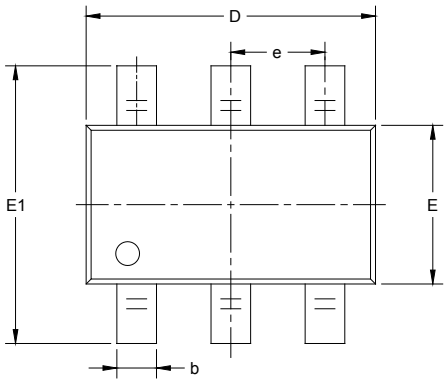
REVISION HISTORY

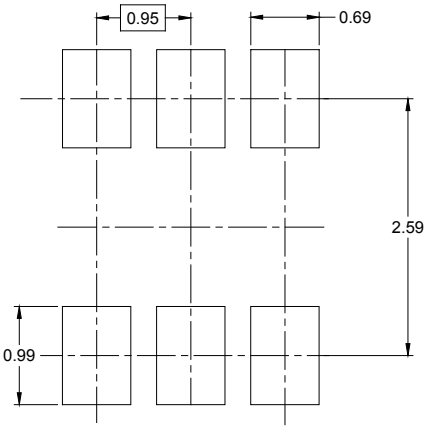
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2020) to REV.A	Page
Changed from product preview to production data	All

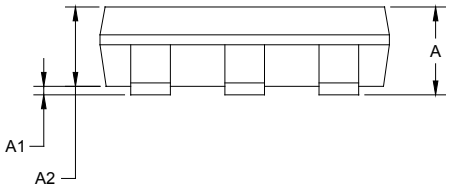
PACKAGE OUTLINE DIMENSIONS

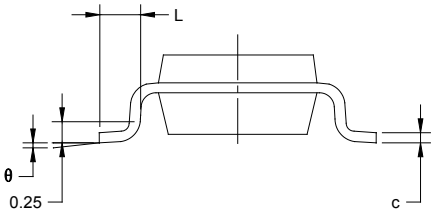
TSOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)

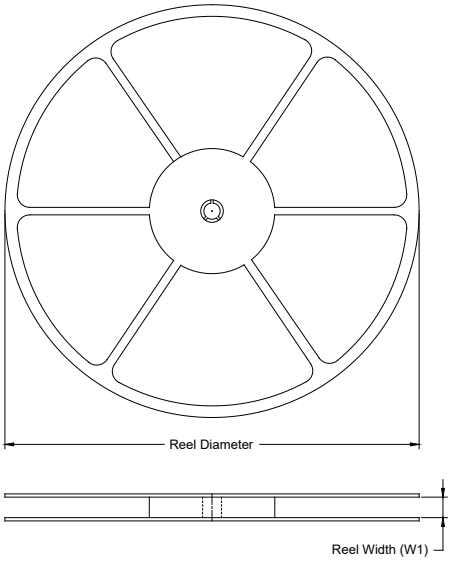




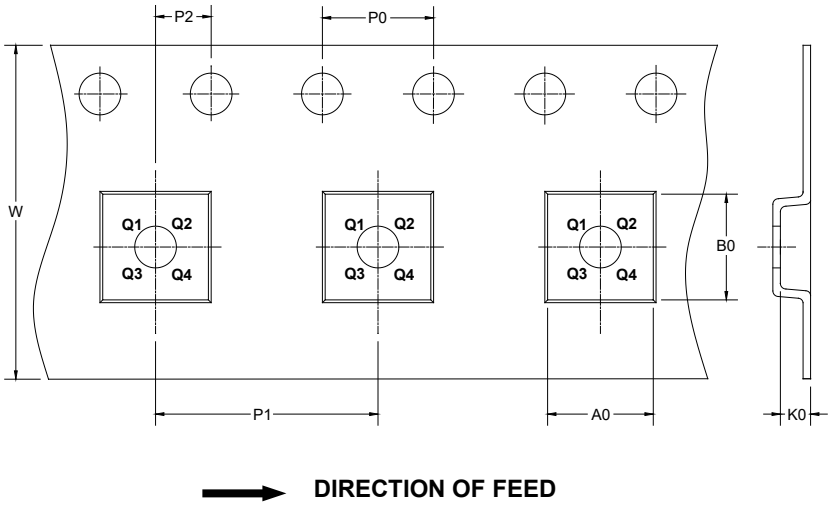
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.000		0.043
A1	0.000	0.100	0.000	0.004
A2	0.700	0.900	0.028	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.200	0.003	0.008
D	2.850	2.950	0.112	0.116
E	1.550	1.650	0.061	0.065
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



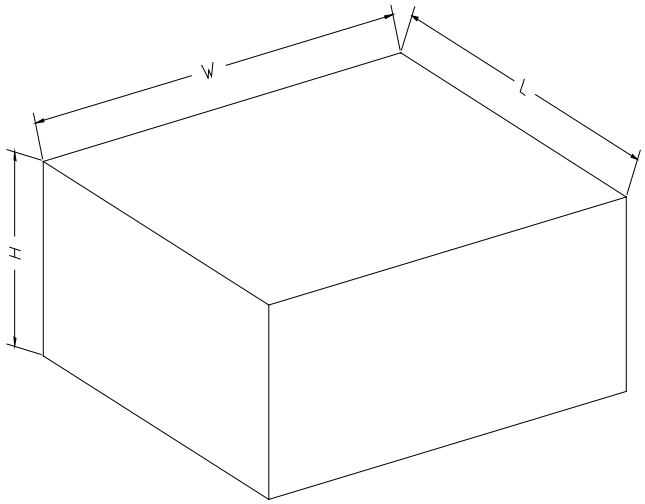
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-6	7″	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002