SGM4029
Low Noise, Low Drift, Precision Voltage Reference

GENERAL DESCRIPTION

The SGM4029 is a low noise, low drift, high precision voltage reference. The reference is capable of both sinking and sourcing current, and has excellent line and load regulation.

Excellent temperature drift (5ppm/℃ TYP) and high accuracy (±0.05% TYP) are achieved using proprietary design techniques. These features, combined with very low noise, make the SGM4029 ideal for use in high-precision data acquisition systems.

The SGM4029 is available in Green SOIC-8 and MSOP-8 packages. It operates an operating temperature range of -40℃ to +125℃.

FEATURES

- **Low Temperature Drift:**
  5ppm/℃ (TYP), 10ppm/℃ (MAX)
- **High Accuracy: ±0.05% (TYP), ±0.1% (MAX)**
- **Low Noise: 3μV_{PP}/V**
- **Excellent Long-Term Stability:**
  50ppm/1000 hour (TYP) First 1000 Hours
  25ppm/1000 hour (TYP) Second 2000 Hours
- **High Output Current: ±10mA**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-8 and MSOP-8 Packages**

APPLICATIONS

Precision Data Acquisition Systems
Semiconductor Test Equipment
Industrial Process Controls
Medical Instrumentation
Pressure and Temperature Transmitters
Lab and Field Instrumentation

SIMPLIFIED SCHEMATIC

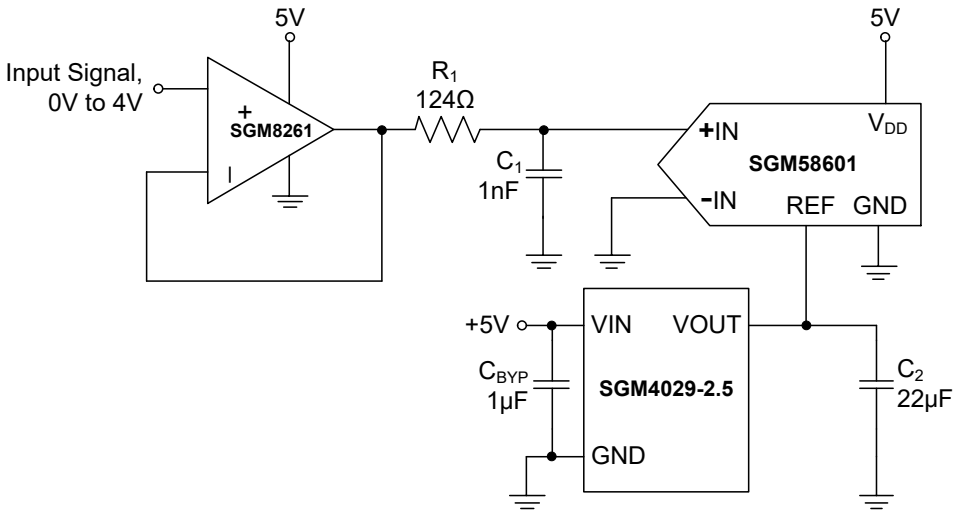


Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4029-2.048	SOIC-8	-40℃ to +125℃			
	MSOP-8	-40℃ to +125℃			
SGM4029-2.5	SOIC-8	-40℃ to +125℃			
	MSOP-8	-40℃ to +125℃			
SGM4029-3.0	SOIC-8	-40℃ to +125℃			
	MSOP-8	-40℃ to +125℃			
SGM4029-4.096	SOIC-8	-40℃ to +125℃			
	MSOP-8	-40℃ to +125℃			
SGM4029-4.5	SOIC-8	-40℃ to +125℃			
	MSOP-8	-40℃ to +125℃			
SGM4029-5.0	SOIC-8	-40℃ to +125℃			
	MSOP-8	-40℃ to +125℃			
SGM4029-10	SOIC-8	-40℃ to +125℃			
	MSOP-8	-40℃ to +125℃			

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.2V to 18V
Output Short Circuit ..... -30mA to 30mA
Package Thermal Resistance
SOIC-8, θ_{JA} ..... ℃/W
SOIC-8, θ_{JB} ..... ℃/W
SOIC-8, $\theta_{JC(TOP)}$ ..... ℃/W
SOIC-8, $\theta_{JC(BOT)}$ ..... ℃/W
MSOP-8, θ_{JA} ..... ℃/W
MSOP-8, θ_{JB} ..... ℃/W
MSOP-8, $\theta_{JC(TOP)}$ ..... ℃/W
MSOP-8, $\theta_{JC(BOT)}$ ..... ℃/W
Operating Temperature Range ..... -55℃ to +125℃
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 400V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... V_{OUT} + 0.2V (1) to 18V
Output Current Range ..... -10mA to 10mA

NOTE: Except for the SGM4029-2.048, where V_{IN} (MIN) = 2.7V.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

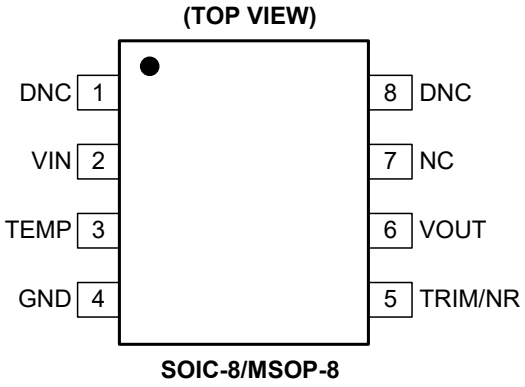
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
SOIC-8/MSOP-8		
1, 8	DNC	Do Not Connect. Don’t connect with any external device in application.
2	VIN	Power Supply.
3	TEMP	Temperature Monitoring Pin. Provides a temperature-dependent output voltage.
4	GND	Ground.
5	TRIM/NR	Output Adjustment and Noise Reduction Pin.
6	VOUT	Reference Voltage Output.
7	NC	No Internal Connection.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (V_{OUT} + 0.2V) to 18V, I_{LOAD} = 0mA and C_L = 1μF, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	V_{OUT}	SGM4029-2.048 (V_{OUT} = 2.048V) (1), 2.7V < V_{IN} < 18V		2.048		V
		SGM4029-2.5		2.5		
		SGM4029-3.0		3.0		
		SGM4029-4.096		4.096		
		SGM4029-4.5		4.5		
		SGM4029-5.0		5.0		
		SGM4029-10		10.0		
Initial Accuracy			-0.1		0.1	%
Output Voltage Noise		f = 0.1Hz to 10Hz		3		$\mu V_{PP}/V$
Output Voltage Temperature Drift	dV_{OUT}/dT			5	10	ppm/℃
Line Regulation	$\Delta V_{O(\Delta VI)}$	V_{IN} = (V_{OUT} + 0.2V) to 18V (2)		0.1	1	ppm/V
		V_{IN} = V_{OUT} + 0.2V, T_A = -40℃ to +125℃ (2)		0.2	1	ppm/V
Load Regulation	$\Delta V_{O(\Delta IL)}$	-10mA < I_{LOAD} < 10mA, V_{IN} = V_{OUT} + 0.75V (3)		20	30	ppm/mA
		-10mA < I_{LOAD} < 10mA, V_{IN} = V_{OUT} + 0.75V, T_A = -40℃ to +125℃ (3)			50	ppm/mA
Short Circuit Current	I_{SC}	V_{OUT} = 0V		25		mA
Thermal Hysteresis		High Grade, VSSOP-8, Cycle 1		50		ppm
		Standard Grade, VSSOP-8, Cycle 1		70		ppm
		High Grade, SOIC-8, Cycle 1		70		ppm
		Standard Grade, SOIC-8, Cycle 1		90		ppm
		High Grade, VSSOP-8, Cycle 2		40		ppm
		Standard Grade, VSSOP-8, Cycle 2		40		ppm
		High Grade, SOIC-8, Cycle 2		50		ppm
		Standard Grade, SOIC-8, Cycle 2		50		ppm
Long-Term Stability		VSSOP-8, 0 to 1000 hours		50		ppm/1000hr
		VSSOP-8, 1000 to 2000 hours		25		ppm/1000hr
		SOIC-8, 0 to 1000 hours		100		ppm/1000hr
		SOIC-8, 1000 to 2000 hours		50		ppm/1000hr
TEMP Pin Voltage Output		T_A = +25℃		575		mV
TEMP Pin Temperature Sensitivity		T_A = -40℃ to +125℃		2.64		mV/℃
TEMP Pin Turn-On Settling Time		To 0.1% with C_L = 1μF		200		μs
Supply Voltage Range (1)	V_{IN}		V_{OUT} + 0.2		18	V
Quiescent Current				1.5	2.0	mA
		T_A = -40℃ to +125℃			2.0	
Specified Temperature Range			-40		125	℃
Operating Temperature Range			-55		125	℃

NOTES:
1. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7V.
2. Except for SGM4029-2.048, where V_{IN} = 2.7V to 18V.
3. Except for SGM4029-2.048, where V_{IN} = 3V.

FUNCTIONAL BLOCK DIAGRAM

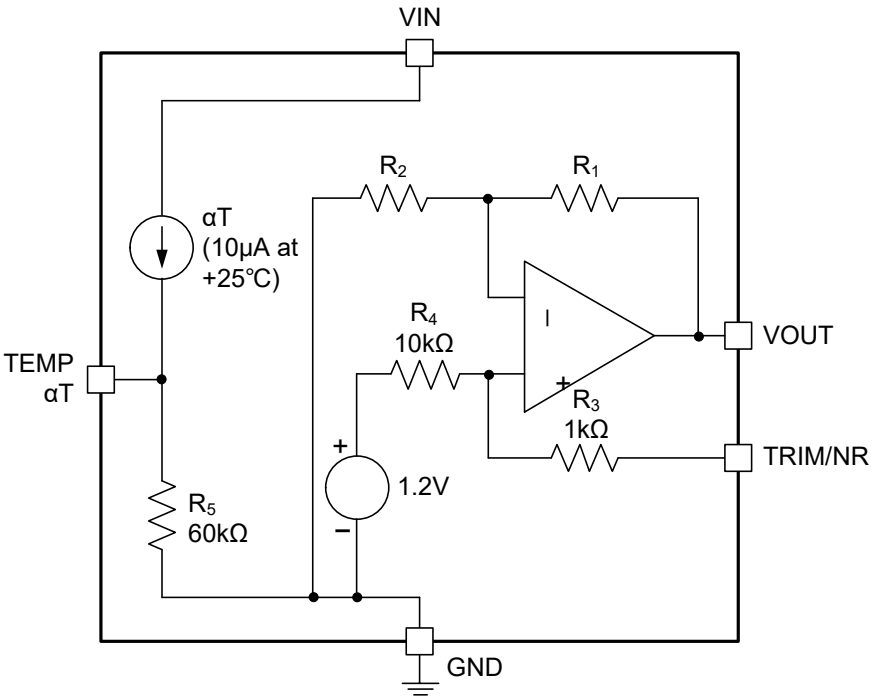


Figure 2. Block Diagram

PARAMETER MEASUREMENT INFORMATION

Solder Heat Shift

The materials used in the manufacture of the SGM4029 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device can cause the output voltages to shift, degrading the initial accuracy and drift specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 36 devices were soldered on printed-circuit-boards using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 3. The printed-circuit-board is comprised of FR4 material. The board thickness is 0.8 mm and the area is 13 mm × 13 mm.

The reference voltage is measured before and after the reflow process across temperature; the typical shift of accuracy and drift is displayed in Figure 4 through Figure 5. Although all tested units exhibit very low shifts, higher shifts are also possible depending on the size, thickness, and material of the printed-circuit-board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on printed circuit boards (PCBs) with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, then solder the device in the last pass to minimize device exposure to thermal stress.

Figure 3. Reflow Profile

Figure 4. Solder Heat Shift Distribution (%), SOIC Package

Figure 5. Drift Shift Distribution,MSOP Package

DETAILED DESCRIPTION

The SGM4029 is a low noise, precision bandgap voltage reference that is specifically designed for excellent initial voltage accuracy and drift. See the Functional Block Diagram for a simplified block diagram of the SGM4029.

Temperature Monitoring

The temperature output terminal (TEMP, pin 3) provides a temperature dependent voltage output with approximately 60kΩ source impedance. The output voltage follows the nominal relationship:

$$V_{TEMP} = 509mV + 2.64 \times T(℃) \quad (1)$$

This pin indicates general chip temperature, accurate to approximately ±15℃. Although not generally suitable for accurate temperature measurements, this pin can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30℃ corresponds to an approximate 79mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see the Functional Block Diagram). Loading this pin with a low impedance circuit induces a measurement error; however, this pin does not have any effect on V_{OUT} accuracy.

To avoid errors caused by low impedance loading, buffer the TEMP pin output with a suitable low temperature drift op amp, as shown in Figure 6.

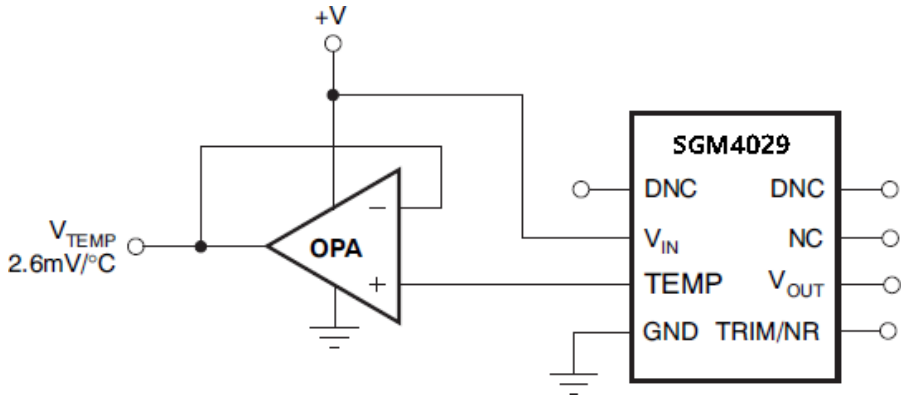


Figure 6. Buffering the TEMP Pin Output

Temperature Drift

The SGM4029 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described in Equation 2.

$$Drift = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times Temp\ Range} \right) \times 10^6 (ppm) \quad (2)$$

The SGM4029 features a maximum drift coefficient of 3ppm/℃ for the high-grade version, and 8ppm/℃ for the standard grade.

Thermal Hysteresis

Thermal hysteresis for the SGM4029 is defined as the change in output voltage after operating the device at +25℃, cycling the device through the specified temperature range, and returning to +25℃. Thermal hysteresis can be expressed as Equation 3:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \times 10^6 (ppm) \quad (3)$$

where:

V_{HYST} = thermal hysteresis (in units of ppm).

V_{NOM} = the specified output voltage.

V_{PRE} = output voltage measured at +25℃ pre-temperature cycling.

V_{POST} = output voltage measured after the device has been cycled from +25℃ through the specified temperature range of -40℃ to +125℃ and returned to +25℃.

DETAILED DESCRIPTION (continued)

Noise Performance

Typical 0.1Hz to 10Hz voltage noise for the SGM4029 is specified in the Electrical Characteristics table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although take care to ensure the output impedance does not degrade performance. One 1μF ceramic capacitor can be connected between TRIM/NR pin and GND to reduce noise.

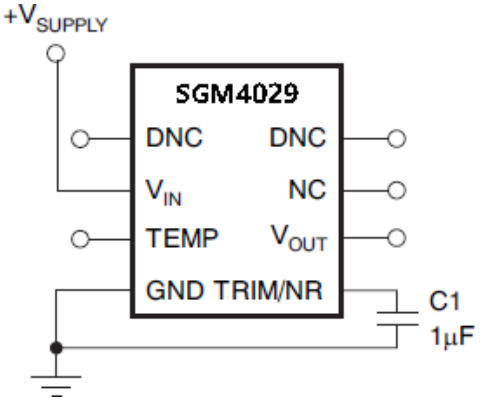


Figure 7. Noise Reduction Using the TRIM/NR Pin

Long Term Stability

Due to aging and environmental effects, all semiconductor devices experience physical changes of the semiconductor die and the packaging material over time. These changes and the associated package stress on the die cause the output voltage in precision voltage references to deviate over time. The value of such change is specified on the datasheet by a parameter called the Long-term stability (also known as the Long Term Drift (LTD)). Equation 4 shows how LTD is calculated. Note that the LTD value will be positive if the output voltage drifts higher over time, negative if the voltage drifts lower over time.

$$LTD(ppm)|_{t=n} = \left(\frac{V_{OUT}|_{t=0} - V_{OUT}|_{t=n}}{V_{OUT}|_{t=0}} \right) \times 10^6 \qquad (4)$$

where

$LTD(ppm)|_{t=n}$ = Long term stability (in units of ppm).

$V_{OUT}|_{t=0}$ = Output voltage at time = 0 hr.

$V_{OUT}|_{t=n}$ = Output voltage at time = n hr.

Output Adjustment Using the TRIM/NR Pin

The SGM4029 provides a very accurate, factory-trimmed voltage output. However, V_{OUT} can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5).Figure 8 shows a typical circuit that allows an output adjustment of ±15mV

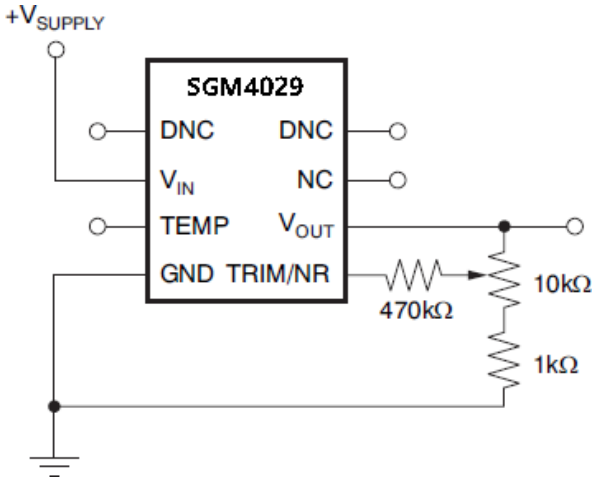


Figure 8. V_{OUT} Adjustment Using the TRIM/NR Pin

The SGM4029 allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (Figure 7) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of 1μF creates a low-pass filter with the corner frequency from 10Hz to 20Hz. Such a filter decreases the overall noise measured on the VOUT pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Using this capacitor increases start-up time.

DETAILED DESCRIPTION (continued)

Basic Connections

Figure 9 shows the typical circuit for the SGM4029. It is recommended a supply bypass capacitor ranging from 1μF to 10μF. A 1μF to 50μF output capacitor (C_L) must be connected from VOUT to GND. The equivalent series resistance (ESR) value of C_L must be less than or equal to 1.5Ω to ensure output stability. To minimize noise, the recommended ESR of C_L is from 1Ω and 1.5Ω.

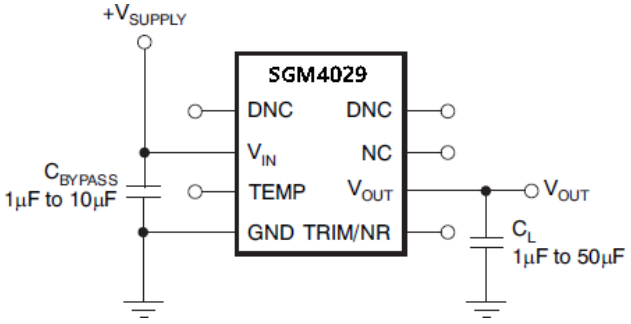


Figure 9. Basic Connections

Supply Voltage

The SGM4029 voltage reference features extremely low dropout voltage. With the exception of the SGM4029-2.048, which has a minimum supply requirement of 2.7V, these references can be operated with a supply of 200mV more than the output voltage in an unloaded condition.

Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the SGM4029 and SGM8263 can be used to generate positive and negative reference voltage from dual power supplies. Figure 10 shows the SGM4029-2.5 used to generate ±2.5V reference voltage. The low drift performance of the SGM4029 complements the low offset voltage and zero drift of the SGM8263 to generate low noise and low drift positive and negative V_{REF}. Take care to match the temperature coefficients of R_1 and R_2.

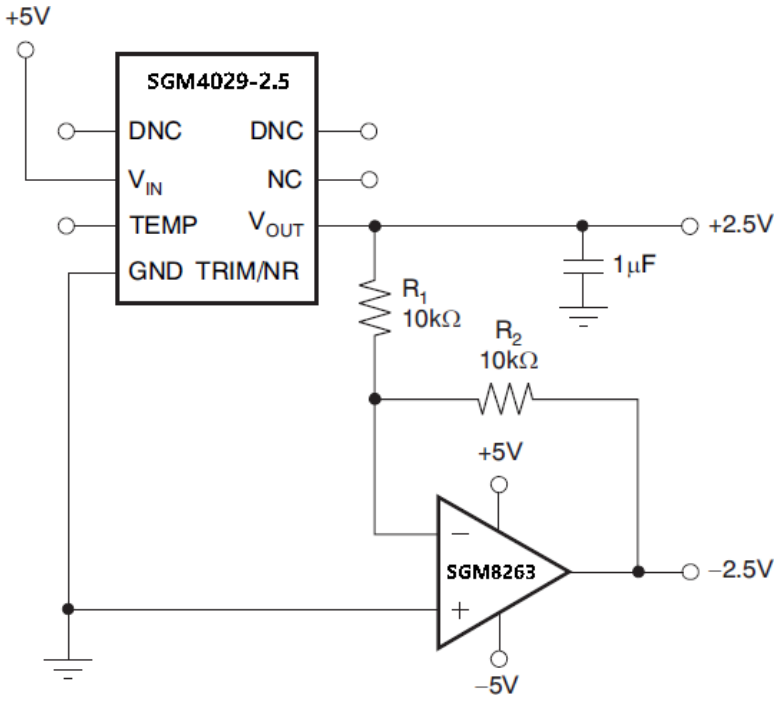


Figure 10. The SGM4029-2.5 and SGM8263 Create Positive and Negative Reference Voltages

APPLICATION INFORMATION

Data acquisition systems often require stable voltage references to maintain accuracy. The SGM4029 features low noise, low drift and high initial accuracy for high-performance data converters. Figure 11 shows the SGM4029-2.5 in a basic data acquisition system.

24-bit, 32KSPS Data Acquisition System

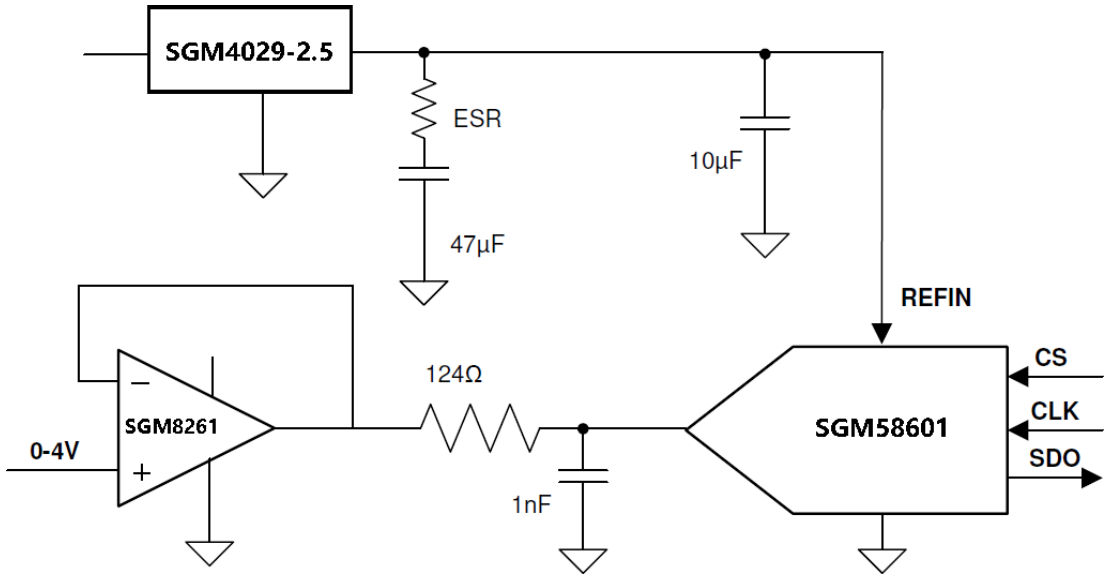


Figure 11. Complete Data Acquisition System Using SGM4029

Design Requirements

When using the SGM4029 in the design, select a proper output capacitor that does not create gain peaking, thereby increasing total system noise. At the same time, the capacitor must be selected to provide required filtering performance for the system. In addition, input bypass capacitor and noise reduction capacitors must be added for optimum performances. During the design of the data acquisition system, equal consideration must be given to the buffering analog input signal as well as the reference voltage. Having a properly designed input buffer with an associated RC filter is a necessary requirement for good performance of the data acquisition system.

Detailed Design Procedure

The SGM8261 is used to drive the 24-bit Analog to Digital Converter (SGM58601). The RC filter at the output of the SGM8261 is used to reduce the charge kick-back created by the opening and closing of the sampling switch inside the ADC. Design the RC filter such that the voltage at the sampling capacitor settles to 24-bit accuracy within the acquisition time of the ADC. The bandwidth of the driving amplifier must at least be 4 times the bandwidth of the RC filter.

The SGM4029-2.5 is used to drive the REF pin of the SGM58601. Proper selection of Voltage Reference output capacitor is very important for this design. Very Low equivalent series resistance (ESR) creates gain-peaking which degrades SNR of the total system. If the ESR of the capacitor is not enough, then an additional resistor must be added in series with the output capacitor. A capacitance of 1μF can be connected to the NR pin to reduce bandgap noise of the SGM4029.

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM4029 features extremely low dropout voltage. With the exception of the SGM4029-2.048, which has a minimum supply requirement of 2.7V, these references can be operated with a supply of 200mV more than the output voltage in an unloaded condition. It is recommended a supply bypass capacitor ranging from 1μF to 50μF.

Layout

Place the power supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is from 1μF to 10μF. If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

Place a 1μF noise filtering capacitor between the NR pin and ground.

The output must be decoupled with a 1μF to 50μF capacitor. A resistor in series with the output capacitor is optional. For better noise performance, the recommended ESR on the output capacitor is from 1Ω to 1.5Ω.

A high frequency, 1μF capacitor can be added in parallel between the VOUT pin and GND to filter noise and help with switching loads as data converters.

Power Dissipation

The SGM4029 is specified to deliver current loads of ±10mA over the specified input voltage range. The temperature of the device increases according to following equation:

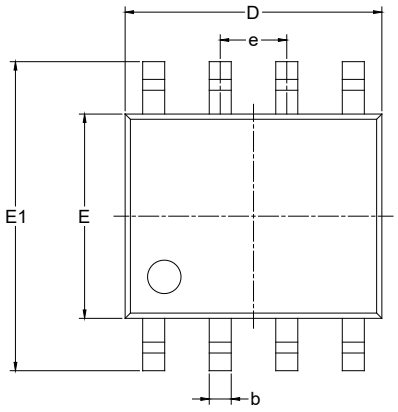
$$T_J = T_A + P_D \times \theta_{JA}$$

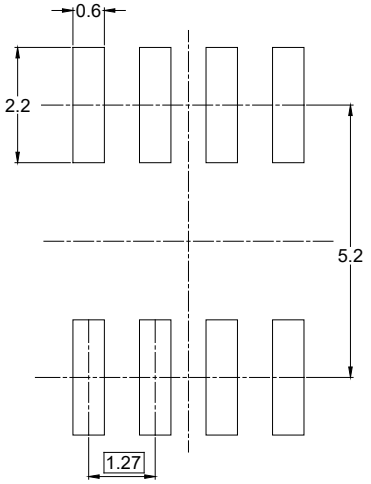
where:
T_J = Junction temperature (℃)
T_A = Ambient temperature (℃)
P_D = Power dissipated (W)
θ_{JA} = Junction-to-ambient thermal resistance (℃/W)

The SGM4029 junction temperature must not exceed the absolute maximum rating of +150℃.

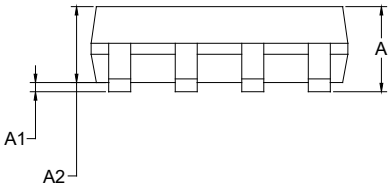
PACKAGE OUTLINE DIMENSIONS

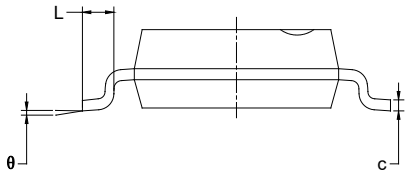
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

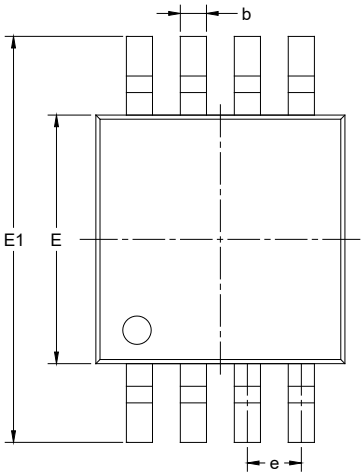


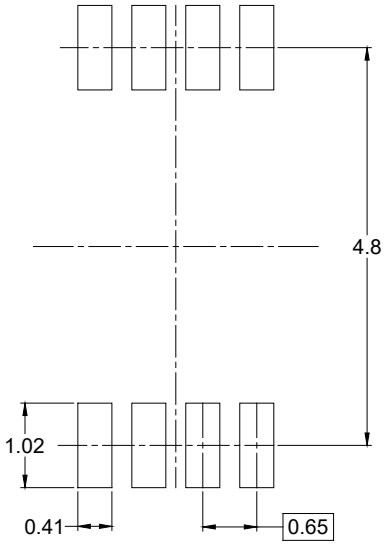


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

MSOP-8





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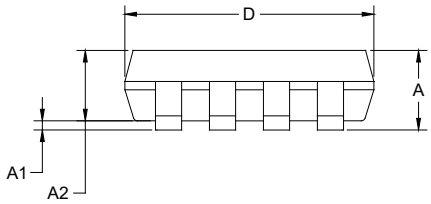

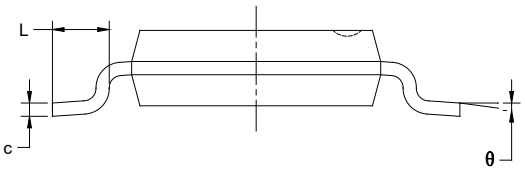

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°