OPAx140 高精度、低噪声、轨至轨输出、11MHz JFET 运算放大器

1 特性

- 极低的温漂：1μV/°C（最大值）
- 极低的偏移：120μV
- 低输入偏置电流：10pA（最大值）
- 极低的 1/f 噪声：250nV$_{PP}$，0.1Hz 至 10Hz
- 低噪声：5.1nV/√Hz
- 压摆率：20V/μs
- 低电源电流：2mA（最大值）
- 输入电压范围包括 V– 电源
- 单电源运作：4.5V 至 36V
- 双电源运作：±2.25V 至 ±18V
- 无相位反转
- 行业标准 SOIC 封装
- VSSOP、TSSOP 和 SOT-23 封装

2 应用

- 电池供电仪器
- 工业控制
- 医疗仪表
- 光电二极管放大器
- 有源滤波器
- 数据采集系统
- 自动测试系统

3 说明

OPA140、OPA2140 和 OPA4140 运算放大器系列器件是一系列具有良好漂移性能和低输入 偏置 电流的低功耗 JFET 输入放大器。凭借其包括 V- 在内的轨至轨输出摆幅和输入范围，设计人员可以利用 JFET 放大器的低噪声特性，同时还可以连接到现代单电源精密模数转换器 (ADC) 和数模转换器 (DAC)。

OPA140 可实现 11MHz 单位增益带宽和 20V/μs 压摆率，同时仅消耗 1.8mA（典型值）的静态电流。它由 4.5V 至 36V 单电源或 ±2.25V 至 ±18V 双电源供电。

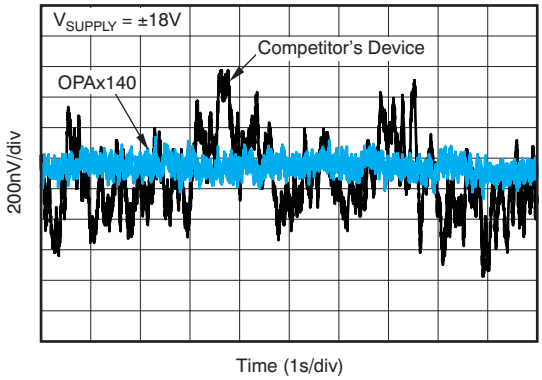
所有器件版本的额定工作温度范围均为 –40°C 至 +125°C，可用于最具有挑战性的环境中。OPA140（单通道）采用 5 引脚 SOT-23、8 引脚 VSSOP 和 8 引脚 SOIC 封装；OPA2140（双通道）采用 8 引脚 VSSOP 和 8 引脚 SOIC 封装；OPA4140（四通道）采用 14 引脚 SOIC 和 14 引脚 TSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA140	SOIC (8)	4.90mm × 3.90mm
	SOT23 (5)	2.90mm × 1.60mm
	VSSOP (8)	3.00mm × 3.00mm
OPA2140	SOIC (8)	4.90mm × 3.90mm
	VSSOP (8)	3.00mm × 3.00mm
OPA4140	SOIC (14)	8.65mm × 3.90mm
	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅产品数据表末尾的封装选项附录。

0.1Hz 至 10Hz 噪声



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (August 2016) to Revision D **Page**

- Changed Figure 12 x-axis title From: Frequency (Hz) To: Output Amplitude (V_{RMS}) ... 10

Changes from Revision B (November 2015) to Revision C **Page**

- Changed units for E_n Input voltage noise From: µV To: nV in *Electrical Characteristics: V_S = 4.5 V to 36 V; ±2.25 V to ±18 V* ... 7

Changes from Revision A (August 2010) to Revision B **Page**

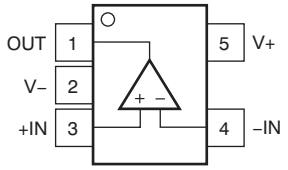
- 已添加 添加了 *ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- Changed title of Table 1 From: *Characteristic Performance Measurements* To: *Table of Graphs* ... 8
- Changed section 7.37 title From: *Power Dissipation and Thermal Protection* To: *Thermal Protection* ... 18

Changes from Original (July 2010) to Revision A **Page**

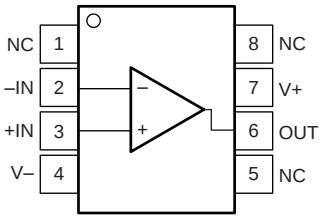
- 已更改 将器件和数据表状态更改成了生产数据状态 ... 1
- Added SOIC (8) (MSOP) packages ... 3

5 Pin Configuration and Functions

DBV Package: OPA140
5-Pin SOT-23
Top View



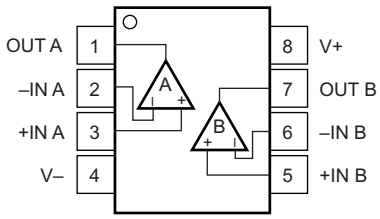
D and DGK Packages: OPA140
8-Pin SOIC and VSSOP
Top View



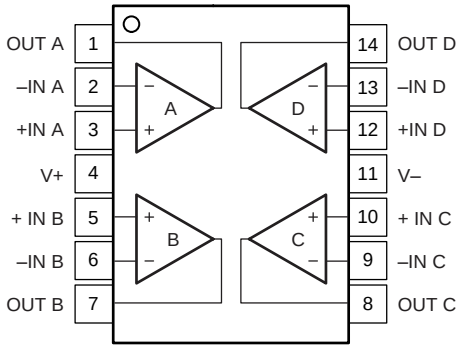
Pin Functions: OPA140

PIN			I/O	DESCRIPTION
NAME	OPA140			
	D (SOIC), DGK (VSSOP)	DBV (SOT)		
+IN	3	3	I	Noninverting input
–IN	2	4	I	Inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V+	7	5	—	Positive (highest) power supply
V–	4	2	—	Negative (lowest) power supply

D and DGK Packages: OPA2140
8-Pin SOIC and VSSOP
Top View



D and PW Packages: OPA4140
14-Pin SOIC and TSSOP
Top View



Pin Functions: OPA2140 and OPA4140

PIN			I/O	DESCRIPTION
NAME	OPA2140	OPA4140		
	D (SOIC), DGK (VSSOP)	D (SOIC), PW (TSSOP)		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input, channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	—	Positive (highest) power supply
V–	4	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)			40	V
Signal input pins	Voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Current(2)	–10	10	mA
Output short circuit(3)		Continuous		
Temperature	Operating	–55	150	°C
	Junction		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to V_S/2 (ground in symmetrical dual-supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	±2.25		±18	V
Specified temperature	–40		125	°C

6.4 Thermal Information: OPA140

THERMAL METRIC(1)		OPA140			UNIT
		D (SOIC)	DBV (SOT)	DGK (VSSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	210	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	200	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	110	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9	40	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	105	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2140

THERMAL METRIC(1)		OPA2140		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4140

THERMAL METRIC(1)		OPA4140		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	135	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	66	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics: V_S = 4.5 V to 36 V; ±2.25 V to ±18 V

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				30	120	µV
		V_S = ±18 V, T_A = –40°C to 125°C				220	
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 125°C				±4	µV/V
dV_{OS}/dT	Input offset voltage drift	V_S = ±18 V, T_A = –40°C to 125°C			±0.35	1	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V, T_A = –40°C to 125°C			±0.1	±0.5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±10	pA
		T_A = –40°C to 125°C				±3	nA
I_{OS}	Input offset current				±0.5	±10	pA
		T_A = –40°C to 125°C				±1	nA
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			250		nV_{PP}
		f = 0.1 Hz to 10 Hz			42		nV_{RMS}
e_n	Input voltage noise density	f = 10 Hz			8		$nV/\sqrt{Hz}$
		f = 100 Hz			5.8		
		f = 1 kHz			5.1		
i_n	Input current noise density	f = 1 kHz			0.8		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V		126	140		dB
			T_A = –40°C to 125°C	120			
INPUT IMPEDANCE							
Z_{ID}	Differential				10^{13} || 10		Ω || pF
Z_{IC}	Common-mode	V_{CM} = (V–) – 0.1 V to (V+) – 3.5 V			10^{13} || 7		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 10 kΩ		120	126		dB
		V_O = (V–) + 0.35 V to (V+) – 0.35 V, R_L = 2 kΩ		114	126		
			T_A = –40°C to 125°C	108			
FREQUENCY RESPONSE							
BW	Gain bandwidth product				11		MHz
SR	Slew rate				20		V/µs
t_s	Settling time	12-bit			880		ns
		16-bit			1.6		µs
t_{OR}	Overload recovery time				600		ns
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_O = 3.5 V_{RMS}			0.00005%		
OUTPUT							
V_O	Voltage output	R_{LOAD} = 10 kΩ, A_{OL} ≥ 108 dB		(V–) + 0.2		(V+) – 0.2	V
		R_{LOAD} = 2 kΩ, A_{OL} ≥ 108 dB		(V–) + 0.35		(V+) – 0.35	
I_{SC}	Short-circuit current	Source			36		mA
		Sink			–30		
C_{LOAD}	Capacitive load drive			See Figure 19 and Figure 20			
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A (See Figure 18)			16		Ω

Electrical Characteristics: V_S = 4.5 V to 36 V; ±2.25 V to ±18 V (continued)

at T_A = 25°C, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Power-supply voltage		4.5 (±2.25)		9 (±18)	V
I_Q	Quiescent current per amplifier	I_O = 0 A		1.8	2	mA
		T_A = –40°C to 125°C			2.7	
CHANNEL SEPARATION						
	Channel separation	At dc		0.02		µV/V
		At 100 kHz		10		

6.8 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	Figure 3
I_B vs Common-Mode Voltage	Figure 5
Input Offset Voltage vs Temperature	Figure 4
Output Voltage Swing vs Output Current	Figure 6
CMRR and PSRR vs Frequency (RTI)	Figure 7
Common-Mode Rejection Ratio vs Temperature	Figure 8
0.1-Hz to 10-Hz Noise	Figure 9
Input Voltage Noise Density vs Frequency	Figure 10
THD+N Ratio vs Frequency (80-kHz AP Bandwidth)	Figure 11
THD+N Ratio vs Output Amplitude	Figure 12
Quiescent Current vs Temperature	Figure 13
Quiescent Current vs Supply Voltage	Figure 14
Gain and Phase vs Frequency	Figure 15
Closed-Loop Gain vs Frequency	Figure 16
Open-Loop Gain vs Temperature	Figure 17
Open-Loop Output Impedance vs Frequency	Figure 18
Small-Signal Overshoot vs Capacitive Load (G = 1)	Figure 19
Small-Signal Overshoot vs Capacitive Load (G = –1)	Figure 20
No Phase Reversal	Figure 21
Positive Overload Recovery	Figure 23
Negative Overload Recovery	Figure 24
Large-Signal Positive and Negative Settling Time	Figure 25, Figure 26
Small-Signal Step Response (G = 1)	Figure 27
Small-Signal Step Response (G = –1)	Figure 28
Large-Signal Step Response (G = 1)	Figure 29
Large-Signal Step Response (G = –1)	Figure 30
Short-Circuit Current vs Temperature	Figure 31
Maximum Output Voltage vs Frequency	Figure 22
Channel Separation vs Frequency	Figure 32

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

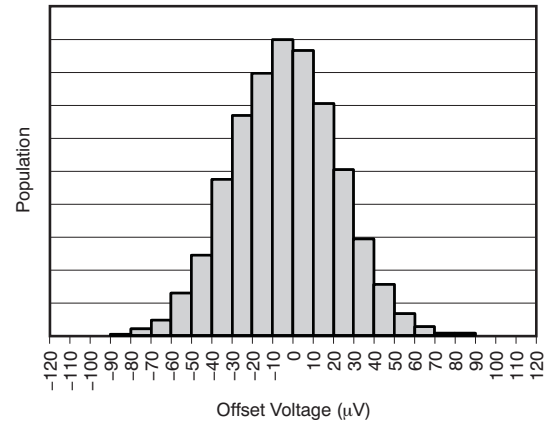


Figure 1. Offset Voltage Production Distribution

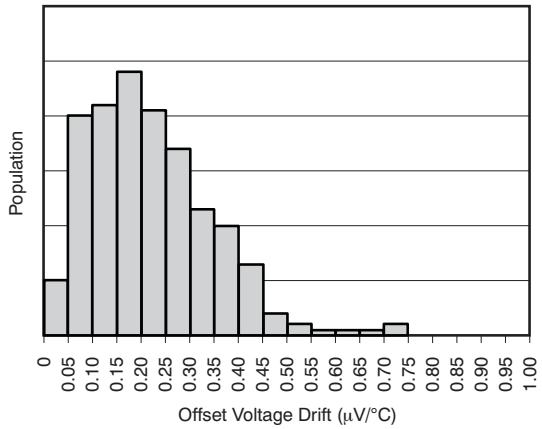


Figure 2. Offset Voltage Drift Distribution

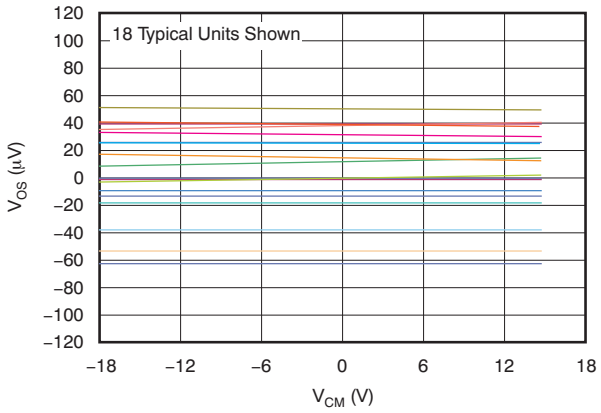


Figure 3. Offset Voltage vs Common-Mode Voltage

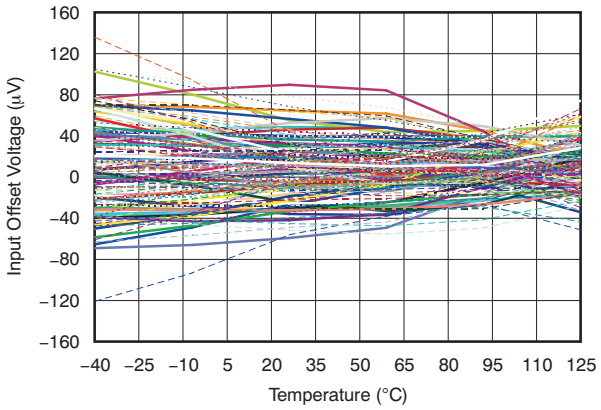


Figure 4. Input Offset Voltage vs Temperature (144 Amplifiers)

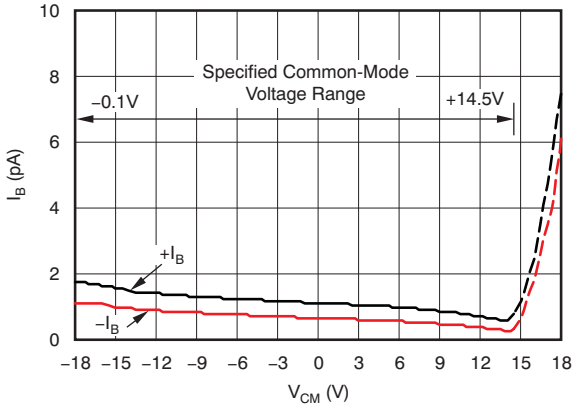


Figure 5. I_B vs Common-Mode Voltage

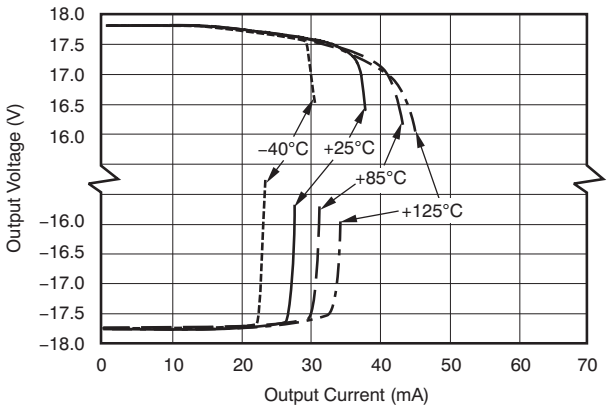


Figure 6. Output Voltage Swing vs Output Current (Maximum Supply)

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

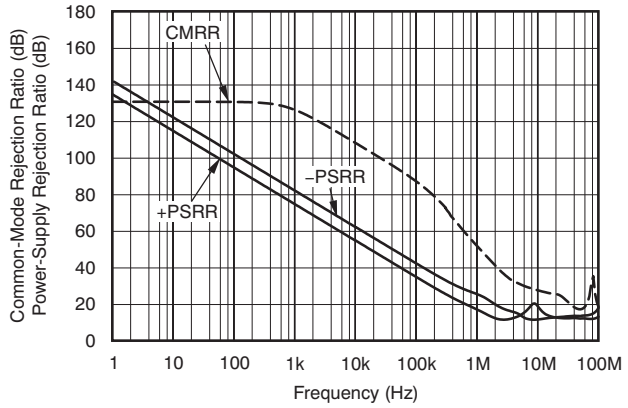


Figure 7. CMRR and PSRR vs Frequency (Referred to Input)

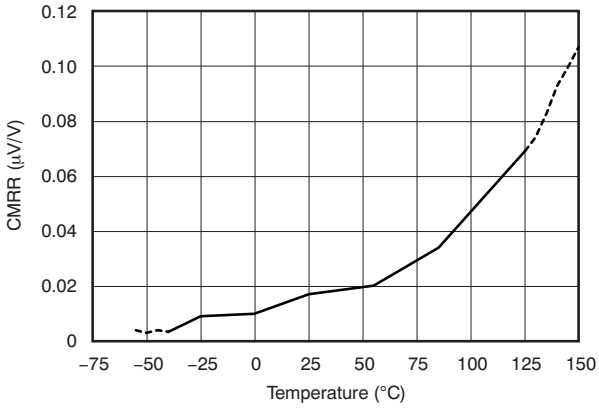


Figure 8. Common-Mode Rejection Ratio vs Temperature

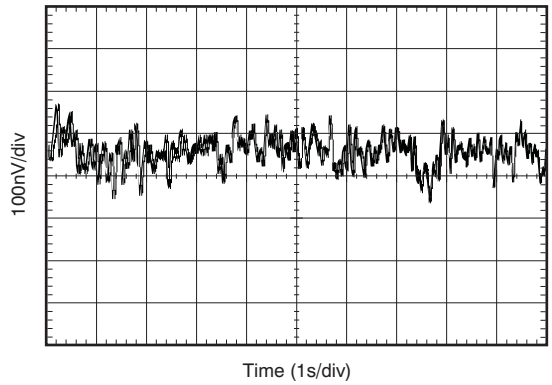


Figure 9. 0.1-Hz to 10-Hz Noise

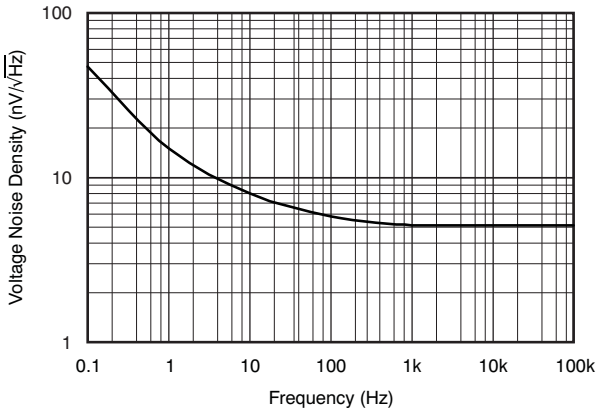


Figure 10. Input Voltage Noise Density vs Frequency

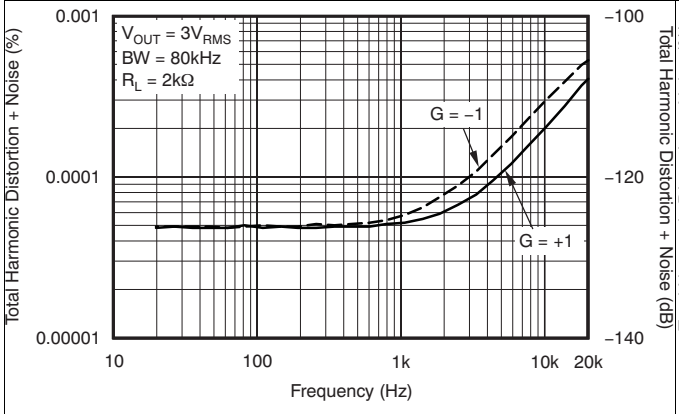


Figure 11. THD+N Ratio vs Frequency

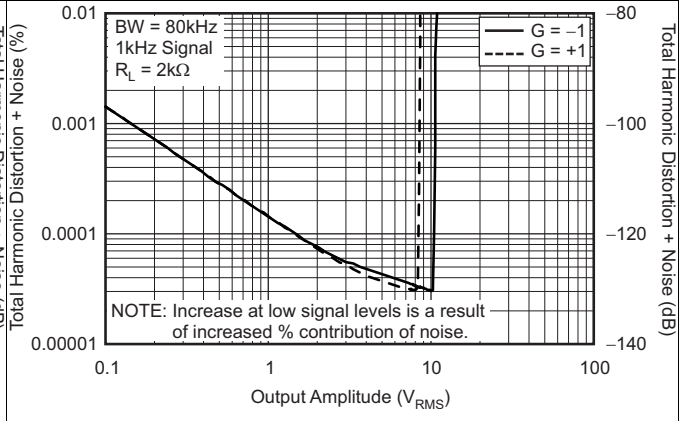


Figure 12. THD+N Ratio vs Output Amplitude

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

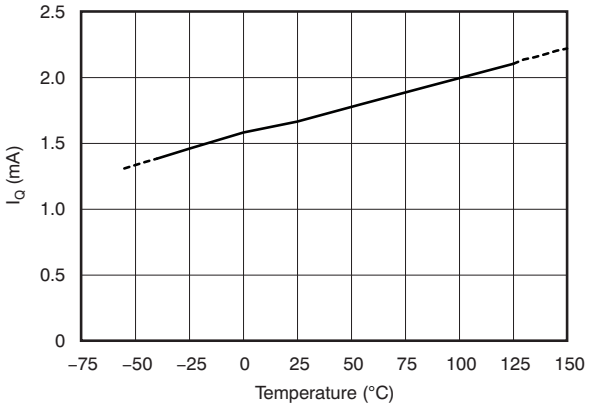


Figure 13. Quiescent Current vs Temperature

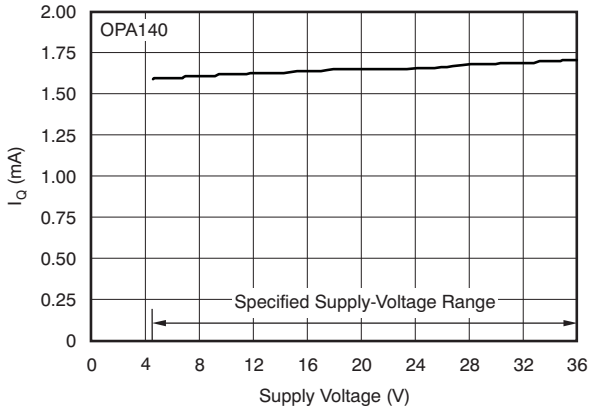


Figure 14. Quiescent Current vs Supply Voltage

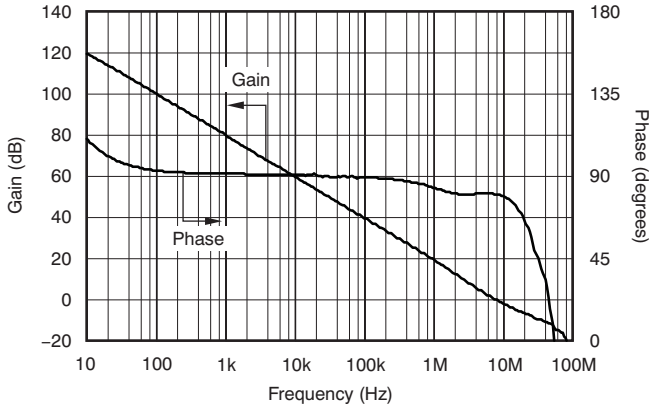


Figure 15. Gain and Phase vs Frequency

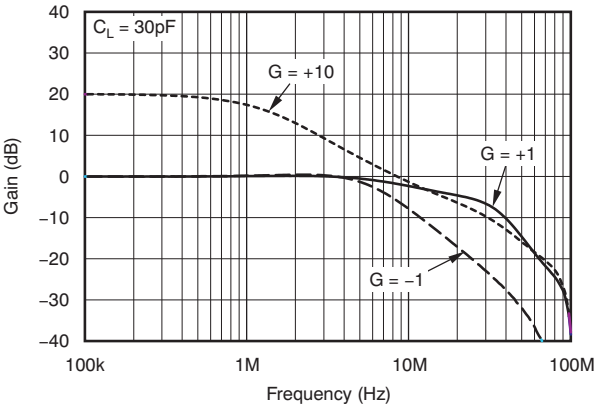


Figure 16. Closed-Loop Gain vs Frequency

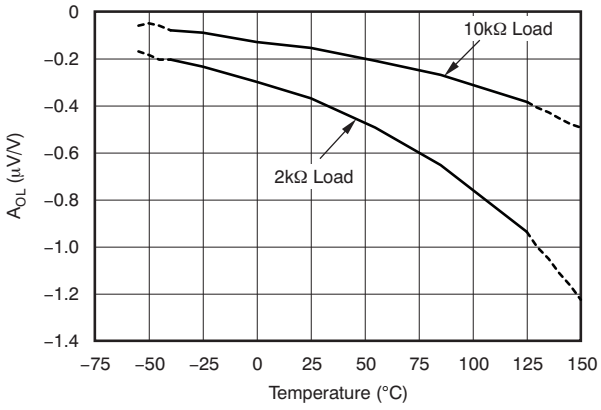


Figure 17. Open-Loop Gain vs Temperature

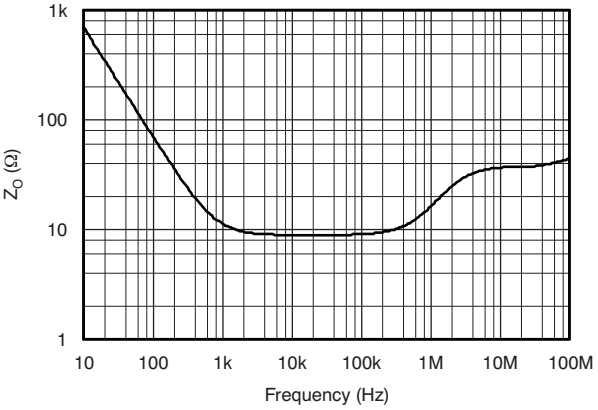


Figure 18. Open-Loop Output Impedance vs Frequency

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

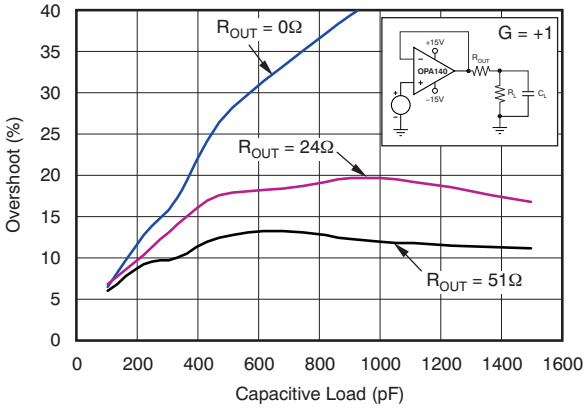


Figure 19. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

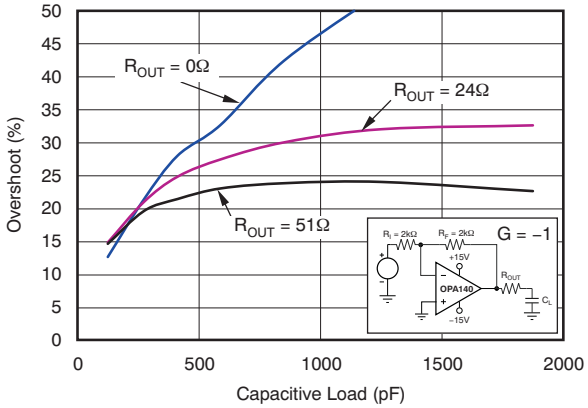


Figure 20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

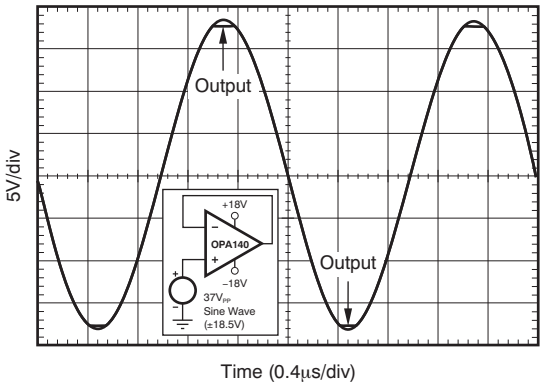


Figure 21. No Phase Reversal

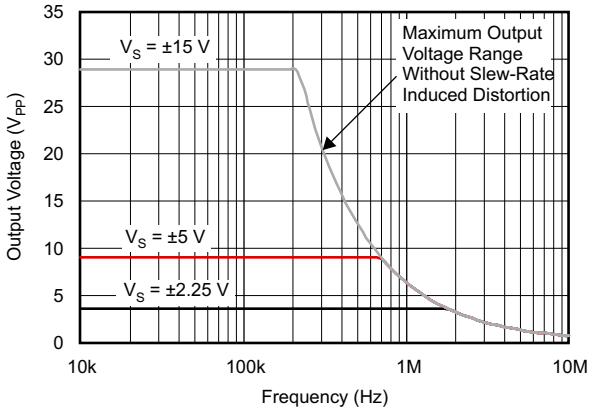


Figure 22. Maximum Output Voltage vs Frequency

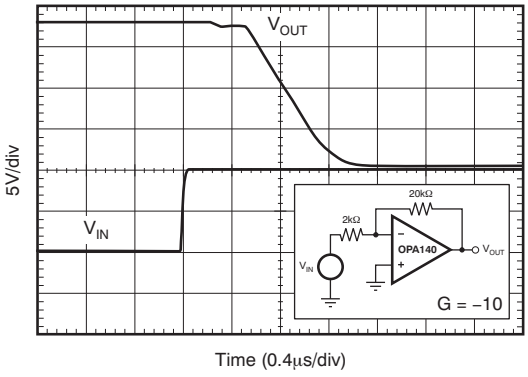


Figure 23. Positive Overload Recovery

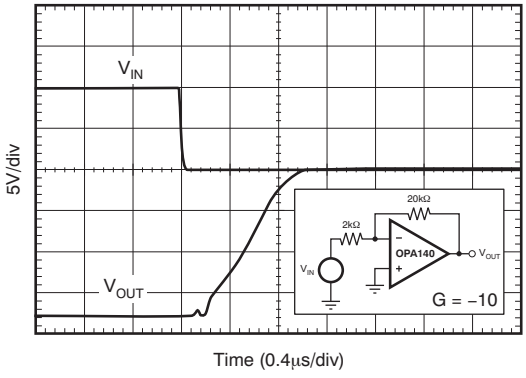


Figure 24. Negative Overload Recovery

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

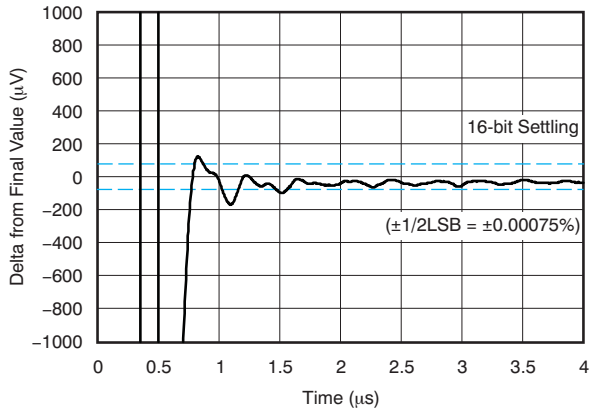


Figure 25. Large-Signal Positive Settling Time (10-V Step)

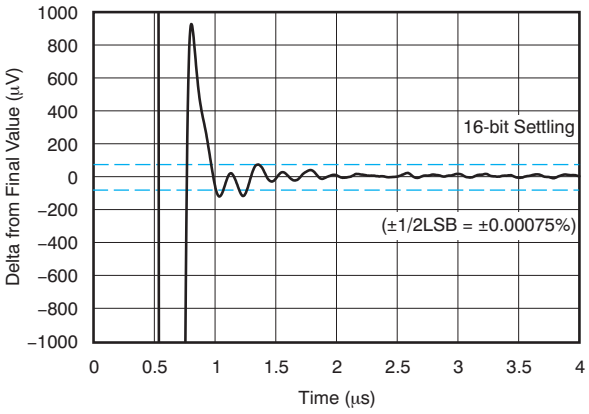


Figure 26. Large-Signal Negative Settling Time (10-V Step)

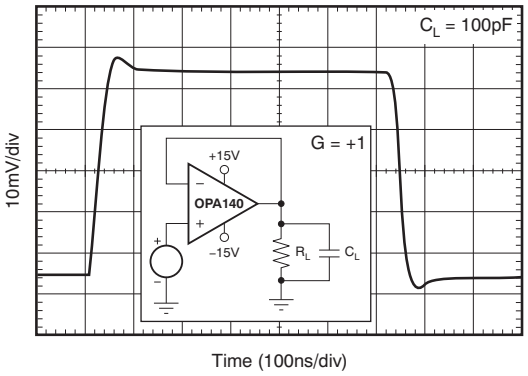


Figure 27. Small-Signal Step Response (100 mV)

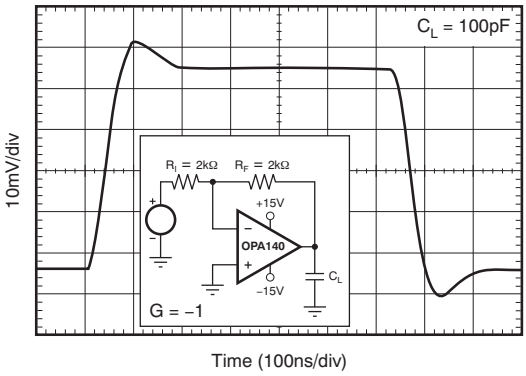


Figure 28. Small-Signal Step Response (100 mV)

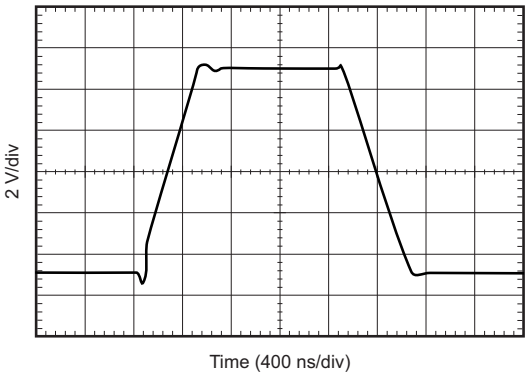


Figure 29. Large-Signal Step Response

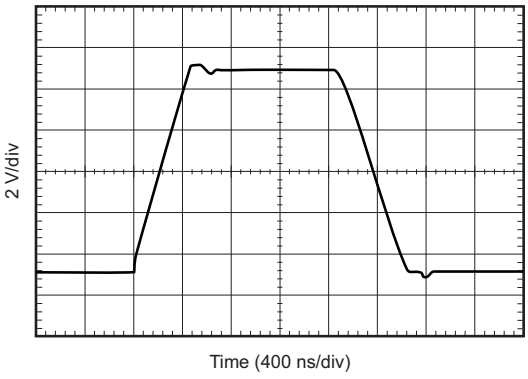


Figure 30. Large-Signal Step Response

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

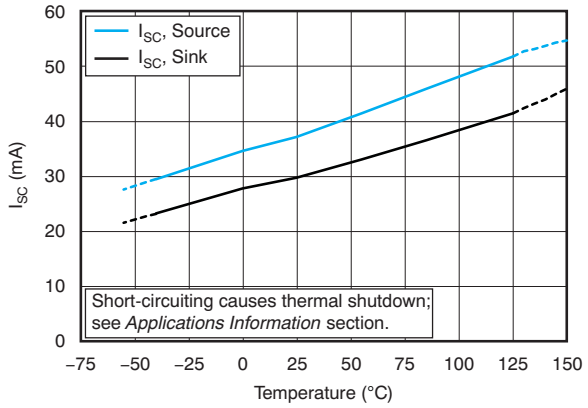


Figure 31. Short Circuit Current vs Temperature

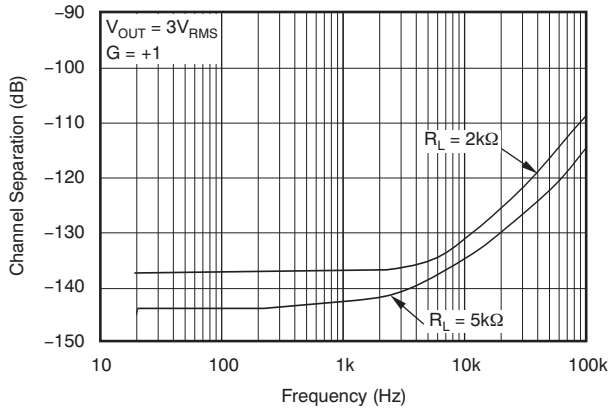


Figure 32. Channel Separation vs Frequency

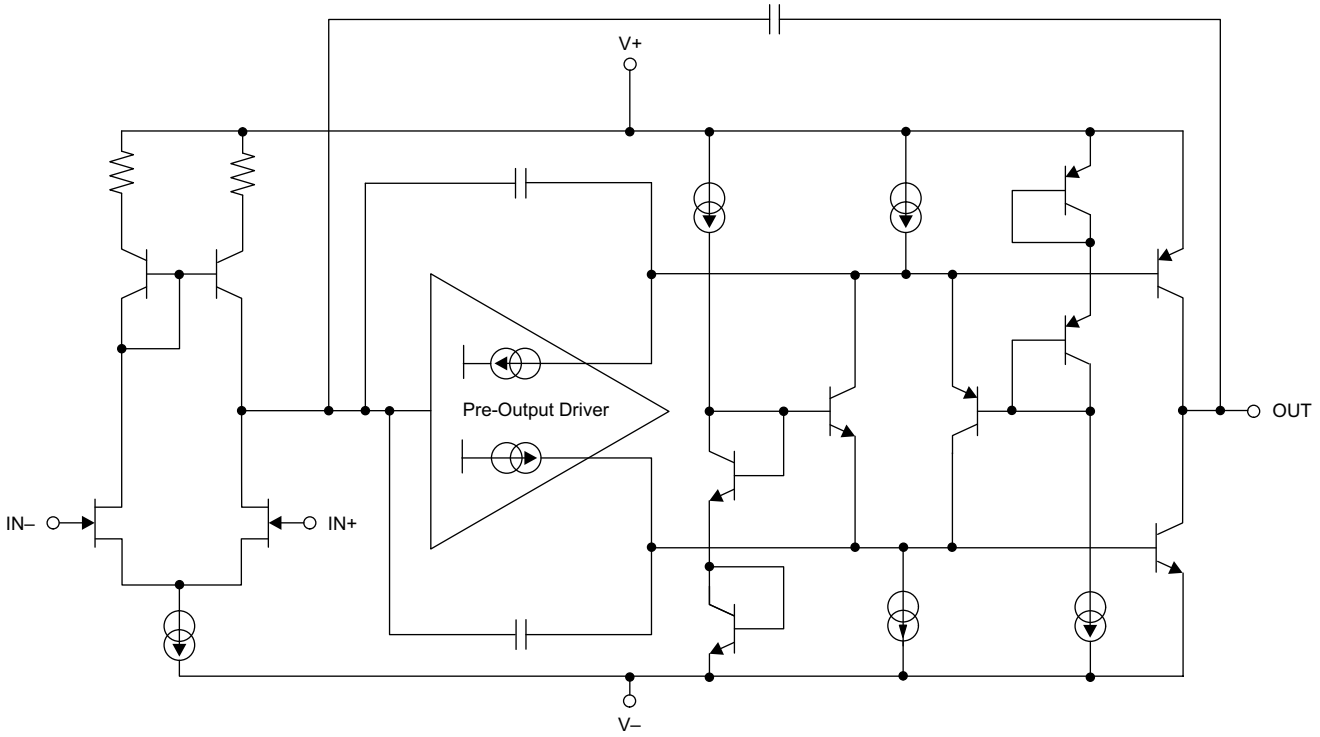
7 Detailed Description

7.1 Overview

The OPAx140 family of operational amplifiers is a series of low-power JFET input amplifiers that feature superior drift performance and low input bias current. The rail-to-rail output swing and input range that includes V– allow designers to use the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The OPAx140 series achieves 11-MHz unity-gain bandwidth and 20-V/μs slew rate, and consumes only 1.8 mA (typical) of quiescent current. These devices operate on a single 4.5-V to 36-V supply or dual ±2.25-V to ±18-V supplies.

The *Functional Block Diagram* section shows the simplified diagram of the OPAx140.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA140, OPA2140, and OPA4140 series of op amps can be used with single or dual supplies from an operating range of V_S = 4.5 V (±2.25 V) and up to V_S = 36 V (±18 V). These devices do not require symmetrical supplies; they only require a minimum supply voltage of 4.5 V (±2.25 V). For V_S less than ±3.5 V, the common-mode input range does not include midsupply. Supply voltages higher than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table. Key parameters are specified over the operating temperature range, T_A = –40°C to 125°C. Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section of this data sheet.

Feature Description (continued)

7.3.2 Capacitive Load and Stability

The dynamic characteristics of the OPAx140 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω, for example) in series with the output.

Figure 19 and Figure 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT}. Also, see the *Feedback Plots Define Op Amp AC Performance Application Bulletin*, available for download from www.ti.com, for details of analysis techniques and application circuits.

7.3.3 Output Current Limit

The output current of the OPAx140 series is limited by internal circuitry to 36 mA/–30 mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short circuit current depends on temperature, as shown in Figure 31.

7.3.4 Noise Performance

Figure 33 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA140 and OPA211 are shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA140, OPA2140, and OPA4140 family has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx140 series is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.

The equation in Figure 33 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see *Basic Noise Calculations*.

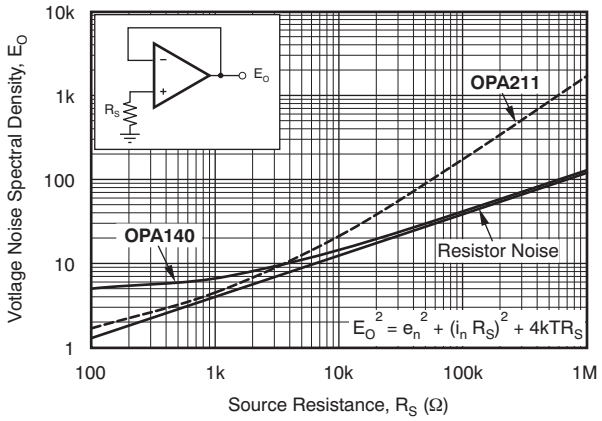


Figure 33. Noise Performance of the OPA140 and OPA211 in Unity-Gain Buffer Configuration

Feature Description (continued)

7.3.5 Basic Noise Calculations

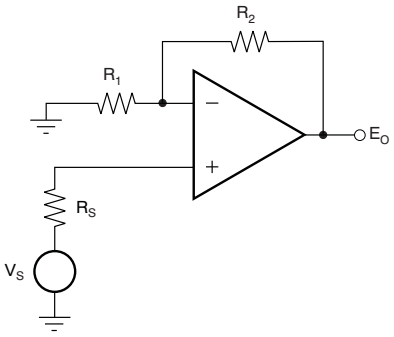
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 33. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 34 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx140 means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

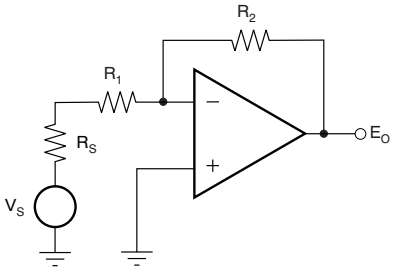
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + \left(\frac{R_2}{R_1}\right)^2 e_1^2 + e_2^2 + \left(1 + \frac{R_2}{R_1}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_1^2 + e_2^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPAx140 series of operational amplifiers at 1 kHz, $e_n = 5.1\ nV/\sqrt{Hz}$.

Figure 34. Noise Calculation in Gain Configurations

7.3.6 Phase-Reversal Protection

The OPA140, OPA2140, and OPA4140 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA140, OPA2140, and OPA4140 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 21).

Feature Description (continued)

7.3.7 Thermal Protection

The OPAx140 series of op amps are capable of driving 2-kΩ loads with power-supply voltages of up to ±18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8 kΩ at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used, as long as the output current does not exceed 13 mA; otherwise, the device short circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA140, OPA2140, and OPA4140 series devices improves heat dissipation compared to conventional materials. Printed-circuit-board (PCB) layout can also help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36 mA leads to an internal power dissipation of over 600 mW at a supply of ±18 V.

In the case of a dual OPA2140 in an 8-pin VSSOP package (thermal resistance θ_{JA} = 180°C/W), such power dissipation would lead the die temperature to be 220°C above ambient temperature, when both channels are shorted. This temperature increase significantly decreases the operating life of the device.

To prevent excessive heating, the OPAx140 series has an internal thermal shutdown circuit that shuts down the device if the die temperature exceeds approximately 180°C. When this thermal shutdown circuit activates, a built-in hysteresis of 15°C makes sure that the die temperature must drop to approximately 165°C before the device switches on again.

Additional consideration should be given to the combination of maximum operating voltage, maximum operating temperature, load, and package type. Figure 35 and Figure 36 show several practical considerations when evaluating the OPA2140 (dual version) and the OPA4140 (quad version).

As an example, the OPA4140 has a maximum total quiescent current of 10.8 mA (2.7 mA/channel) over temperature. The 14-pin TSSOP package has a typical thermal resistance of 135°C/W. This parameter means that because the junction temperature should not exceed 150°C to provide reliable operation, either the supply voltage must be reduced, or the ambient temperature should remain low enough so that the junction temperature does not exceed 150°C. This condition is illustrated in Figure 35 for various package types. Moreover, resistive loading of the output causes additional power dissipation and thus self-heating, which also must be considered when establishing the maximum supply voltage or operating temperature. To this end, Figure 36 shows the maximum supply voltage versus temperature for a worst-case dc load resistance of 2 kΩ.

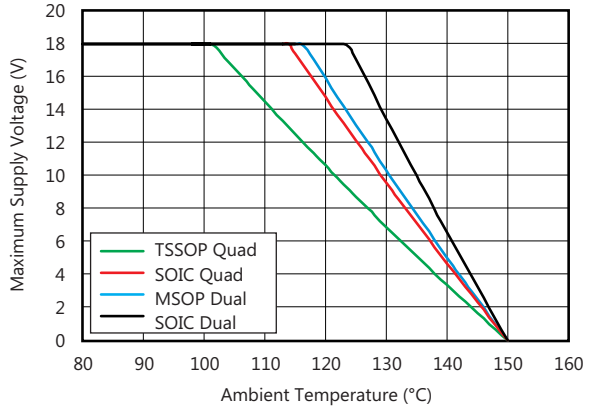


Figure 35. Maximum Supply Voltage vs Temperature (OPA2140 and OPA4140), Quiescent Condition

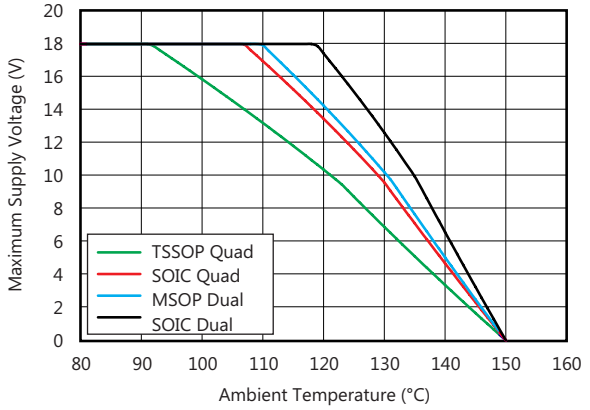


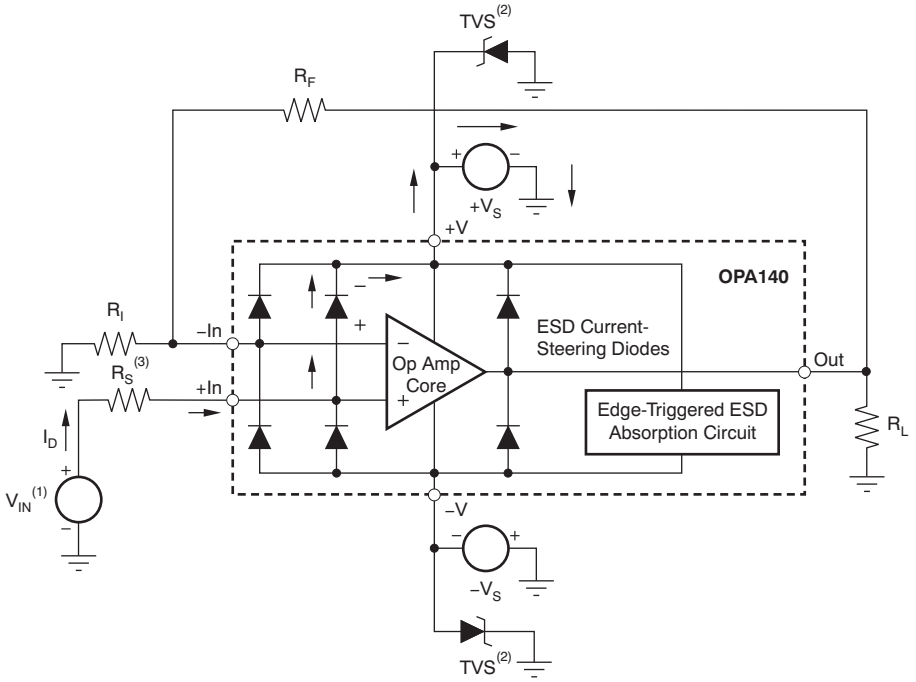
Figure 36. Maximum Supply Voltage vs Temperature (OPA2140 and OPA4140), Maximum DC Load

Feature Description (continued)

7.3.8 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 37 shows an illustration of the ESD circuits contained in the OPAx140 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) V_{IN} = $+V_S$ + 500 mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1 kΩ.

Figure 37. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx140 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

Feature Description (continued)

When the operational amplifier connects into a circuit such as the one Figure 37 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 37 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V.

Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 37. The Zener voltage must be selected such that the diode does not turn on during normal operation.

However, its Zener voltage should be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

Feature Description (continued)

7.3.9 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces. Figure 38

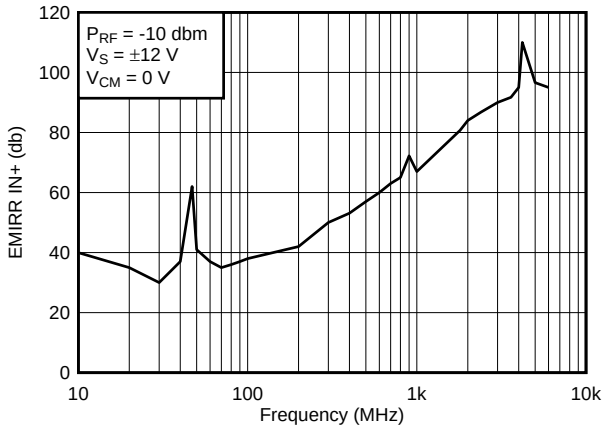


Figure 38. OPA2140 EMIRR

The EMIRR IN+ of the OPA2140 is plotted versus frequency as shown in .If available, any dual and quad op amp device versions have nearly similar EMIRR IN+ performance. The OPA2140 unity-gain bandwidth is 11 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

For more information, see the *EMI Rejection Ratio of Operational Amplifiers Application Report*, available for download from www.ti.com.

Feature Description (continued)

Table 2 lists the EMIRR IN+ values for the OPA2140 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 2. OPA2140 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	53.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	72.2 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	80.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	86.8 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	91.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	96.6 dB

7.3.10 EMIRR +IN Test Configuration

Figure 39 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

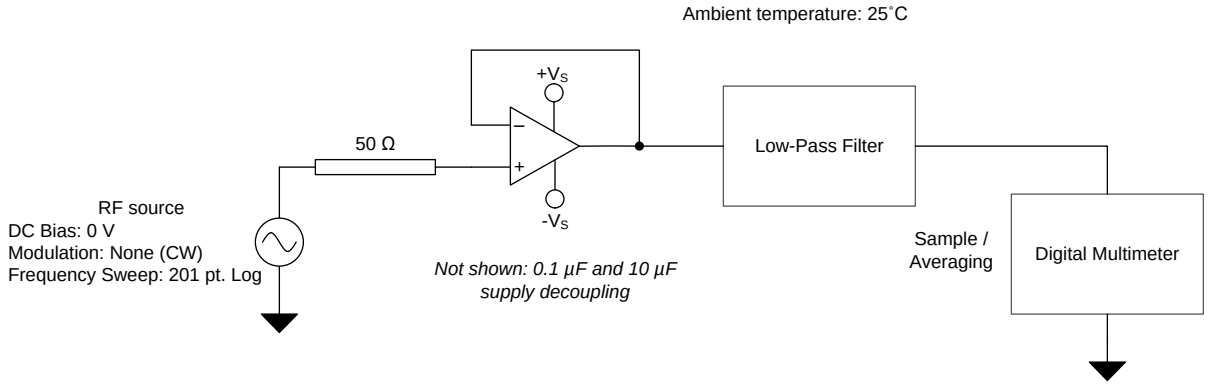


Figure 39. EMIRR +IN Test Configuration

7.4 Device Functional Modes

The OPAx140 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx140 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA140, OPA2140, and OPA4140 are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-μF capacitors are adequate. Designers can easily use the rail-to-rail output swing and input range that includes V– to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision data converters.

8.2 Typical Application

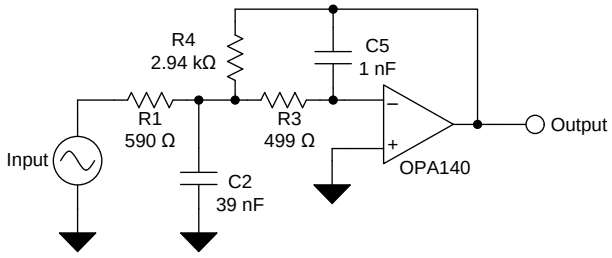


Figure 40. 25-kHz Low-pass Filter

8.2.1 Design Requirements

Lowpass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx140 are an excellent choice to construct high-speed, high-precision active filters. Figure 40 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) \quad \frac{-1/R_1R_3C_2C_5}{s^2+(s/C_2)(1/R_1+1/R_3+1/R_4)+1/R_3R_4C_2C_5} \tag{1}$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the lowpass cutoff frequency are calculated by Equation 2:

$$\text{Gain} \quad \frac{R_4}{R_1}$$

$$f_C \quad \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \tag{2}$$

Typical Application (continued)

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2.3 Application Curve

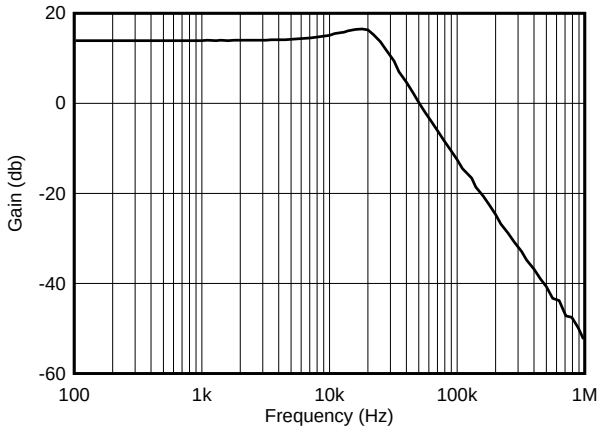


Figure 41. OPAx140 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

9 Power Supply Recommendations

The OPAx140 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 42, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

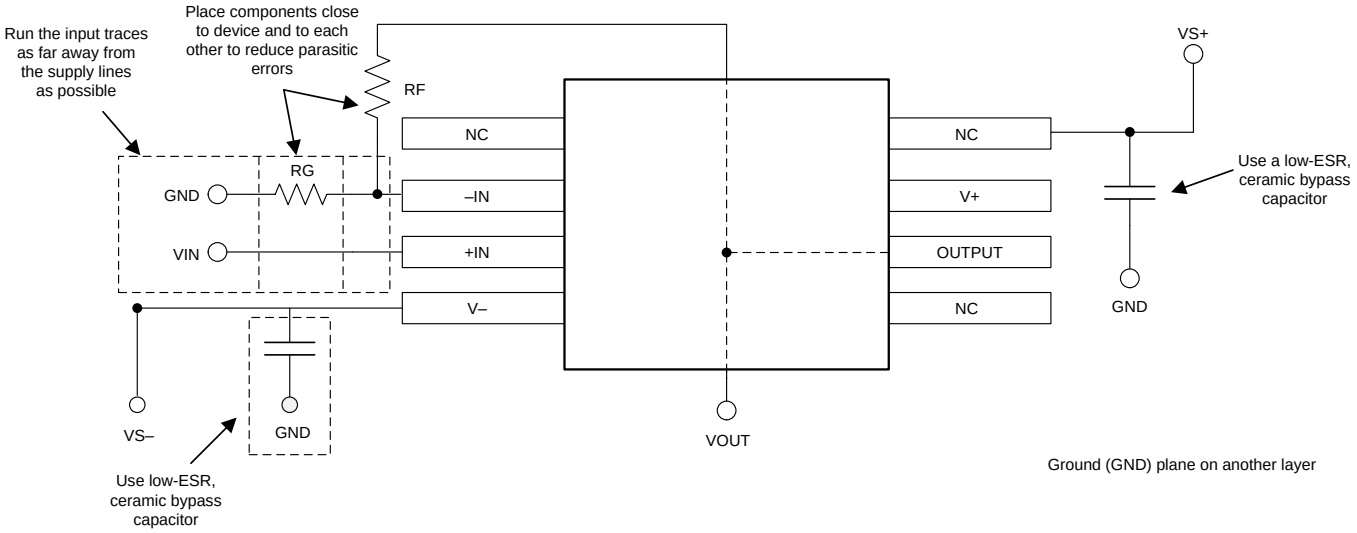


Figure 42. Operational Amplifier Board Layout for Noninverting Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 WEBENCH 滤波器设计器工具

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助 WEBENCH 滤波器设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来构建最佳滤波器设计方案。

11.1.1.3 TI 高精度设计

欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

11.2 文档支持

11.2.1 相关文档

如需相关文档，请参阅：

- 德州仪器 (TI)，*《电路板布局技巧》*
- 德州仪器 (TI)，*《适合所有人的运算放大器设计参考》*
- 德州仪器 (TI)，*《OPA140、OPA2140、OPA4140 EMI 抗干扰性能技术简介》*
- 德州仪器 (TI)，*《用直观方式补偿跨阻放大器的应用报告》*
- 德州仪器 (TI)，*《运算放大器增益稳定性，第 3 部分：交流增益误差分析》*
- 德州仪器 (TI)，*《运算放大器增益稳定性，第 2 部分：直流增益误差分析》*
- 德州仪器 (TI)，*《在全差分有源滤波器中使用无限增益、MFB 滤波器拓扑》*
- 德州仪器 (TI)，*《运算放大器性能分析应用简报》*
- 德州仪器 (TI)，*《运算放大器的单电源运行应用简报》*
- 德州仪器 (TI)，*《在放大器中进行调优应用简报》*
- 德州仪器 (TI)，*《无铅组件涂层的储存寿命评估应用报告》*
- 德州仪器 (TI)，*《反馈曲线图定义运算放大器交流性能应用简报》*
- 德州仪器 (TI)，*《运算放大器的 EMI 抑制比应用报告》*

11.3 相关链接

表 3 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
OPA140	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2140	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA4140	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
WEBENCH is a registered trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OPTION ADDENDUM

7-Oct-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA140AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140	Samples
OPA140AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140	Samples
OPA140AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O140	Samples
OPA140AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(140, O140)	Samples
OPA140AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	140	Samples
OPA140AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA140	Samples
OPA2140AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A	Samples
OPA2140AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2140	Samples
OPA2140AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2140	Samples
OPA2140AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2140A	Samples
OPA4140AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A	Samples
OPA4140AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4140A	Samples
OPA4140AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A	Samples
OPA4140AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4140A	Samples
POPA2140AIDRGR	ACTIVE	SON	DRG	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

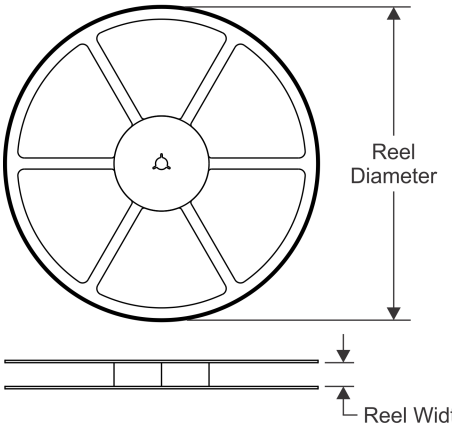
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

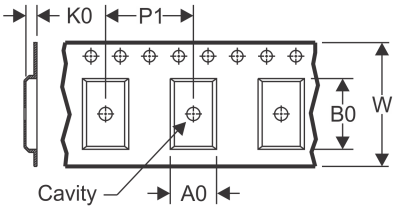
10-Mar-2021

TAPE AND REEL INFORMATION

REEL DIMENSIONS

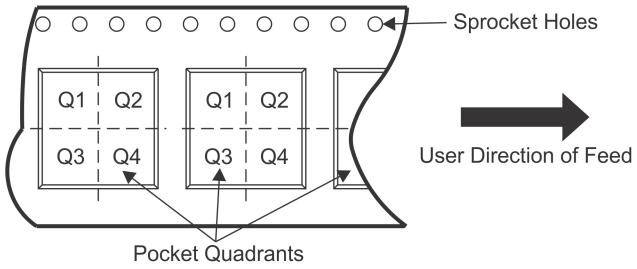


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



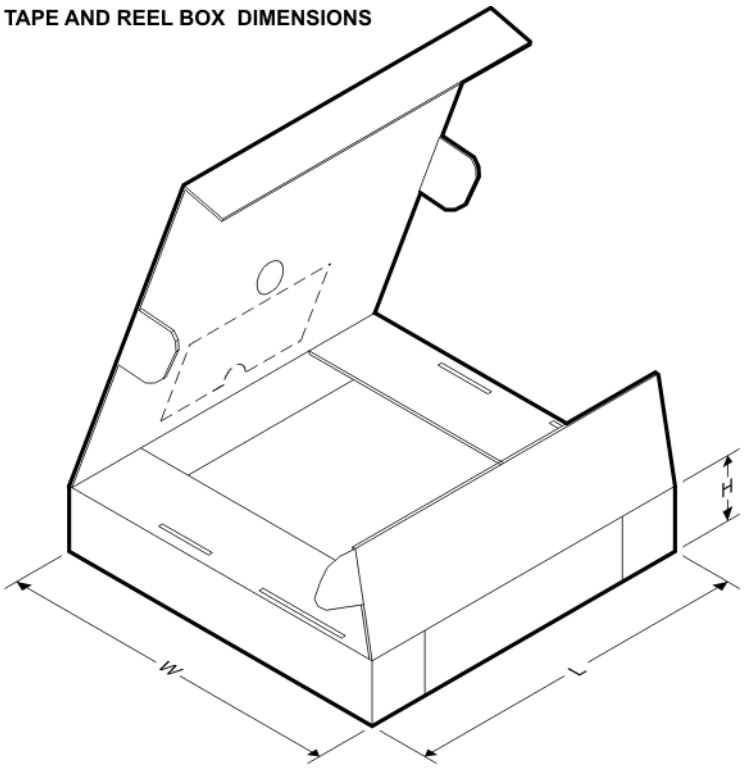
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA140AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA140AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA140AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2140AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2140AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4140AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4140AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

10-Mar-2021

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

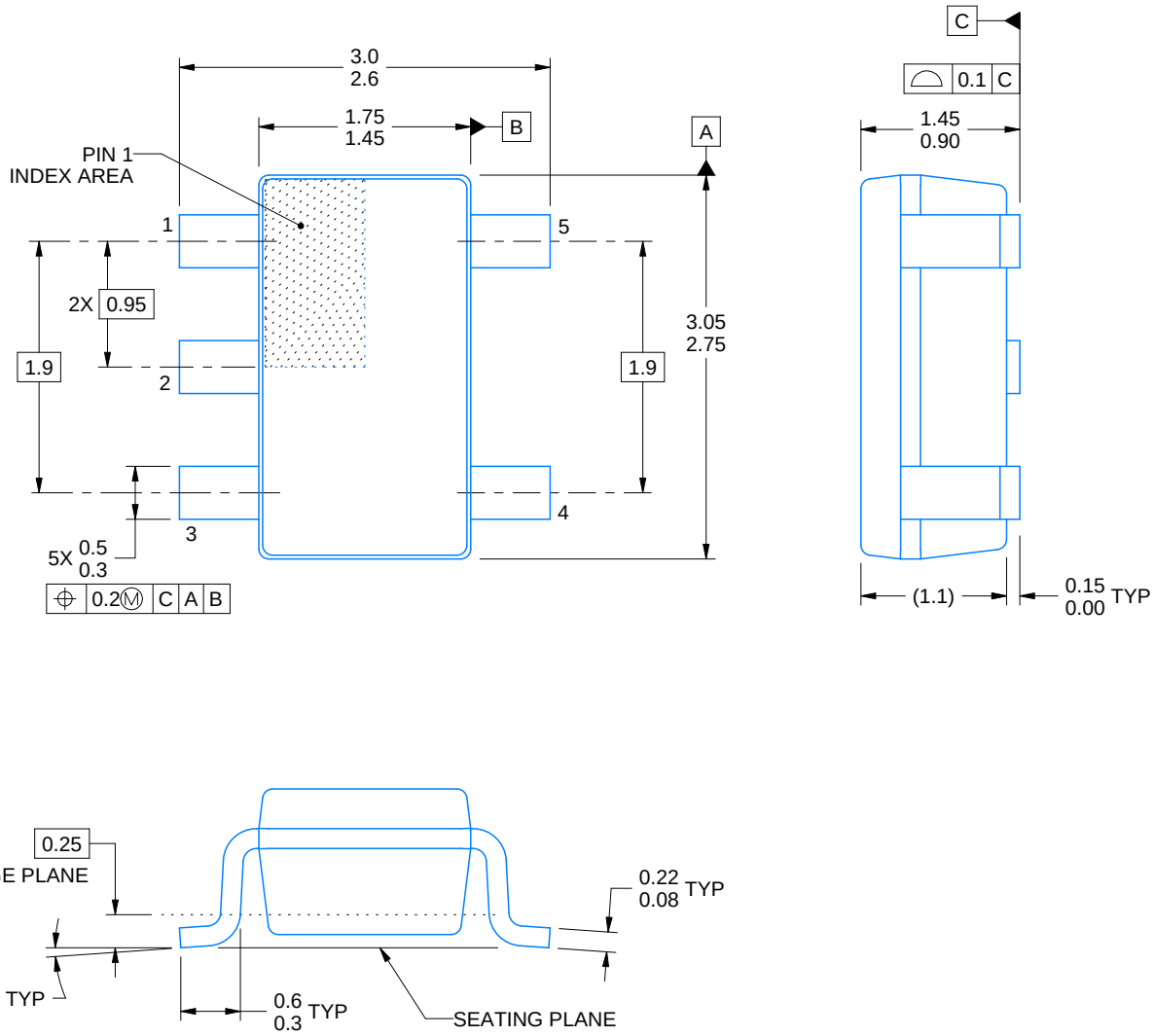
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA140AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA140AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA140AIDR	SOIC	D	8	2500	853.0	449.0	35.0
OPA2140AIDGKR	VSSOP	DGK	8	2500	853.0	449.0	35.0
OPA2140AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2140AIDR	SOIC	D	8	2500	853.0	449.0	35.0
OPA4140AIDR	SOIC	D	14	2500	853.0	449.0	35.0
OPA4140AIPWR	TSSOP	PW	14	2000	853.0	449.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

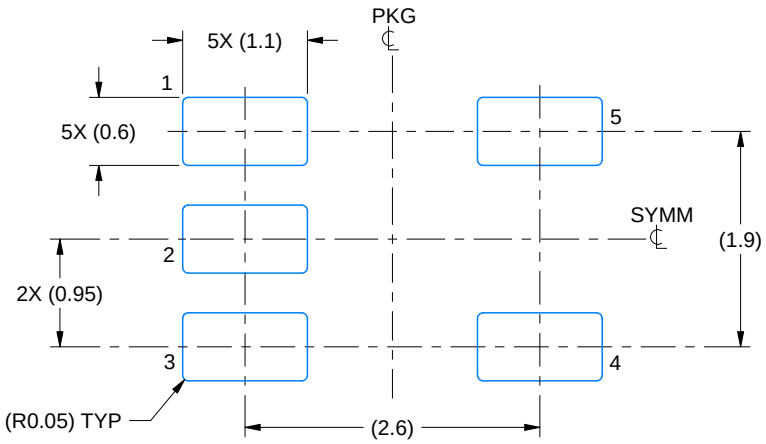
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

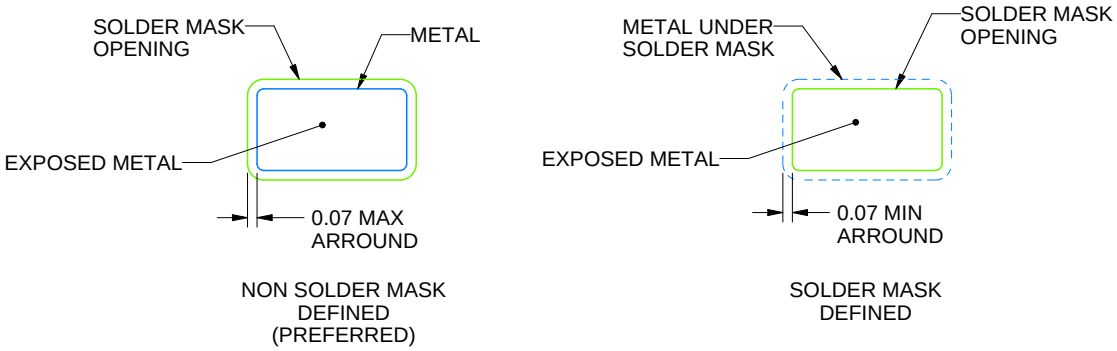
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

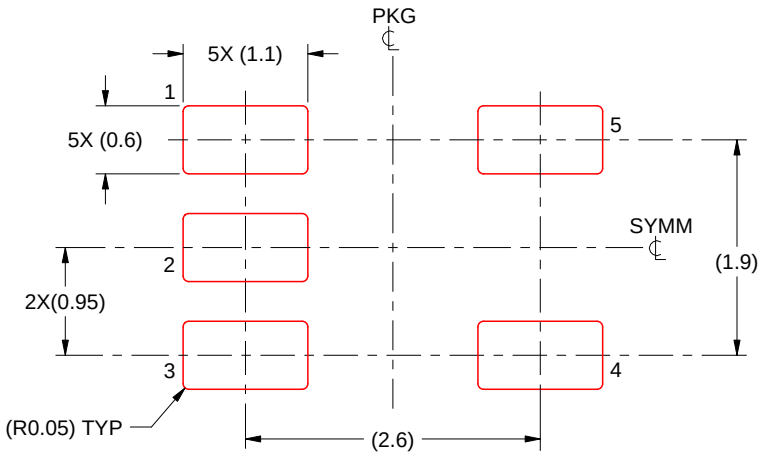
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



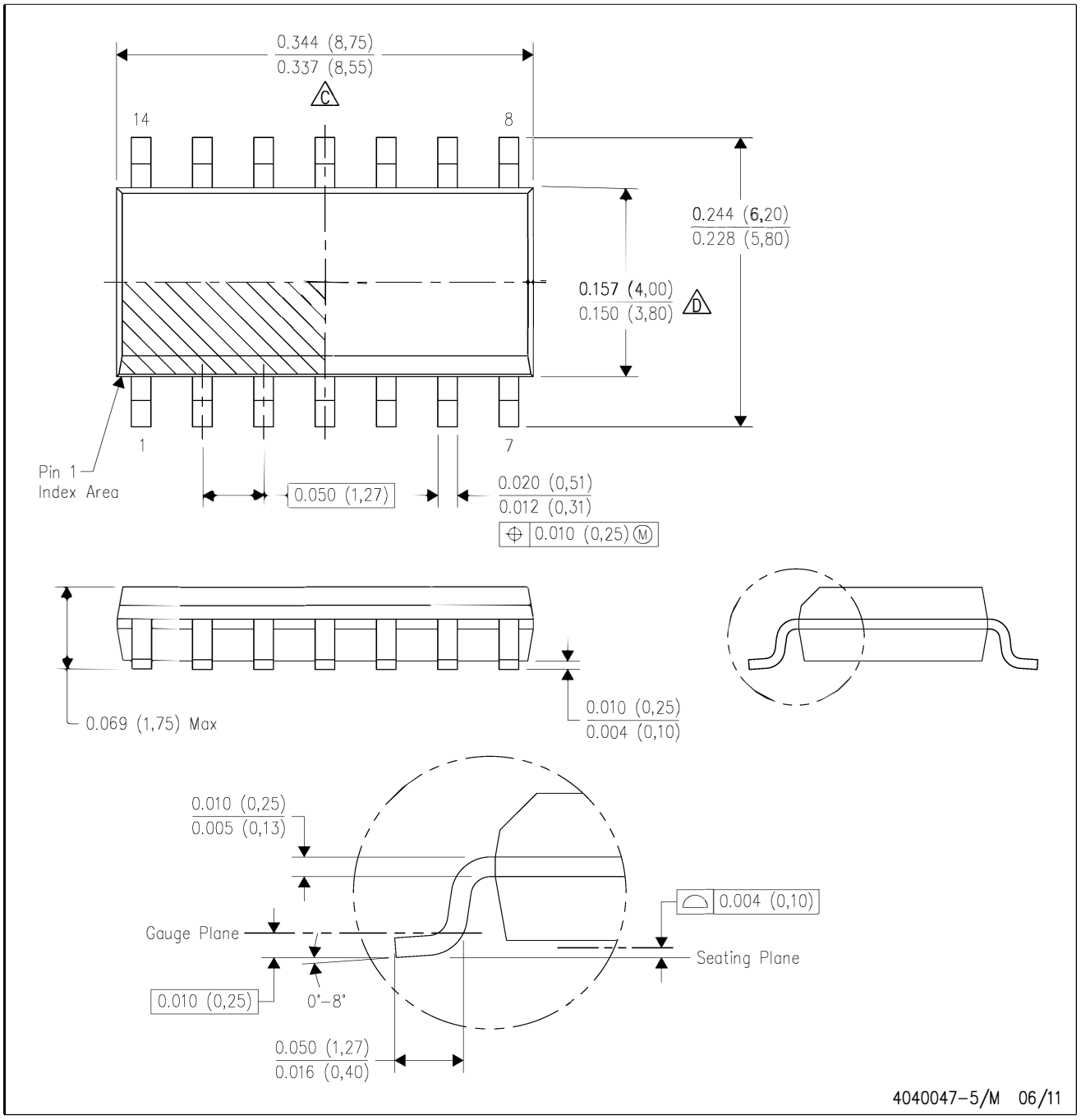
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

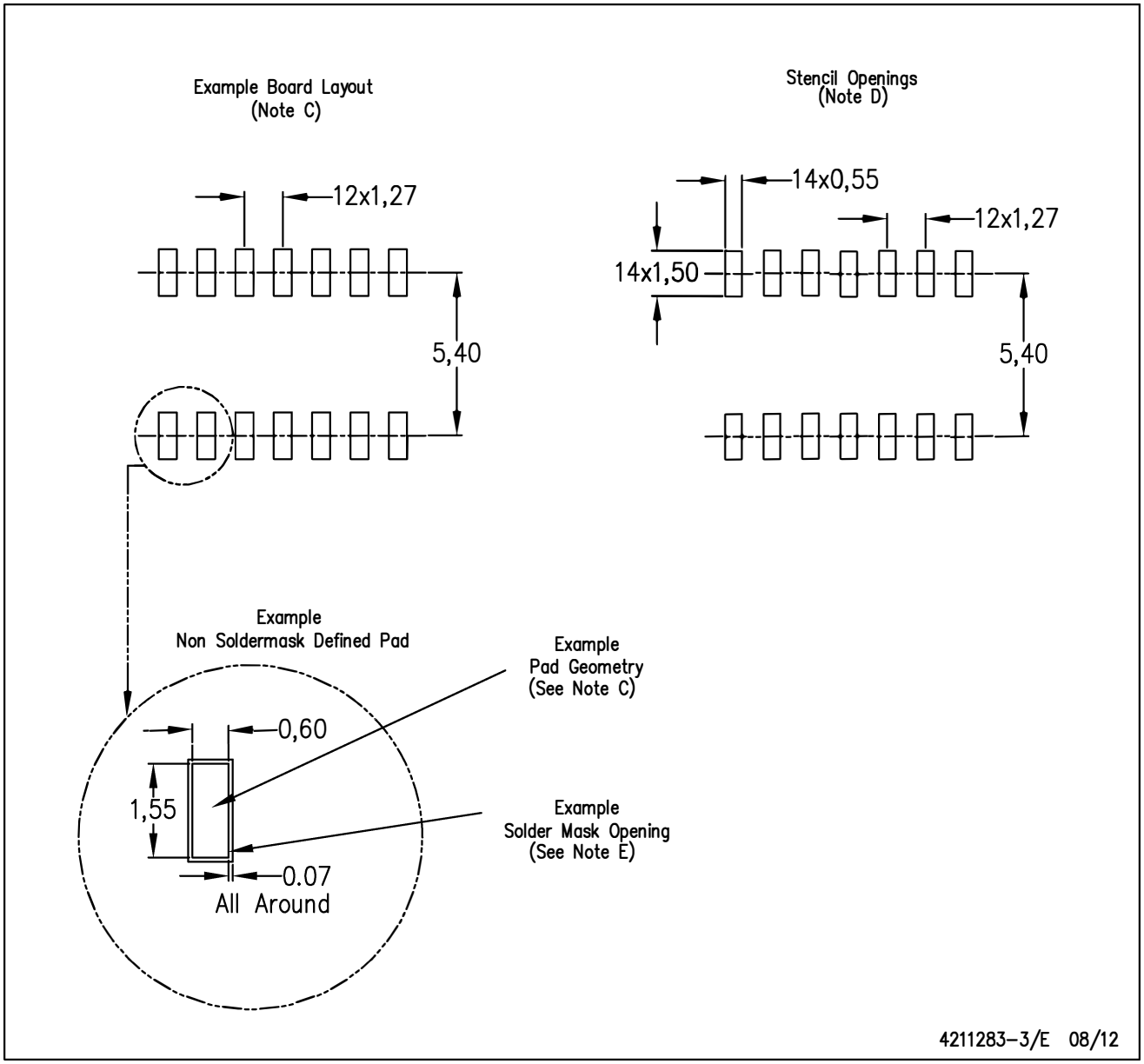
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



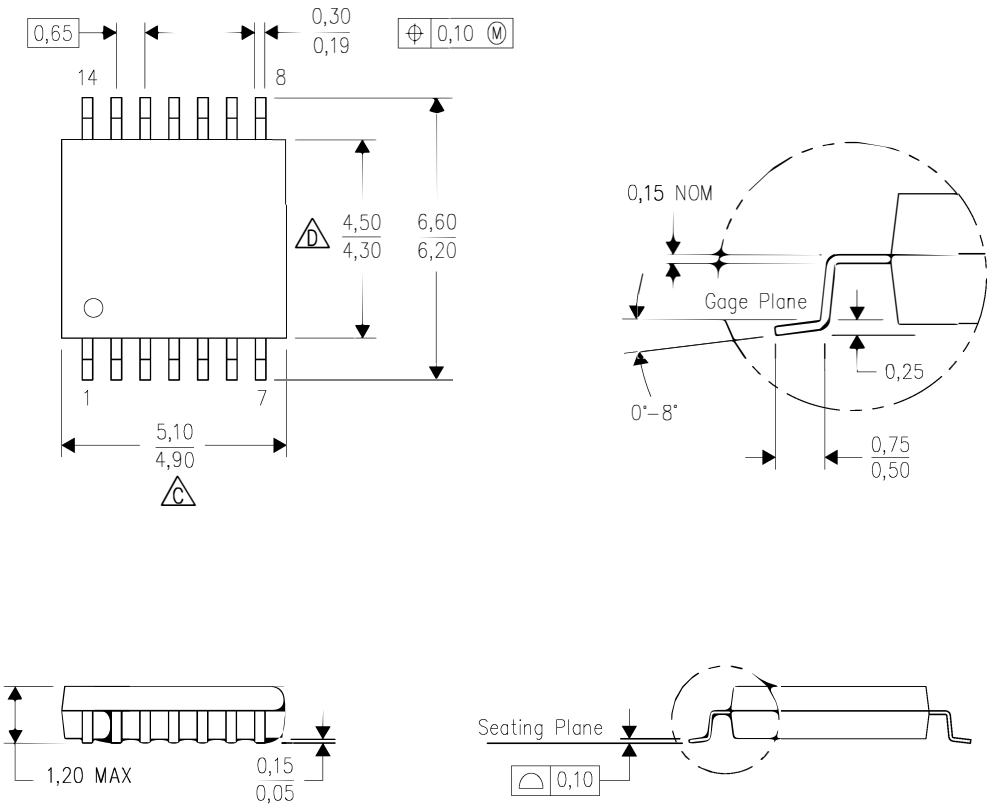
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

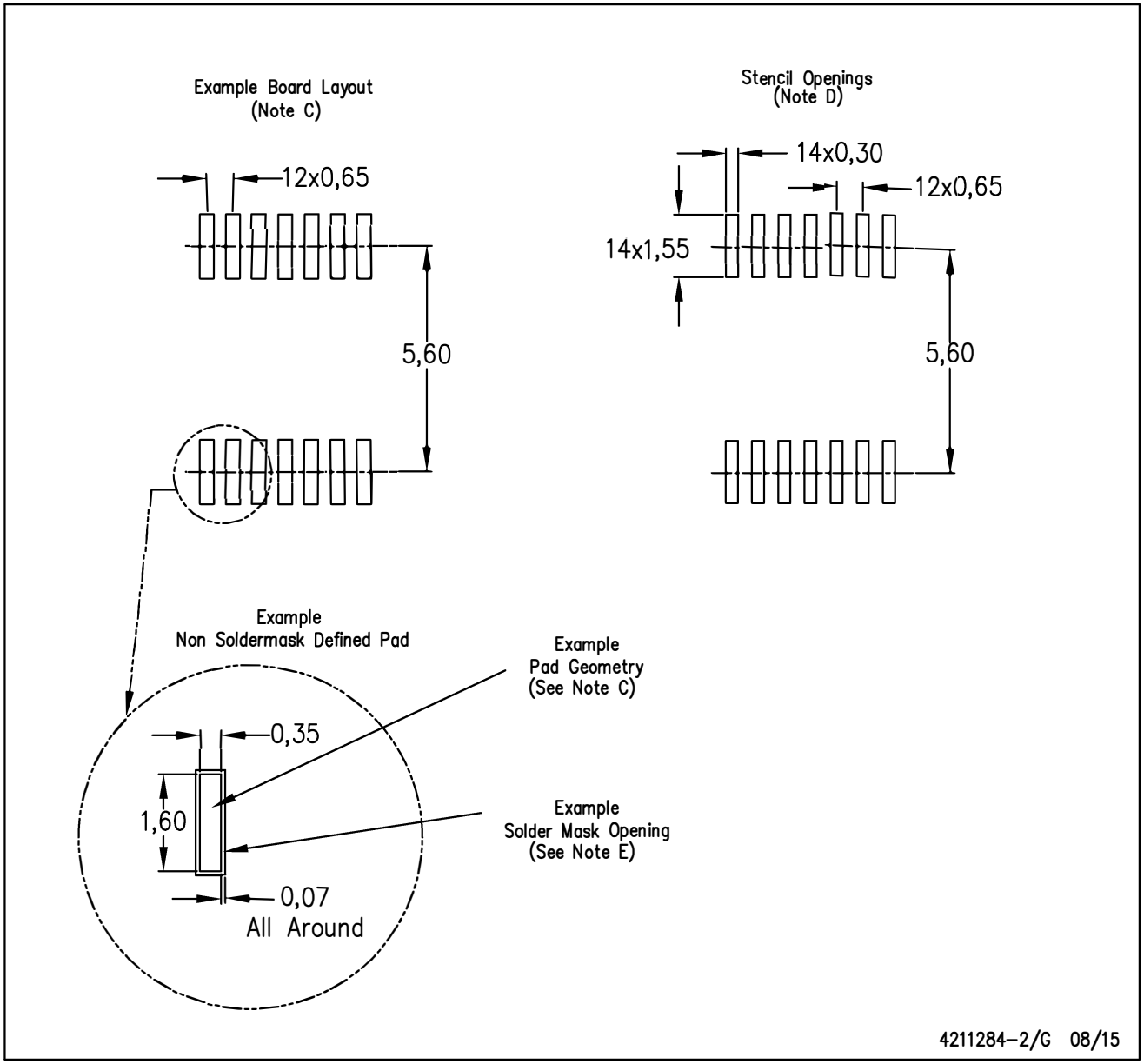
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



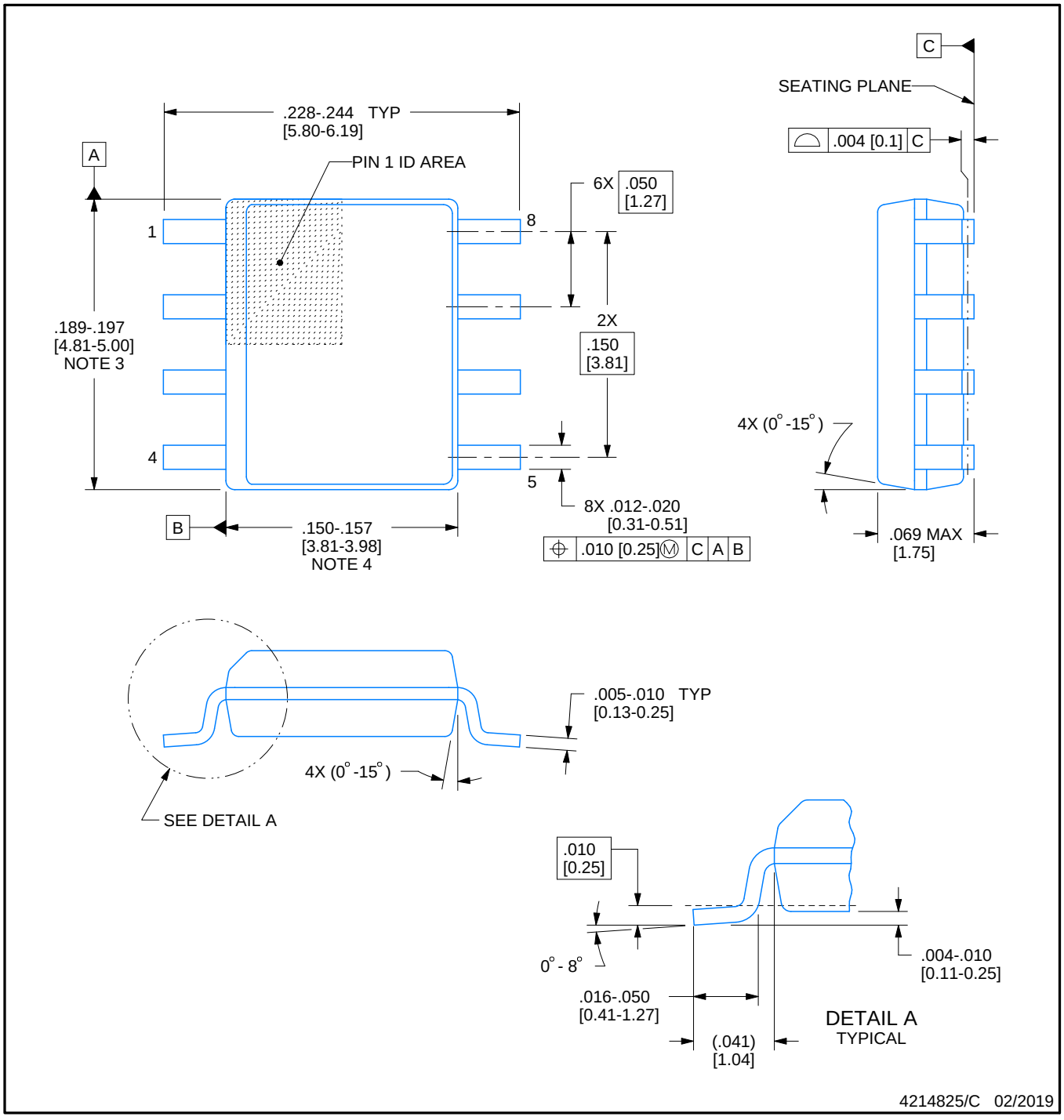
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

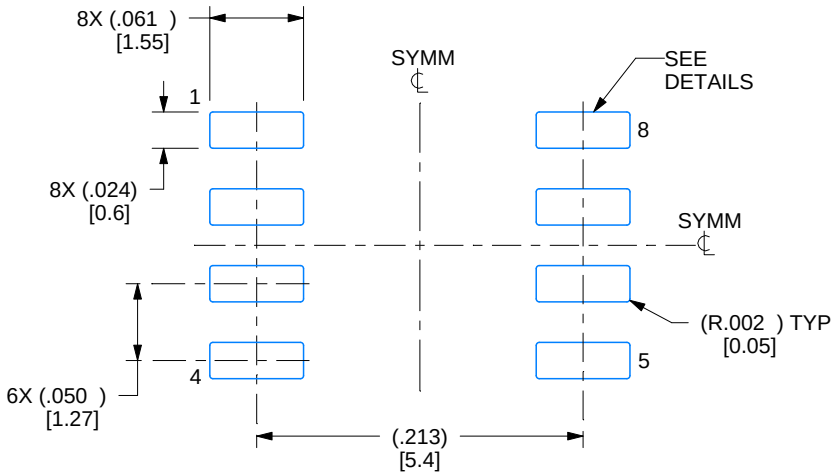
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

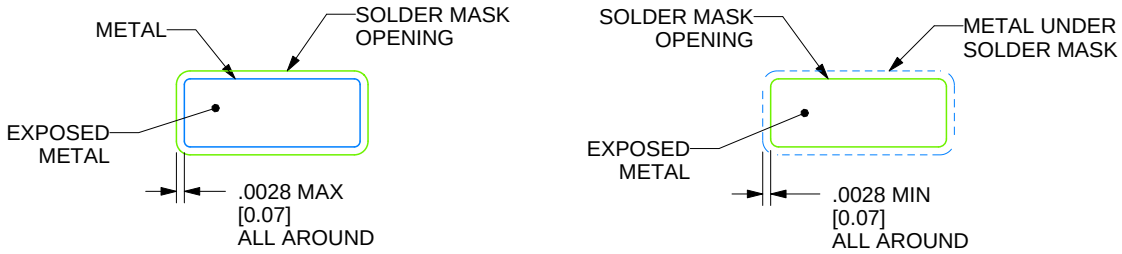
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

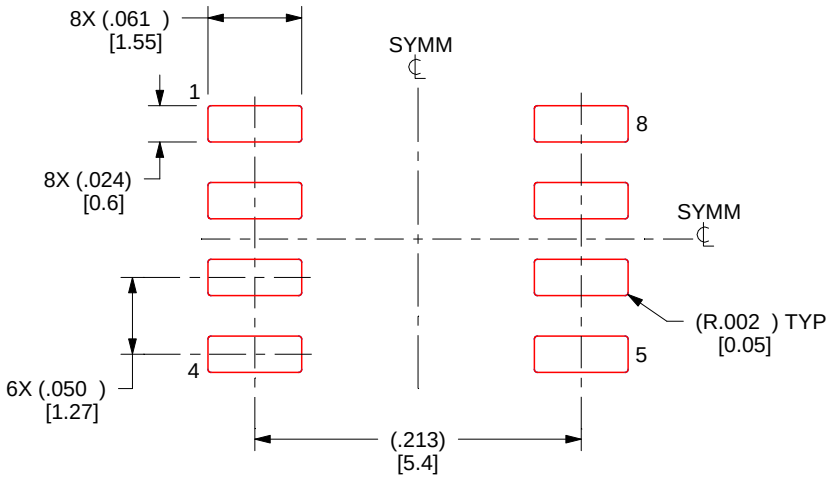
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



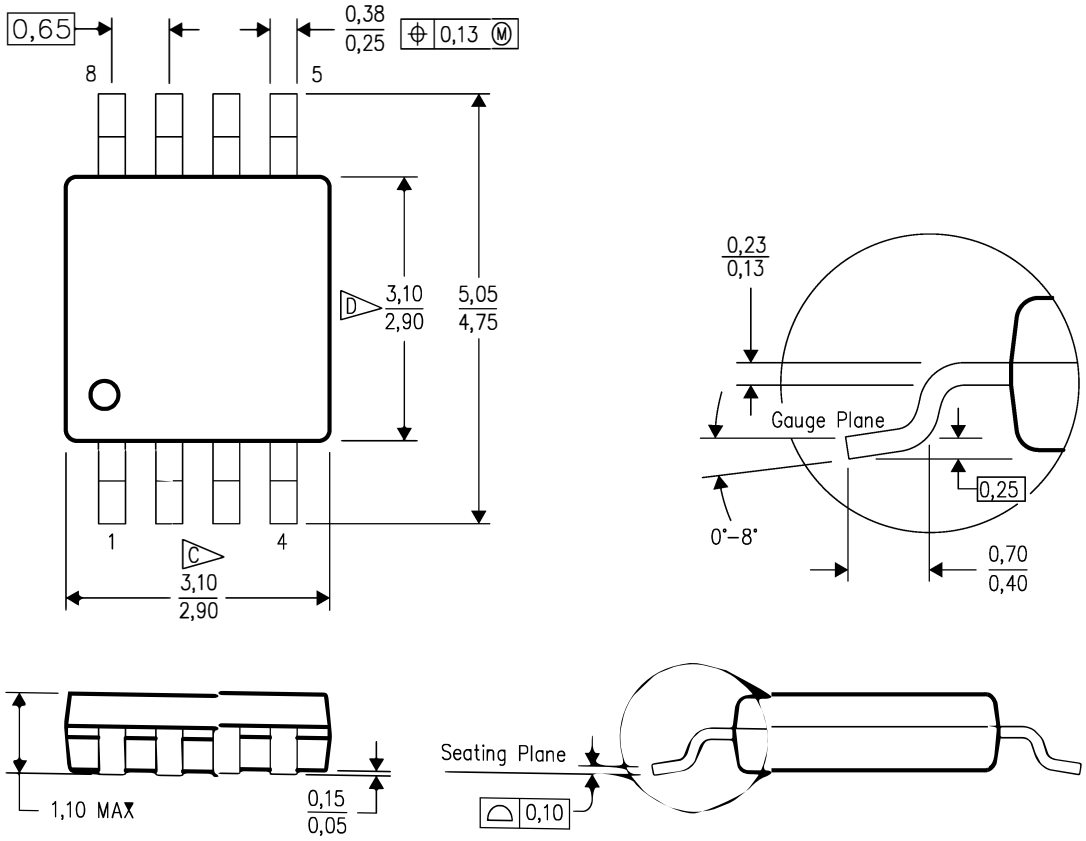
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

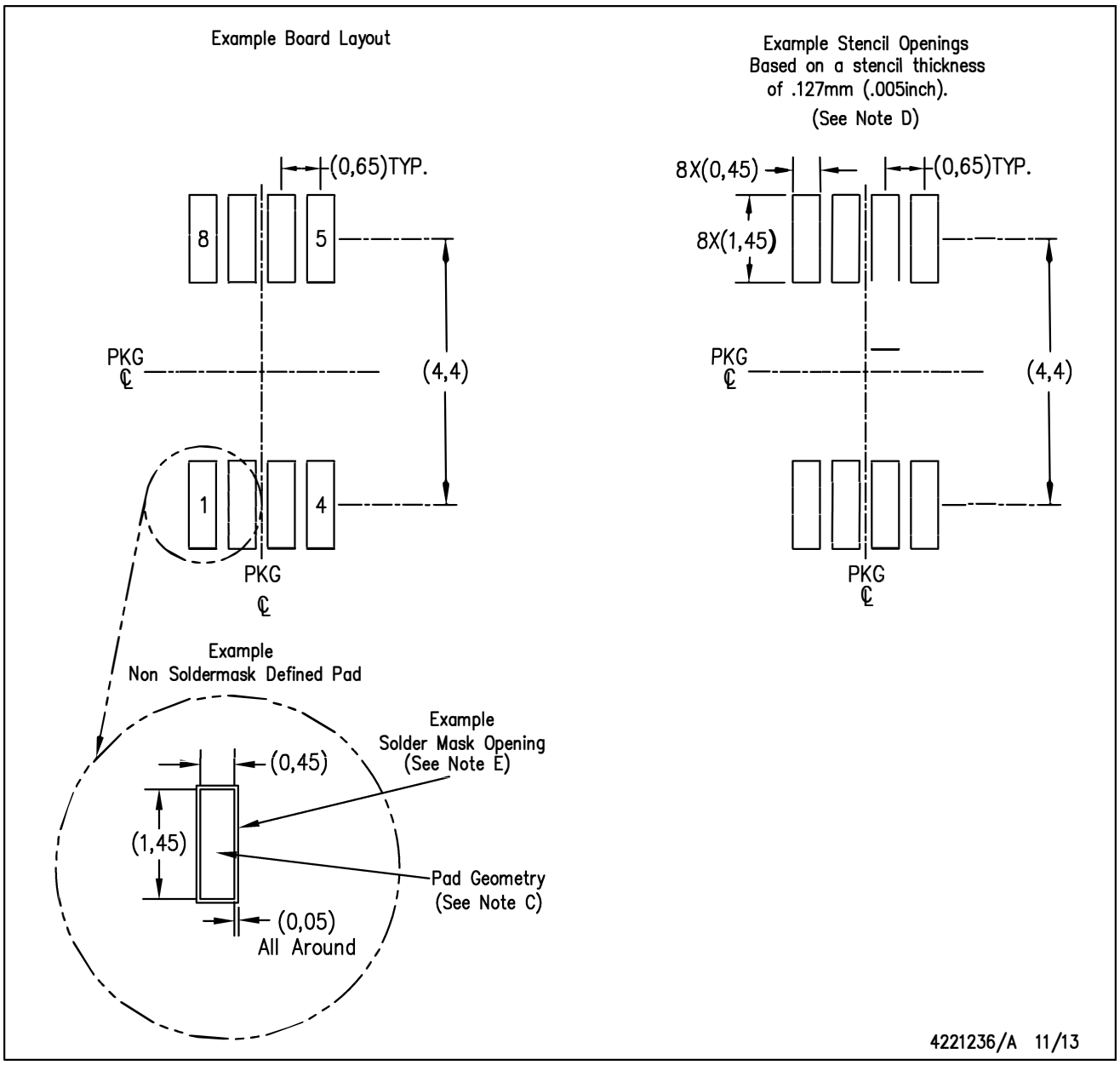
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

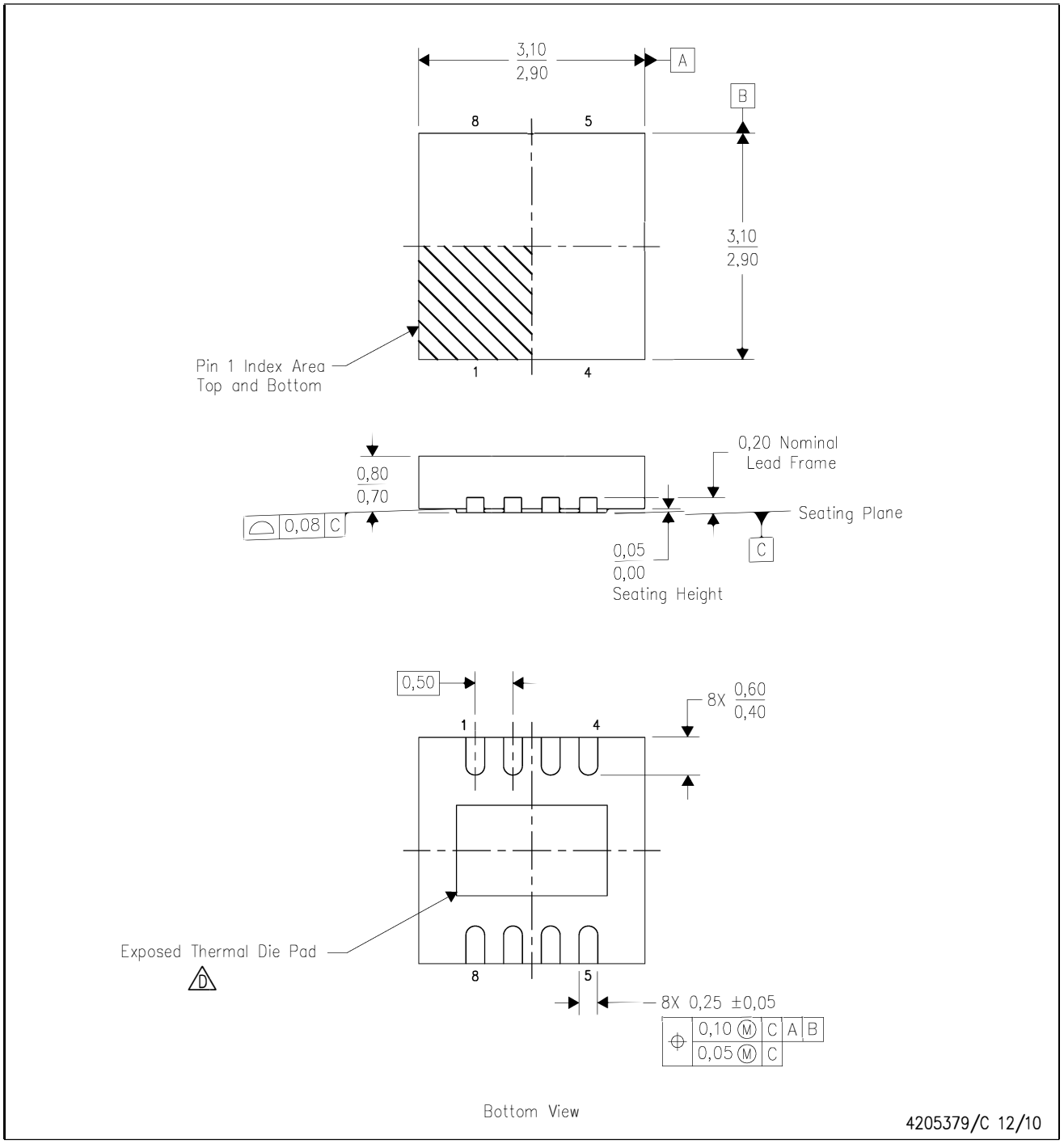
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.