SGM61180
4.5V to 18V Input, 8A, Synchronous Step-Down Converter

GENERAL DESCRIPTION

The SGM61180 is an efficient, 8A, synchronous, step-down converter with integrated power MOSFETs and a wide 4.5V to 18V input range. This current mode control device is optimized for high density applications with minimal number of external components. High switching frequency, up to 2MHz, can be chosen to reduce the solution size by smaller inductor and capacitors. This device can be used as a standalone or tracking power supply. The SS/TR pin can be used to control the output voltage startup ramp or as an input for tracking.

Power supply sequencing for two or more power supplies is possible by using the enable input (EN) and the open-drain power good output (PG) signals.

The high-side (HS) MOSFET current is cycle-by-cycle limited for overload protection. The low-side (LS) MOSFET sourcing current is also limited to prevent current runaway. The low-side switch also has a sinking current limit that turns it off if an excessive reverse current flows through it.

Thermal shutdown protection disables the device if the die temperature exceeds the shutdown threshold.

The SGM61180 is available in a Green TQFN-3.5×3.5-14L package and can operate over the wide ambient temperature range of -40℃ to +125℃.

FEATURES

- **Low Integrated R_{DSON} Switches: 24mΩ/16mΩ**
- **Split Rails for Supply (VIN) and Power (PVIN)**
  - **1.8V to 18V Range for PVIN**
  - **4.5V to 18V Range for VIN**
- **200kHz to 2MHz Switching Frequency**
- **External Clock Synchronization**
- **Voltage Tracking Capability**
- **0.6V Internal Reference Voltage**
- **±1% Reference Voltage Accuracy**
- **3.4μA (TYP) Shutdown Current**
- **Hiccup Mode Current Limit**
- **Monotonic Startup with Pre-biased Outputs**
- **Adjustable Soft-Start Time**
- **Power Sequencing Capability**
- **Power Good Output Monitor for Under-Voltage and Over-Voltage Protections**
- **Adjustable Input Under-Voltage Lockout (UVLO)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TQFN-3.5×3.5-14L Package**

APPLICATIONS

High Density Distributed Power Systems
High Performance Point of Load Regulation
Broadband, Networking and Optical Communications Infrastructure

TYPICAL APPLICATION

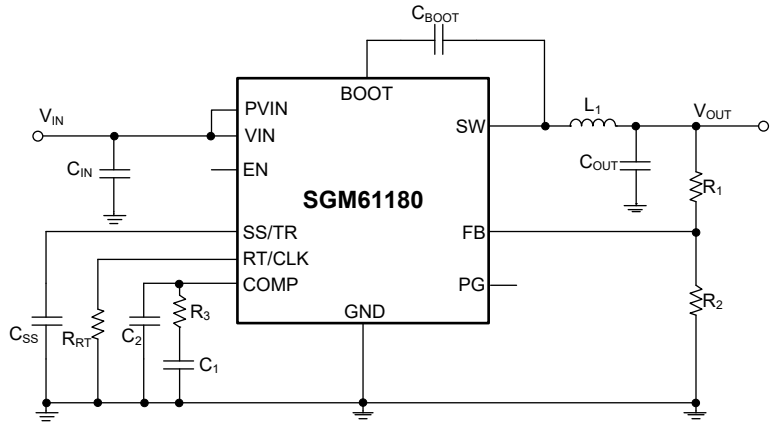


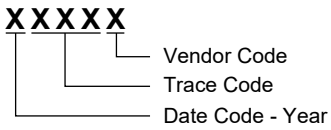
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61180	TQFN-3.5×3.5-14L	-40℃ to +125℃	SGM61180XTRI14G/TR	SGM 61180RI XXXXX	Tape and Reel, 6000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... -0.3V to 22V
PVIN Voltage ..... -0.3V to 22V
EN, PG, RT/CLK Voltage ..... -0.3V to 6V
BOOT Voltage ..... -0.3V to 29V
FB, COMP, SS/TR Voltage ..... -0.3V to 3V
BOOT-SW ..... 0V to 7V
SW ..... -1V to 22V
SW 10ns Transient ..... -3V to 22V
Package Thermal Resistance
TQFN-3.5×3.5-14L, θ_{JA} ..... 42℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 4.5V to 18V
Power Stage Input Voltage Range ..... 1.8V to 18V
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

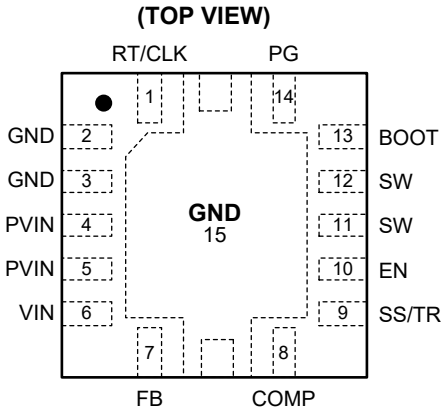
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFN-3.5×3.5-14L

PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
1	RT/CLK	I	An input pin for RT programming resistor or external CLK input (auto select) for setting the switching frequency. In RT mode, an external timing resistor connected between this pin and GND adjusts the switching frequency. In CLK mode, the device synchronizes to an external clock received by this pin.
2, 3	GND	G	Control circuit and low-side power MOSFET ground returns.
4, 5	PVIN	P	Power Input for the Power Stage Switches. PVIN voltage can be lower or higher than VIN voltage.
6	VIN	P	Power Input for the control circuitry.
7	FB	I	Inverting Input of the transconductance error amplifier with gm = 1450μA/V gain.
8	COMP	O	Error amplifier output and the input to the high-side switch current comparator. Connect the frequency compensation circuit between this pin and GND.
9	SS/TR	I/O	Soft-start and Tracking Input. Connect a capacitor between the SS and GND pins to set the rise time of the internal voltage reference. A voltage applied on this pin (TR) overrides the internal reference and the output will follow that voltage. This feature is used for tracking and sequencing functions.
10	EN	I	Enable Input Pin with Internal Pull-up. Float this pin to enable the device or pull it down to disable it. The EN input can be used to adjust the input UVLO by a resistor divider from VIN or PVIN.
11, 12	SW	O	Switching Node Output of the converter.
13	BOOT	I	Bootstrap Input to supply the high-side gate driver. A bootstrap capacitor (0.1μF) is required between the BOOT and SW pins. The voltage on this capacitor supplies the gate driver of the high-side MOSFET.
14	PG	O	Power Good Open-drain Output Pin. PG is released to go high by the external pull-up resistor if the output is in regulation. It is pulled low during soft-start, when EN is low or during fault events such as thermal shutdown, dropout and over-voltage.
Exposed Pad	GND	G	Package Thermal Pad and Analog Ground. This pad must be soldered to the ground plane for proper operation and heat relief. Connect it to a PCB ground on the top layer that is only connected to the GND pins and use it as reference for RT, COMP, SS/TR, UVLO setting and VIN bypass.

NOTE: I = input, O = output, I/O = input or output, G = ground, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +150℃, V_{IN} = 4.5V to 18V, V_{PVIN} = 1.8V to 18V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VIN and PVIN Pins)						
PVIN Operating Input Voltage	V_{PVIN}		1.8		18	V
PVIN OVP	V_{PVIN_OVP}	PVIN rising		24.4		V
PVIN OVP Hysteresis	$V_{PVIN\_OVP\_H}$	PVIN falling		0.3		V
VIN Operating Input Voltage	V_{IN}		4.5		18	V
VIN Internal UVLO Threshold	V_{IN_UVLO}	V_{IN} rising		4		V
VIN Internal UVLO Hysteresis	$V_{IN\_UVLO\_H}$			180		mV
VIN Shutdown Supply Current		EN = 0V		3.4		μA
VIN Non-Switching Operating Supply Current		V_{FB} = 610mV (to activate OVP and stop switching)		1.1		mA
Enable and UVLO (EN Pin)						
Enable Rising Threshold	$V_{ENRISING}$	Rising		1.2		V
Enable Falling Threshold	$V_{ENFALLING}$	Falling		1.15		V
Input Current	I_P	EN = 1.1V		1.1		μA
Hysteresis Current	I_H	EN = 1.3V		3.3		μA
Reference Voltage						
Reference Voltage	V_{REF}			0.6		V
Power MOSFETs						
HS Switch Resistance	R_{DSH}	BOOT-SW = 3.3V		27		mΩ
HS Switch Resistance (1)		BOOT-SW = 5V		24		mΩ
LS Switch Resistance (1)	R_{DSL}	V_{IN} = 12V		16		mΩ
Error Amplifier						
Error Amplifier Transconductance (gm)	gm_{EA}	-2μA < I_{COMP} < 2μA, V_{COMP} = 1V		1450		μA/V
Error Amplifier DC Gain	A_{DC}	V_{FB} = 0.6V		10000		V/V
Error Amplifier Source/Sink		V_{COMP} = 1V, 100mV input overdrive		±120		μA
Start Switching Threshold				0.79		V
COMP to I_{SWITCH} gm				21		A/V
Current Limit						
HS Switch Current Limit Threshold				14.5		A
LS Switch Sourcing Current Limit				11.5		A
LS Switch Sinking Current Limit				3		A
Hiccup Wait Time				512		Cycles
Hiccup Time Before Re-Start				16384		Cycles
Thermal Shutdown						
Thermal Shutdown	T_{SD}			175		℃
Thermal Shutdown Hysteresis	T_{SD_H}			15		℃

NOTE: 1. Measured at pins.

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +150℃, V_{IN} = 4.5V to 18V, V_{PVIN} = 1.8V to 18V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timing Resistor and External Clock (RT/CLK Pin)						
Minimum Switching Frequency	f_{SW}	R_{RT} = 240kΩ (1%)		210		kHz
Switching Frequency		R_{RT} = 100kΩ (1%)		480		
Maximum Switching Frequency		R_{RT} = 21.5kΩ (1%)		2000		
Minimum Pulse Width				20		ns
RT/CLK High Threshold					2	V
RT/CLK Low Threshold			0.8			V
RT/CLK Falling Edge to SW Rising Edge Delay		Measured at 500kHz with RT resistor in series		35		ns
Switching Frequency Range (RT Mode Set Point and PLL Mode)			200		2000	kHz
SW (SW Pin)						
Minimum On-Time	t_{ON}	Measured at 90% to 90% of V_{IN}, +25℃, I_{SW} = 2A		100		ns
Minimum Off-Time	t_{OFF}	BOOT-SW ≥ 3V		0		ns
BOOT (BOOT Pin)						
BOOT-SW UVLO				2.48		V
Slow Start and Tracking (SS/TR Pin)						
SS Charge Current	I_{SS}			2		μA
SS/TR to FB Matching	V_{SS_OFFSET}	$V_{SS/TR}$ = 0.4V		35		mV
Power Good (PG Pin)						
FB Threshold		V_{FB} falling (fault)		92% × V_{REF}		V
		V_{FB} rising (good)		94% × V_{REF}		
		V_{FB} rising (fault)		108% × V_{REF}		
		V_{FB} falling (good)		106% × V_{REF}		
Output High Leakage		V_{FB} = V_{REF}, V_{PG} = 5.5V		30		nA
Output Low		I_{PG} = 2mA		0.21		V
Minimum VIN for Valid Output		V_{PG} < 0.5V at 100μA		1.8		V
Minimum SS/TR Voltage for PG					1.4	V

FUNCTIONAL BLOCK DIAGRAM

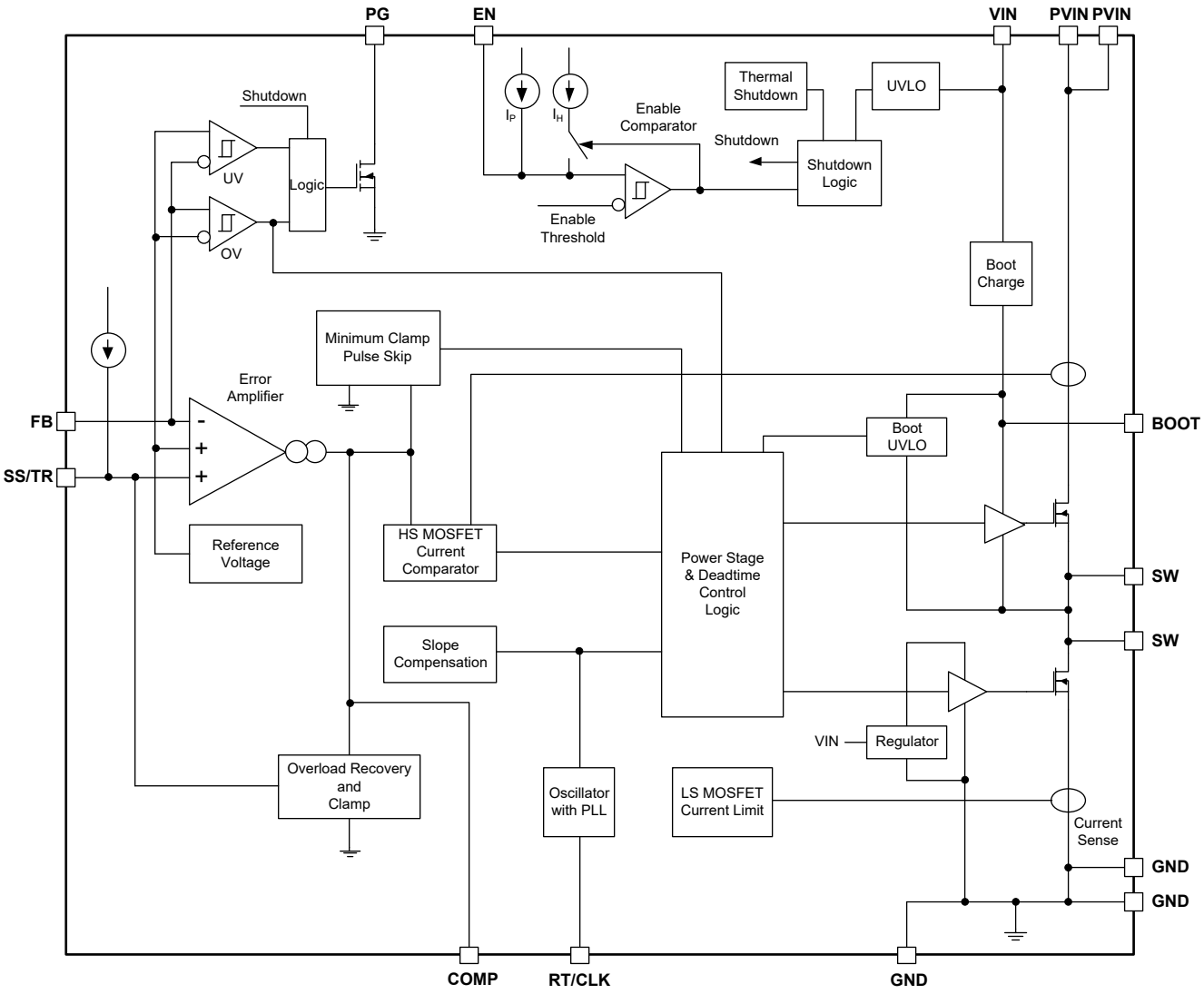


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61180 is an 8A output synchronous step-down converter with integrated N-channel MOSFET switches. It can operate from an input voltage range of 4.5V to 18V. The output voltage can be set as low as 0.6V, which is equal to the device internal reference voltage (V_{REF}).

As a constant frequency, peak current mode control device, SGM61180 can provide fast transient response with a simple compensation circuit. The fixed switching frequency is adjustable from 200kHz to 2000kHz to allow optimizing of the efficiency and size of the converter. The internal switching frequency is set by an external R_{RT} resistor connected between the RT/CLK pin and GND. The device also accepts an external clock source on this pin to synchronize the oscillator using the internal phase locked loop (PLL). Beginning of each switching cycle (ON pulse) is synchronized to the CLK falling edge.

This device can have a safe and monotonic startup in output pre-biased conditions. The V_{IN} must exceed the under-voltage lockout threshold (UVLO, 4V TYP) for device power-up. The UVLO thresholds can be adjusted (increased) by connecting the EN pin to the tap point of a resistor divider between the VIN (or PVIN) pin and GND. The EN internal pull-up current source and the resistor divider determine the UVLO thresholds. When the EN is floated or is pulled high, the device is enabled and the total device current (no switching) is near 1100μA. Pulling the EN pin low will shut down the device with less than 3.4μA (TYP) supply current.

The integrated MOSFETs are optimized for higher efficiency at lower duty cycles. They can efficiently provide up to 8A continuous output current.

The integrated bootstrap circuit along with the external boot capacitor provides the bias voltage for the high-side MOSFET driver. The voltage of the bootstrap capacitor that is placed between the BOOT and SW pins is continuously monitored for bootstrap UVLO (BOOT-SW UVLO) detection. If the boot capacitor voltage drops below the bootstrap UVLO, the SW pin will be pulled low to recharge the boot capacitor. Such condition may occur only if the on-time is too short or there is no switching for a relatively long period. 100% duty cycle operation is possible as long as the boot capacitor voltage is higher than the 2.48V (TYP) threshold (preset UVLO level).

The device has a power good hysteresis comparator (PG) that monitors the output voltage through the FB pin. The PG pin is connected to an open-drain MOSFET. It is pulled low when the FB pin voltage is less than 92% or greater than 108% of the reference voltage V_{REF} and is asserted high when the FB pin voltage is within 94% to 106% range of the V_{REF}.

The SS/TR (soft-start/tracking) pin can be used to minimize the inrush currents (soft-start function) with a small value capacitor, or for power supply sequencing during power-up with a resistor divider from preceding voltage rail. It is the input pin for the voltage that is followed by the output when the power supply is used in the tracking mode.

The SGM61180 is protected from output over-voltage, over-current, and over-heating damage. The output over-voltage transients are effectively minimized by the over-voltage comparator of the power good circuit. When an over-voltage is detected, the high-side MOSFET is turned off and prohibited from turning on until the FB pin voltage falls below 106% of the V_{REF}.

High-side MOSFET is naturally protected from sourcing over-current by peak current mode control. The low-side MOSFET is also protected bidirectionally against over-current. This feature helps the control of the inductor current to avoid current runaway.

If a die temperature is too high ($T_J > T_{SD}$), the device will stop switching and go to shutdown state. It will automatically recover with a soft-start when the junction temperature drops 15℃ (TYP) below the shutdown temperature.

Note that a continued overload condition may cause a cycling thermal shutdown and recovery. It will depend on the temperature and the ventilation conditions of the system.

DETAILED DESCRIPTION (continued)

Constant Frequency PWM

The SGM61180 has an internal oscillator with adjustable constant frequency that can be synchronized (PLL) to an external clock. Each switching cycle (ON pulse) starts with the falling edge of the clock. The output voltage is sensed by the V_{OUT} resistor divider and fed back to the FB pin. This voltage is compared with the internal reference by the error amplifier (EA) that drives the COMP output pin. The EA output current is injected into the external compensation network to create the control voltage for the PWM modulator as the set point for the peak current of the high-side switch. When the high-side switch current reaches this reference, it is turned off and the low-side switch is turned on until the end of switching cycle. A slope compensation block slightly reduces the sensed high-side switch current before comparison (depending on the on-time) to avoid sub-harmonic oscillations.

Continuous Current Mode Operation (CCM)

As a synchronous step-down converter, the device normally works in continuous conduction mode (CCM) under all load conditions (forced PWM). Therefore, under light load conditions the inductor current can be negative when the low-side switch is ON.

Power Input Pins

VIN and PVIN pins can be tied together or separated depending on the application and minimum input voltage. The VIN pin supplies the internal circuits of the device and needs to be above 4.5V, while the PVIN provides the supply voltage for the switches and can go down to 1.8V. So, if these pins are tied, the input voltage range is from 4.5V to 18V. A voltage divider connected to the EN pin from either VIN or PVIN can be used to adjust the power supply UVLO. For a consistent power-up behavior, PVIN is the recommended source for the UVLO programming.

Reference Voltage (V_{REF})

A precise 0.6V reference is internally implemented by scaling the output of a temperature-stable bandgap circuit. The reference voltage tolerance over the whole temperature range is ±1.5%. The actual reference voltage for output setting is changed during startup or tracking.

Output Voltage Setting

A resistor divider connecting the output (V_{OUT}) to the FB pin (see Figure 1) is used to set the output voltage. Use resistors with 1% tolerance or better for good output accuracy. Equation 1 can be used to calculate the R_1 and R_2 (upper and lower resistors) values based on the desired output voltage (V_{OUT}) and V_{REF}.

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_2 \quad (1)$$

where:

• V_{REF} = 0.6V.

For example, a 10kΩ resistor can be chosen for R_2 and then R_1 is calculated. Do not choose too large resistors that may cause output errors due to the FB bias current or make the regulator susceptible to the noises coupled to the FB input.

The minimum and maximum adjustable output voltages are limited by the minimum on-time of the high-side switch and the required bootstrap voltage respectively. More details are provided in the Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle) section.

Startup with Pre-biased Output

The low-side switch is prohibited from turning on and discharging the output if a pre-biased voltage is sensed on the output before startup. As long as the SS/TR pin voltage is below V_{FB}, the low-side switch is not allowed to sink current to have a monotonic startup with pre-biased output.

Error Amplifier

A transconductance error amplifier (EA) compares the FB voltage with the lower of the SS/TR pin voltage and the internal 0.6V reference. The gain of the error amplifier is 1450μA/V in normal conditions. The frequency compensation network is placed between the COMP pin and GND.

Slope Compensation

To avoid sub-harmonic oscillations that result in unstable PWM pulses, a small negative-slope compensating ramp is added to the measured switch current before it is used to generate the PWM signal. The limit for the peak inductor current is not affected and is constant over the full duty cycle range.

DETAILED DESCRIPTION (continued)

EN Pin and UVLO Programming

The EN pin is used to turn the device on and off. The device starts operation when the EN voltage rises above the enable rising threshold. Pulling the EN voltage below the enable falling threshold stops switching and reduces the device current to the very low quiescent shutdown level. Floating the EN pin will enable the device due to its internal pull-up current source. This current source is used for programming the UVLO threshold. An open-drain or open-collector output connected to the EN pin can be used to control the device. An internal UVLO circuit is implemented on the VIN pin to disable the device and prevent malfunction when the supply voltage is too low. The internal VIN UVLO hysteresis is 180mV. To program a higher UVLO threshold for the VIN or to add a secondary UVLO on the PVIN that is typically needed for split-rail applications, the EN pin can be configured to one of the configurations shown in Figure 3, Figure 4, or Figure 5. Without external components, the internal pull-up current (I_P) sets the EN pin default state to enable. When the device is enabled, the second current source (I_H) is activated. I_P and I_H are used to set the UVLO.

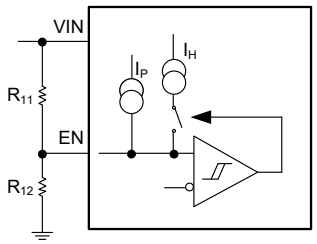


Figure 3. VIN UVLO Setting with a Resistor Divider

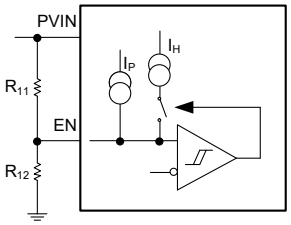


Figure 4. PVIN UVLO Setting with a Resistor Divider (V_{IN} ≥ 4.5V)

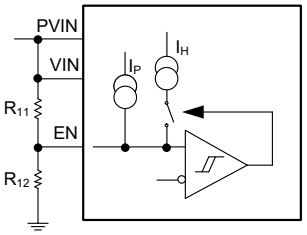


Figure 5. VIN and PVIN UVLO Setting

The resistor divider can be calculated from Equations 2 and 3 based on the desired UVLO start and stop thresholds. A 500mV or higher hysteresis (V_{START} - V_{STOP}) is recommended for the UVLO programming.

$$R_{11} = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_H} \quad (2)$$

$$R_{12} = \frac{R_{11} \times V_{ENRISING}}{V_{STOP} - V_{ENFALLING} + R_{11}(I_P + I_H)} \quad (3)$$

where:

- I_H = 3.3μA.
- I_P = 1.1μA.
- $V_{ENRISING}$ = 1.2V.
- $V_{ENFALLING}$ = 1.15V.

If a UVLO or thermal shutdown event occurs, the EN pin is internally pulled below 1.2V and the device is disabled. When the shutdown condition is cleared, the pull-down is removed and the device is powered up again. However, the switching will not start until the SS/TR voltage is completely discharged to ground to ensure a complete soft-start process.

Frequency and Synchronization (RT/CLK)

The switching frequency can be set in two modes by the RT/CLK pin.

In the RT mode, a resistor (R_{RT}) is placed between the RT/CLK and GND pins to set the free running switching frequency of the PLL. It can be set between 200kHz to 2000kHz by choosing R_{RT} resistor between 240kΩ to 21.5kΩ respectively.

In the CLK mode, an external clock drives the RT/CLK pin and the internal switching clock oscillator is synchronized to CLK by the PLL. The CLK mode overrides the RT mode. The device automatically detects the input clock and switches to the CLK mode.

DETAILED DESCRIPTION (continued)

Slow Start (SS/TR)

The lower voltage between the internal V_{REF} and the SS/TR pin is used as the reference to regulate the output. The soft-start capacitor is connected to the SS/TR pin and is charged by a 2μA internal current source to set the soft-start time (t_{SS}).

Equation 4 can be used to calculate the soft-start time for a selected soft-start capacitor (C_{SS}).

$$t_{SS}\ (ms) = \left(\frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \right) \quad (4)$$

where:

• V_{REF} = 0.6V.

• I_{SS} is the soft-start current source (2μA).

Power Good (PG)

The PG is an open-drain output. It is released if there is no fault and the FB pin voltage is in regulation. The PG is pulled low if the FB voltage is lower than 92% or above 108% of the reference voltage. It is also pulled low if the EN pin is pulled low or the SS/TR pin is below 1.4V, or if a fault such as UVLO or thermal shutdown occurs.

A 10kΩ to 100kΩ pull-up resistor connected to a voltage rail less than 5.5V is recommended for PG. An option is using the output voltage for PG pull-up. The state of PG is valid only if the V_{IN} > 1.8V. The current sinking capability of PG is limited until V_{IN} exceeds the 4.5V at which the full sinking capacity is available.

Output Over-Voltage Protection (OVP)

An output over-voltage protection (OVP) circuit is implemented to protect the output from over-voltage and to minimize the overshoots. Usually an OVP occurs after removal of an overload condition. When the output voltage is dropped due to a persisting overload, the error amplifier output reaches to its maximum and forces the converter to provide the maximum output current. Upon removal of the overload condition, the regulator output rises quickly because the high inductor current charges the output capacitor rapidly, especially if C_{OUT} is small. The error amplifier will respond and re-adjust itself but not as fast as the output filter (LC) and an overshoot occurs.

The OVP feature reduces the overshoot by comparing the FB pin voltage and the OVP threshold. If the threshold is exceeded, the high-side MOSFET is turned off to stop feeding current to the output. When the FB voltage drops below the OVP threshold, the high-side MOSFET can turn on again in the next cycle.

Over-Current Protection

Both high-side (HS) and low-side (LS) switches are protected from over-current with cycle-by-cycle current limiting as will be explained in the next two sections.

High-side Switch Over-Current Protection

Using current mode control, the pulse width (from the beginning of the cycle until HS turn-off) is determined by the compensator output voltage (V_{COMP} at COMP pin) in a cycle-by-cycle basis. In each cycle the high-side switch current is continuously compared with the current set point determined by compensator output (V_{COMP}) and when the high-side current reaches to that reference (peak current), the high-side switch is turned off.

Low-side MOSFET Over-Current Protection

The current of the low-side switch is continuously monitored while it is turned on. Normally, the low-side switch sources current from ground to the load through the inductor. At the end of each cycle, the low-side sourcing current is compared to a limit that is slightly lower than the high-side limit. If at the end of the cycle the low-side current is higher than this limit, it will continue to remain on in the next cycle and the high-side switch remains off. The high-side switch can turn on again when the low-side current falls below low-side sourcing limit at the beginning of a new cycle.

In some operating conditions, the low-side switch sinks current from the load to the ground. The low-side sinking current has a typical limit of 3A. If this limit is exceeded, the low-side switch will immediately turn off and both switches will not turn on until the end of the cycle.

Thermal Shutdown

The device is forced to stop switching by thermal shutdown if the junction temperature exceeds +175℃. When the temperature falls below +160℃, a new power-up sequence will initiate automatically.

DETAILED DESCRIPTION (continued)

Feedback Loop Small Signal Model

The equivalent small signal model of the control loop for frequency response and transient analysis is given in Figure 6.

The compensation network (R_3, C_1 and C_2) is placed in the output of the transconductance error amplifier (EA). The EA has a gain of 1450μA/V and is modeled as an ideal voltage controlled current source. The R_{OEA} (7.14MΩ) and C_{OEA} (20.7pF) model the frequency response of the EA. Power converter is modeled with a pure 21A/V gain. The inductor dynamics is effectively removed in the cycle-by-cycle average small signal model, because with the current mode control the inductor average current is set by the compensator. The C_O and R_{ESR} model the output capacitance and its parasitic ESR. To measure the frequency response, the loop is broken at points 'a' and 'b' to insert a small signal (e.g. 1mV) AC source. For small signal frequency response analysis, the magnitude and phase versus frequency for the output to input transfer functions of each stage is plotted. The 'a/c' (power stage gain), 'c/b' (compensation gain) and 'a/b' (loop gain) voltage ratios are commonly used for the analysis. To simulate or test the response of the output to load steps in time domain (dynamic loop response), the load (R_L) is replaced with a stepping current source with proper amplitude, repetition rate and rate of change (A/μs) depending on the application. As a common example, stepping between 25% and 75% of the nominal load with ±1A/μs slew rate and repeating at 1kHz or 10kHz, can be used for testing and comparison of the power supply transient response to rapid load changes.

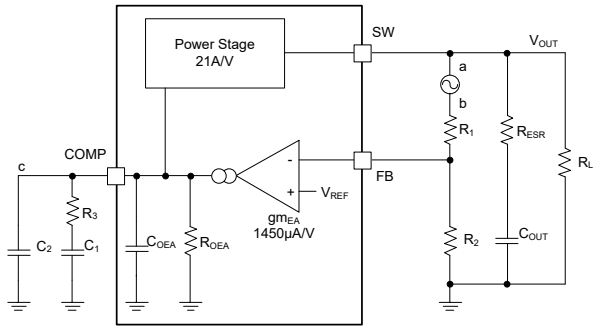


Figure 6. Small Signal Model for Loop Response

Simplified Model for Peak Current Mode

A simplified small signal model to design the frequency compensation network is given in Figure 7. The power stage and duty cycle modulator are approximated by a voltage-controlled current source (VCCS) that is controlled by the error amplifier output (V_{COMP}) and provides current to the output capacitor and the load. The control-to-output transfer function (V_{OUT}/V_{COMP}) consists of a DC voltage gain (A_{DC}), a dominant pole (f_P) determined by $R_L \times C_O$ time constant, and a simple ESR-zero (f_Z) determined by $R_{ESR} \times C_O$ time constant as given in Equations 5, 6, 7 and 8. The VCCS transconductance is the ratio of the output current change to the control voltage (COMP) change. This is equivalent to the power stage transconductance gain (gm_{PS}) that is 21A/V for this device. The DC voltage gain (A_{DC}) of the power stage is the product of gm_{PS}, and the load resistance (R_L) as stated in Equation 6 for the resistive loads. Note that when the load current increases, the DC gain decreases. This relationship can be problematic because it could move the crossover frequency of the converter in the same way.

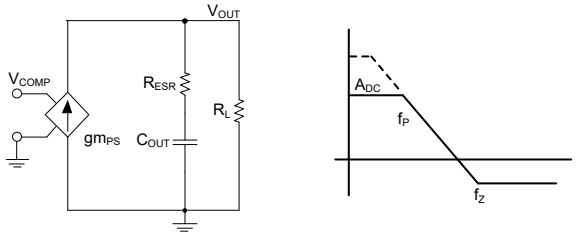


Figure 7. Simplified Model for Peak Current Mode Control and Frequency Response

$$\frac{V_{OUT}(V)}{V_{COMP}} = A_{DC} \times \frac{(1 + \frac{s}{2\pi \times f_Z})}{(1 + \frac{s}{2\pi \times f_P})} \quad (5)$$

$$A_{DC} = gm_{PS} \times R_L \quad (6)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (7)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (8)$$

where:

- gm_{PS} is the gain of the power stage (21A/V).
- R_L is the load resistance.
- C_{OUT} is the output capacitance.
- R_{ESR} is the equivalent series resistance of the output capacitor.

DETAILED DESCRIPTION (continued)

Fortunately, the dominant pole also moves with load current as given in Equation 7. As highlighted in Figure 7, the crossover frequency (0dB gain location) is not affected by the combined effect. As the load current decreases, the gain increases and the pole frequency decreases. Having a fixed crossover frequency simplifies the design of the frequency compensation for a changing load.

Small Signal Model for Frequency Compensation

The SGM61180 can easily use the common Type 2 and 3 compensation circuits, as shown in Figure 8. Compared to Type 2B, the Type 2A compensation has an extra high-frequency pole (by C_6) to attenuate high-frequency noise and ensure that gain remains very low at high frequencies against the ESR-zero effect that tends to increase the gain at higher frequencies. In the Type 3 compensation, the additional C_{10} capacitor is added in parallel to the upper feedback resistor divider for phase boost at the crossover frequency. An extra resistor may be used in series with C_{10} for more control on the phase boost. The following guidelines are provided for designers who prefer to compensate by the standard loop design method. The equations can only apply to applications in which the ESR-zero is above the bandwidth (crossover frequency) of the control loop. This condition is usually valid when ceramic output capacitors are used. For low frequency ESR-zeros (capacitors with high ESR) see the Application Information section for a step-by-step design procedure.

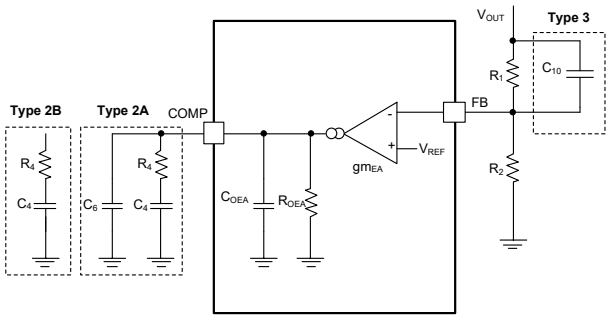


Figure 8. Types of Frequency Compensation

General Guidelines for Loop Compensation Design

1. Determine the crossover frequency (f_C). A good starting point is 1/10th of the switching frequency (f_{SW}). C_O is also initially chosen based on the switching frequency and ripple requirement.

2. R_4 can be determined by:

$$R_4 = \frac{2\pi \times f_c \times V_{OUT} \times C_O}{gm_{EA} \times V_{REF} \times gm_{ps}} \quad (9)$$

where:

- gm_{EA} is the gm amplifier gain (1450μA/V).
- gm_{PS} is the power stage gain (21A/V).
- V_{REF} is the reference voltage (0.6V).

3. Place a compensating zero at the dominant pole of the converter that is at $f_P = \frac{1}{C_O \times R_L \times 2\pi}$.

C_4 can be determined by:

$$C_4 = \frac{R_L \times C_O}{R_4} \quad (10)$$

4. C_6 is optional and adds a high frequency pole to cancel the zero created by the output capacitor ESR.

$$C_6 = \frac{R_{ESR} \times C_O}{R_4} \quad (11)$$

5. C_{10} can be added for Type 3 compensation that allows a slightly higher bandwidth and better phase margin. If C_{10} is needed, use Equation 12.

$$C_{10} = \frac{R_L \times C_O}{2\pi \times R_8 \times f_C} \quad (12)$$

DETAILED DESCRIPTION (continued)

Device Functional Modes

Switching Frequency Setting (RT Mode)

Selection of the switching frequency is generally a tradeoff between the solution size, efficiency, and the minimum controllable on-time. The RT resistance can be designed from Equation 13.

$$R_{RT}\ (k\Omega) = 74920 \times f_{SW}\ (kHz)^{-1.074} \quad (13)$$

Synchronization (CLK Mode)

The device uses an internal phase locked loop (PLL) to set or synchronize to an external clock signal with 200kHz to 2000kHz range. Mode change from RT mode to CLK mode is allowed.

For stable synchronization, a square wave clock with 20% to 80% duty cycle must be applied to the RT/CLK pin. The logic low and high levels of the clock must be below 0.8V and above 2.0V respectively. The switching cycle starts with the falling edge of the RT/CLK signal.

If both RT and CLK modes are needed in an application, configuration shown in Figure 9 can be used. Without the external clock, the switching is set by R_{RT} (RT mode) and when the clock is present, the CLK mode overrides the RT mode. Mode switch occurs when the RT/CLK is pulled above 2.0V for the first time. Upon switching to the CLK mode, the RT/CLK pin becomes high impedance and the PLL starts to lock into the external clock frequency. Going back from CLK mode to RT mode is not recommended because by removing clock, the switching frequency drops to around 100kHz first (waiting for synchronize clock) before recovery to the free running frequency that is set by RT resistor.

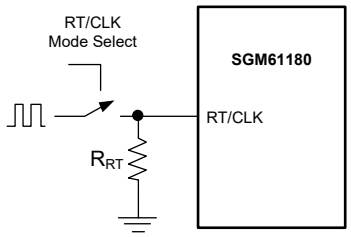


Figure 9. Using RT and CLK Modes Together

Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle)

An integrated bootstrap regulator is used for powering the high-side MOSFET gate driver. A small 0.1μF ceramic capacitor (X5R or X7R grade) with at least 10V rating is required between the BOOT and SW pins to supply the gate driver. It is recharged from VIN source through an internal switch every time the SW goes low. Recharge happens when the BOOT pin voltage is less than V_{IN} and the BOOT-SW voltage is below the required regulation for the high-side gate voltage.

The SGM61180 is designed to operate at 100% duty cycle for low converter dropout, as long as the BOOT to SW voltage is above the BOOT-SW UVLO threshold (2.48V TYP). If the BOOT-SW voltage drops below its UVLO threshold, the high-side switch turns off and the low-side switch turns on to recharge the boot capacitor. If the input voltage rails are split (separate VIN and PVIN sources), the 100% duty cycle operation can be achieved continuously, as long as V_{IN} is at least 4V above V_{PVIN}.

Startup Sequencing (SS/TR)

The SS/TR, EN and PG pins allow the implementation of common power supply sequencing methods. A simple sequencing approach is shown in Figure 10 in which the right side SGM61180 device is powered up after the left one. The PG of the first device is coupled to the EN pin of the second. The second power supply is enabled after the primary supply reaches regulation.

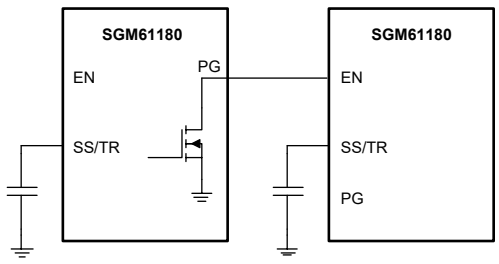


Figure 10. Sequential Startup Sequence

DETAILED DESCRIPTION (continued)

Figure 11 shows the ratiometric sequencing of two converters. The SS/TR and EN inputs of the two devices are tied together. In this configuration, the I_{SS} current sources from the SS/TR pins are added together and 2 × I_{SS} should be considered to calculate the soft-start capacitor from Equation 4.

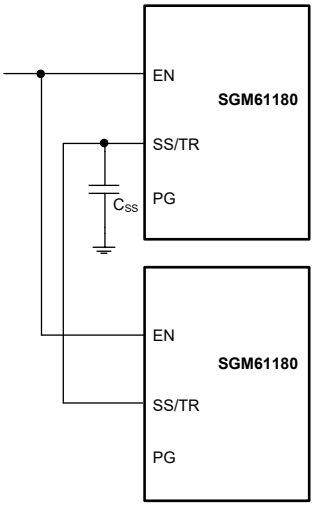


Figure 11. Ratiometric Sequencing of Two Devices

Simultaneous ratiometric sequencing can also be implemented by using a resistor divider as shown in Figure 12 by R_1 and R_2.

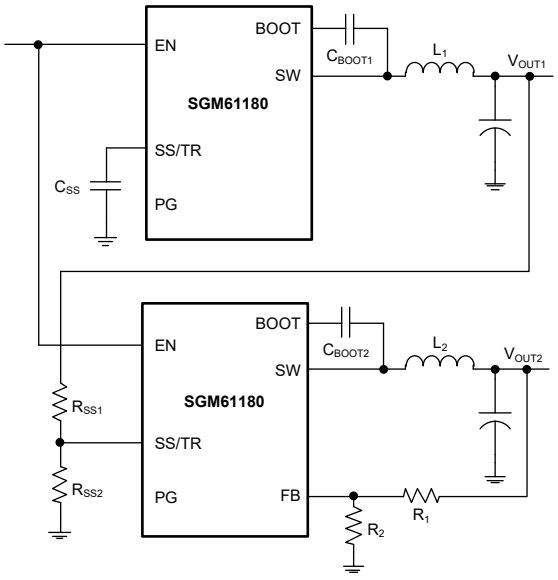


Figure 12. Ratiometric and Simultaneous Startup Sequence

In this example, the second power supply output (V_{OUT2}) tracks V_{OUT1} (the output of the first power supply).

By proper selection of R_1 and R_2, V_{OUT2} can ramp up and reach regulation with the same rate, or a little bit faster or slower than V_{OUT1}. Note that V_{OUT2} is tracking V_{OUT1} and reaches regulation first. Equations 14 and 15 can be used to calculate the tracking resistors. ΔV is the desired V_{OUT1} - V_{OUT2} difference when V_{OUT2} reaches regulation. ΔV will be positive when V_{OUT1} change rate is higher than V_{OUT2} startup rate. It will be negative if V_{OUT2} rate is faster. With simultaneous sequencing, ΔV is zero. To assure the proper device operation, make sure that the selected R_1 is larger than the value given in Equation 17.

$$R_1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSOFFSET}}{I_{SS}} \quad (14)$$

$$R_2 = \frac{V_{REF} \times R_1}{V_{OUT2} + \Delta V - V_{REF}} \quad (15)$$

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (16)$$

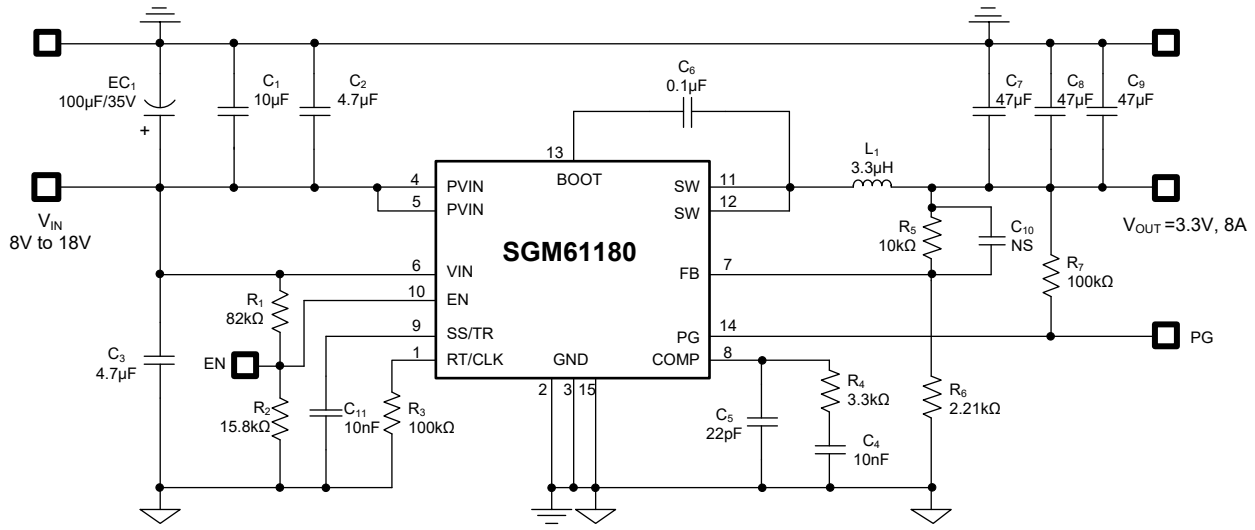
$$R_1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (17)$$

The $V_{SSOFFSET}$ is the inherent SS/TR to FB offset of the device (37mV TYP) and I_{SS} is the pull-up current source (2μA).

APPLICATION INFORMATION

Typical Application

The schematic of a typical application circuit that is used for SGM61180 evaluation module is given in Figure 13.



Note: EC_1 is optional. If VIN pin is more than 200mm far from the PVIN of SGM61180, or the VIN pin is not connected with the PVIN of SGM61180, or the input voltage is on/off by air-break switch, EC_1 should be installed. Otherwise, the spike voltage over 20V at the input side is caused, which will damage SGM61180.

Figure 13. SGM61180 Typical Application Circuit

Design Requirements

In this example, a high frequency regulator with ceramic output capacitors will be designed using SGM61180 and the details will be reviewed. The design requirements are typically determined at the system level. In this example, the known parameters are summarized in Table 1.

Table 1. Design Parameters

Design Parameter	Example Value
Output Voltage	3.3V
Maximum Output Current	8A
Transient Response to 4A Load Step	ΔV_{OUT} = 7%
Input Voltage Range	12V nominal, 8V to 18V
Maximum Output Voltage Ripple	$33mV_{P-P}$
Input Turn-On Voltage (V_{IN} Rising)	7.408V
Input Turn-Off Voltage (V_{IN} Falling)	6.914V
Switching Frequency (f_{SW})	480kHz

Operating Frequency

Usually the first parameter to design is the switching frequency (f_{SW}). Higher switching frequencies allow smaller solution size and smaller filter inductors and capacitors and the bandwidth of the converter can be increased for faster response. It is also easier to filter noises because they also shift to higher frequencies. The drawbacks are increased switching and gate driving losses that result in lower efficiency and tighter thermal limits. Also the duty cycle range and step-down ratio will be limited due to the minimum on-time and/or off-time limits of the converter. In this design, f_{SW} = 480kHz is chosen as a tradeoff. From Equation 13 the nearest standard resistor for this frequency is R_3 = 100kΩ.

APPLICATION INFORMATION (continued)

Inductor Design

Equation 18 is conventionally used to calculate the output inductance of a step-down converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 10% to 30% ripple is selected (K_{IND} = 0.1 ~ 0.3). Choosing a higher K_{IND} value reduces the selected inductance.

$$L_1 = \frac{V_{INMAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (18)$$

In this example, K_{IND} = 0.3 is chosen and the inductance is calculated to be 2.31μH. A larger standard value was chosen as 3.3μH. The ripple, RMS and peak inductors current calculations are summarized in Equations 19, 20 and 21 respectively.

$$I_{RIPPLE} = \frac{V_{INMAX} - V_{OUT}}{L_1} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (19)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left[\frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times L_1 \times f_{SW}} \right]^2} \quad (20)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (21)$$

For this example, the ripple, RMS, and peak inductor current are calculated as 1.68A, 8.02A and 8.84A respectively. A 3.3μH inductor from Vishay IHLP4040DZER3R3M1 series with 18.6A saturation and 10A RMS current ratings is selected for L_1.

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Output Capacitor Design

Three primary criteria must be considered for design of the output capacitor (C_{OUT}): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. Equation 22 can be used to calculate the minimum output capacitance that is needed to supply or absorb a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (22)$$

where:

- ΔI_{OUT} is the change in output current.
- f_{SW} is the regulator's switching frequency.
- ΔV_{OUT} is the allowable change in the output voltage.

APPLICATION INFORMATION (continued)

For example, if the acceptable transient to a 4A load step is 7%, by inserting ΔV_{OUT} = 0.07 × 3.3V = 0.231V and ΔI_{OUT} = 4.0A, the minimum required capacitance will be 72.2μF. Note that the impact of output capacitor ESR on the transient is not taken into account in Equation 22. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient.

Equation 23 can be used for the output ripple criteria and finding the minimum output capacitance needed. $V_{ORIPPLE}$ is the maximum acceptable ripple. In this example, the allowed ripple is 33mV that results in minimum capacitance of 14.6μF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{RIPPLE}}} \quad (23)$$

where:

• $V_{ORIPPLE}$ is the maximum allowable output voltage ripple.

• I_{RIPPLE} is the inductor ripple current.

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 23. Use Equation 24 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement. In this example, the ESR must be less than 33mV/1.68A = 19.6mΩ.

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} \quad (24)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a 3 × 47μF/10V X5R ceramic capacitor with 3mΩ of ESR is used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 25 calculates the RMS current that the output capacitor must support. In this example, it is 485mA.

$$I_{CORMS} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{\sqrt{12} \times V_{INMAX} \times L_1 \times f_{SW}} \quad (25)$$

Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61180. At least 4.7μF of effective capacitance (after deratings) is needed on the PVIN input and similar amount is also needed for the V_{IN} pin. In some applications additional bulk capacitance may also be required for the PVIN input. The PVIN capacitor ripple current rating must also be greater than the maximum input current ripple. The input ripple current can be calculated from Equation 26. For this example, the input ripple RMS current is 3.94A.

$$I_{CIRMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{INMIN} - V_{OUT})}{V_{INMIN} \times V_{INMIN}}} \quad (26)$$

For this design, a ceramic capacitor with at least 25V voltage rating is required to support the maximum input voltage. So, one 10μF and one 4.7μF 25V capacitors in parallel are selected for VIN. They are placed in parallel because the VIN and PVIN inputs are tied together to operate from a single supply in this design.

The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 27. In this example, the input voltage ripple is 417mV.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times 0.25}{C_{IN} \times f_{SW}} \quad (27)$$

Soft-Start Capacitor

The soft-start capacitor programs the ramp-up time of the output voltage during power-up. The ramp is needed in many applications due to limited voltage slew rate required by the load or limited available input current to avoid input voltage sag during startup (UVLO) or to avoid over-current protection that can occur during output capacitor charging. Soft-start will solve all these issues by limiting the output voltage slew rate.

Equation 28 (with I_{SS} = 2μA and V_{REF} = 0.6V) can be used to calculate the soft-start capacitor for a required soft-start time (t_{SS}). In this example, the output capacitor value is relatively small (47μF) and the soft-start time is not critical because it does not require too much charge for 3.3V output voltage. However, it is better to set a small arbitrary value, like C_{SS} = 10nF that results in 3ms startup time.

$$C_{SS}\ (nF) = \frac{t_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V)} \quad (28)$$

APPLICATION INFORMATION (continued)

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor with 10V or higher voltage rating must be connected between the BOOT-SW pin. X5R or better dielectric types are recommended.

UVLO Setting

The under-voltage lockout (UVLO) can be programmed from VIN or PVIN by an external voltage divider network. In this design R_1 is connected between VIN and the EN pin and R_2 is connected between EN and GND (see Figure 5). The UVLO has two thresholds (Hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down or brownout (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when VIN rises above 7.408V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below 6.914V (UVLO falling threshold). Equations 2 and 3 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 82kΩ and R_2 = 15.8kΩ.

Feedback Resistors

The feedback resistor divider (see Figure 13, R_5 and R_6) is used to set the output voltage. Choosing a 10kΩ value for the upper resistor (R_5), the lower resistor (R_6) can be calculated from Equation 29. The nearest 1% resistor for the calculated value (2.222kΩ) is 2.21kΩ. For higher output accuracy, choose resistors with better tolerance (0.5% or better).

$$R_6 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_5 \quad (29)$$

Minimum Output Voltage

There is a minimum output voltage limit for any given input voltage due to the limited minimum switching on-time of the device. Above the 0.6V minimum possible output, the lowest achievable voltage is given by Equation 30.

$$V_{OUTMIN} = t_{ONMIN} \times f_{SWMAX} (V_{INMAX} + I_{OUTMIN} (R_{DSHMIN} - R_{DSLMIN})) - I_{OUTMIN} (R_L + R_{DSHMIN}) \quad (30)$$

where:

- V_{OUTMIN} = Minimum achievable output voltage.
- t_{ONMIN} = Minimum controllable on-time (135ns MAX).
- f_{SWMAX} = Maximum f_{SW} (including tolerance).
- V_{INMAX} = Maximum input voltage.
- I_{OUTMIN} = Minimum load current.
- R_{DSHMIN} = Minimum high-side switch R_{DSON} (24mΩ to 27mΩ TYP).
- R_{DSLMIN} = Minimum low-side switch R_{DSON} (16mΩ TYP).
- R_L = Output Inductor series resistance.

Loop Compensation Design

Several techniques are used by engineers to compensate a DC/DC regulator. The method presented here uses simple calculations and generally results in high phase margins. In most conditions, the phase margin will be between 60 and 90 degrees. In this method the effects of the slope compensation are ignored. Because of this approximation, the actual cross over frequency is usually lower than the calculated value.

First, the converter pole (f_P) and ESR-zero (f_Z) are calculated from Equations 31 and 32. For C_{OUT}, the worst derated value of 78.96μF should be used. Equations 33 and 34 can be used to find an estimation for closed-loop crossover frequency (f_{CO}) as a starting point (choose the lower value).

$$f_P = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (31)$$

$$f_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (32)$$

$$f_{CO} = \sqrt{f_P \times f_Z} \quad (33)$$

$$f_{CO} = \sqrt{f_P \times \frac{f_{SW}}{2}} \quad (34)$$

For this design, f_P = 4.89kHz and f_Z = 2.01MHz. Equation 33 yields 31.4kHz for crossover frequency and Equation 34 gives 34.3kHz. The lower value is 31.4kHz, but a slightly higher frequency of 34.3kHz will be chosen as the intended crossover frequency.

Having the crossover frequency, the compensation network (R_4 and C_4) can be calculated. R_4 sets the gain of the compensated network at the crossover frequency and can be calculated by Equation 35.

$$R_4 = \frac{2\pi \times f_{CO} \times V_{OUT} \times C_{OUT}}{gm_{EA} \times V_{REF} \times gm_{PS}} \quad (35)$$

APPLICATION INFORMATION (continued)

C_4 sets the location of the compensation zero along with R_4. To place this zero on the converter pole, use Equation 36.

$$C_4 = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_4} \quad (36)$$

From Equations 35 and 36 the standard selected values are R_4 = 3.3kΩ and C_4 = 10nF.

A high frequency pole can also be added by a parallel capacitor if needed (not used in this example). The pole frequency can be calculated from Equation 37.

$$f_P = \frac{1}{2\pi \times R_4 \times C_5} \quad (37)$$

Layout Guidelines

• Layout is a critical portion of good power supply design. See Figure 14 for a PCB layout example.

• The top layer contains the main power traces for VIN, VOUT, and FB. Also, on the top layer are connections for the remaining pins of the SGM61180 and a large top-side area filled with ground.

• The top layer ground area must be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the SGM61180 device to provide a thermal path from the exposed thermal pad land to ground.

• The GND pin must be tied directly to the power pad under the IC and the power pad.

• For operation at full rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipating area.

• There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

• To help eliminate these problems, the PVIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.

• Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.

• The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

• Make sure to connect this capacitor to the quite analog ground trace rather than the power ground trace of the PVIN bypass capacitor.

• Since the SW connection is the switching node, the output inductor must be placed close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

• The output filter capacitor ground must use the same power ground trace as the PVIN input bypass capacitor.

• Try to minimize this conductor length while maintaining adequate width.

• The small signal components must be grounded to the analog ground path as shown.

• All sensitive analog traces and components such as FB, RT/CLK and COMP must be placed away from high-voltage switching nodes such as SW, BOOT and the output inductor to avoid noise coupling.

• The output voltage sense trace must be connected to the positive terminal of one output capacitor in the design with the best high frequency characteristics. The output voltage will be most tightly regulated at the voltage sense point.

• The RT/CLK pin is sensitive to noise, so the RT resistor must be placed as close as possible to the IC and routed with minimal lengths of trace.

• The additional external components can be placed approximately as shown.

• It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

• Land pattern and stencil information is provided in the datasheet addendum.

• The dimension and outline information is for the standard TQFN-3.5×3.5-14L package.

APPLICATION INFORMATION (continued)

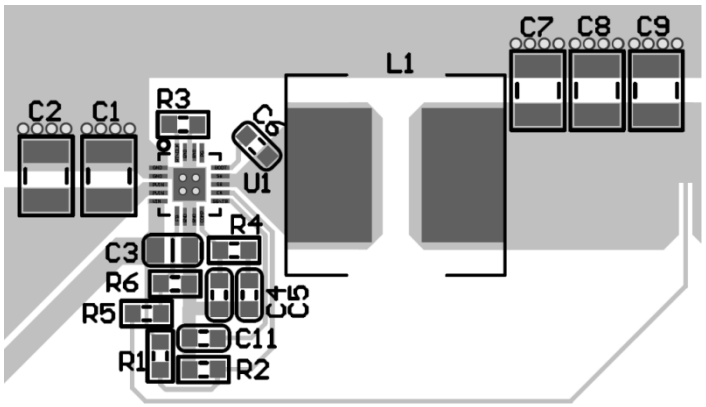
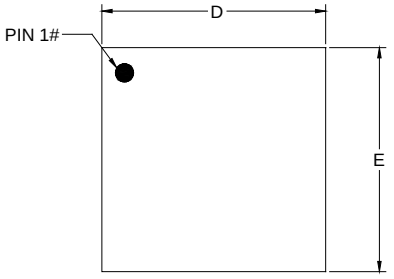


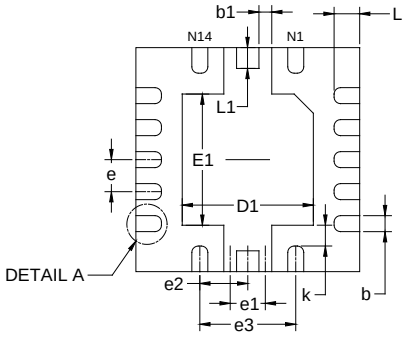
Figure 14. PCB Layout

PACKAGE OUTLINE DIMENSIONS

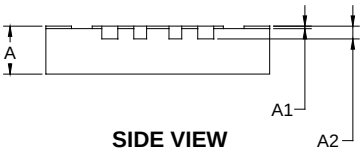
TQFN-3.5×3.5-14L



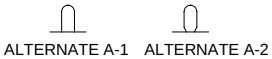
TOP VIEW



BOTTOM VIEW

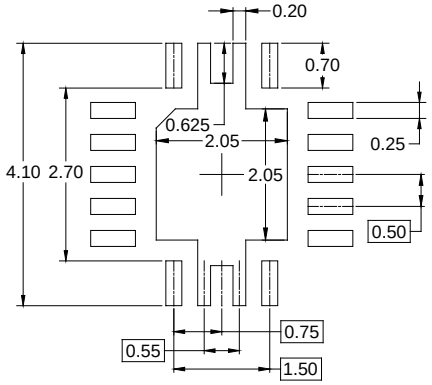


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



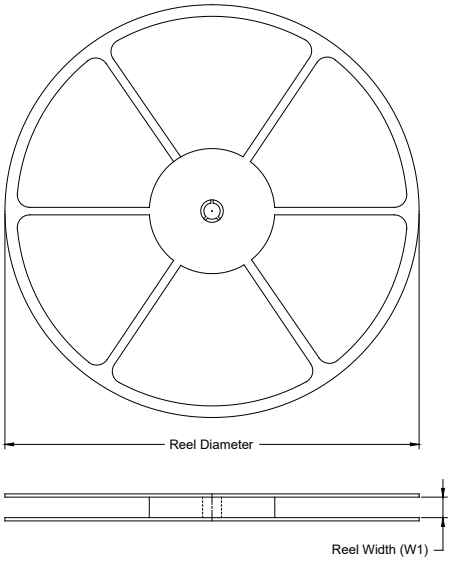
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.200 REF		
D	3.400	3.500	3.600
E	3.400	3.500	3.600
D1	1.950	2.050	2.150
E1	1.950	2.050	2.150
b	0.200	0.250	0.300
b1	0.150	0.200	0.250
e	0.500 BSC		
e1	0.550 BSC		
e2	0.750 BSC		
e3	1.500 BSC		
k	0.220	0.320	0.420
L	0.300	0.400	0.500
L1	0.225	0.325	0.425

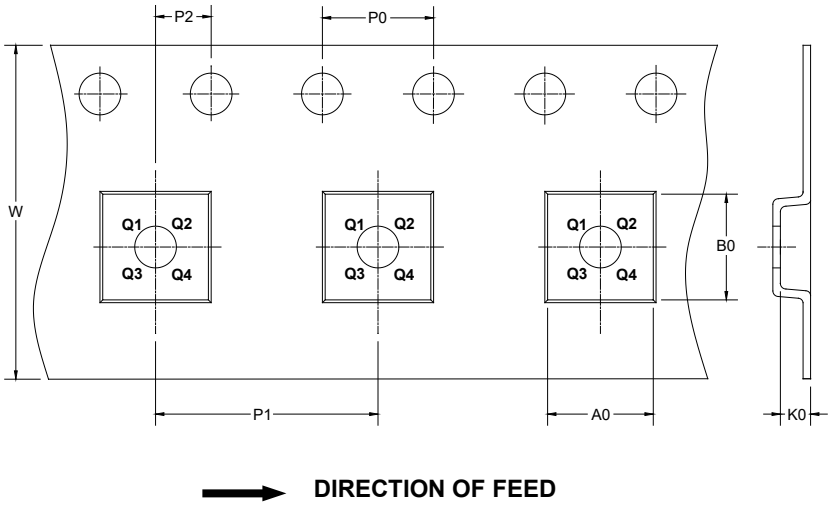
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

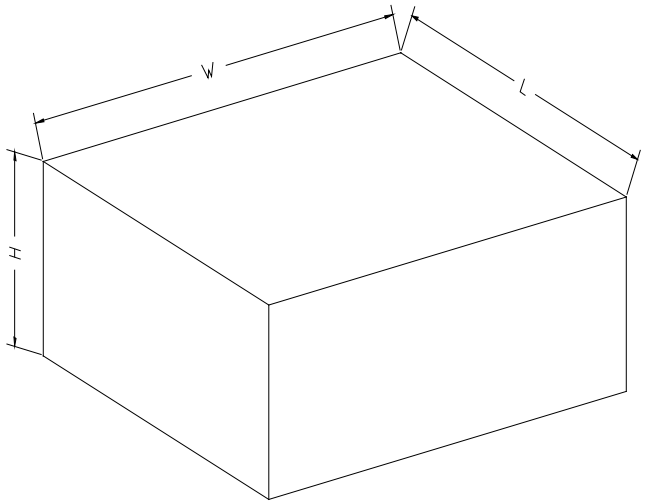
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-14L	13″	12.4	3.75	3.75	1.05	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002