Sink/Source DDR Termination Regulator

DESCRIPTION

The EUP7998 is a high performance linear regulator designed to provide power for termination of a DDR memory bus. It significantly reduces parts count, board space and overall system cost over previous switching solutions.

The EUP7998 maintains a fast transient response using only 20µF or 30µF output capacitance. The EUP7998 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3 and Low Power DDR3/DDR4 VTT bus termination.

The EUP7998 provides current and thermal limits to prevent damage to the linear regulator. Additionally, The EUP7998 generates an open-drain PGOOD signal to monitor the output regulation. An active high enable pin EN can pull VTT low, but REFOUT will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

The EUP7998 is available in the 3mm × 3mm TDFN-10 and SOP-8 (EP) packages.

FEATURES

- VLDOIN Input Voltage Range: 1.1V to 3.5V
- VIN Input Voltage Range: 2.375V to 5.5V
- Typically 3×10µF MLCCs stable for DDR
- Fast Load-Transient Response
- ±10mA Buffered Reference (REFOUT)
- Meet DDR, DDR2 JEDEC Specifications. Supports DDR3 and Low-Power DDR3/DDR4 VTT Applications
- Power-Good Window Comparator
- With Soft Start, UVLO and OCP
- Thermal Shutdown
- Available in 10-Pin 3mm×3mm TDFN and SOP-8 (EP) packages
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Notebook/Desktop/Server
- DDR Memory Termination
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

Typical Application Circuit

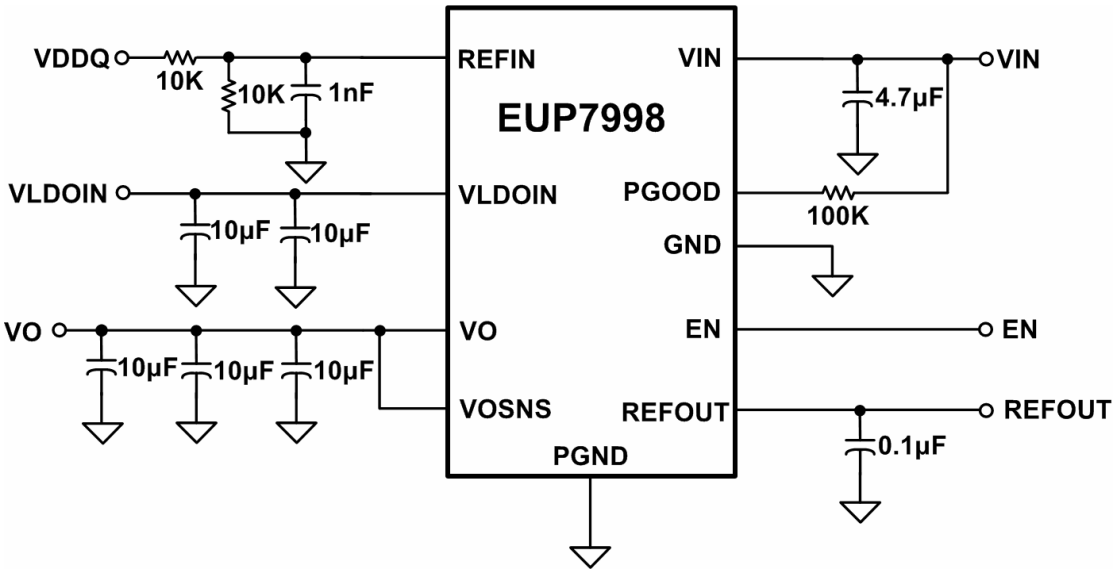


Figure 1. For TDFN-10 package

Typical Application Circuit (continued)

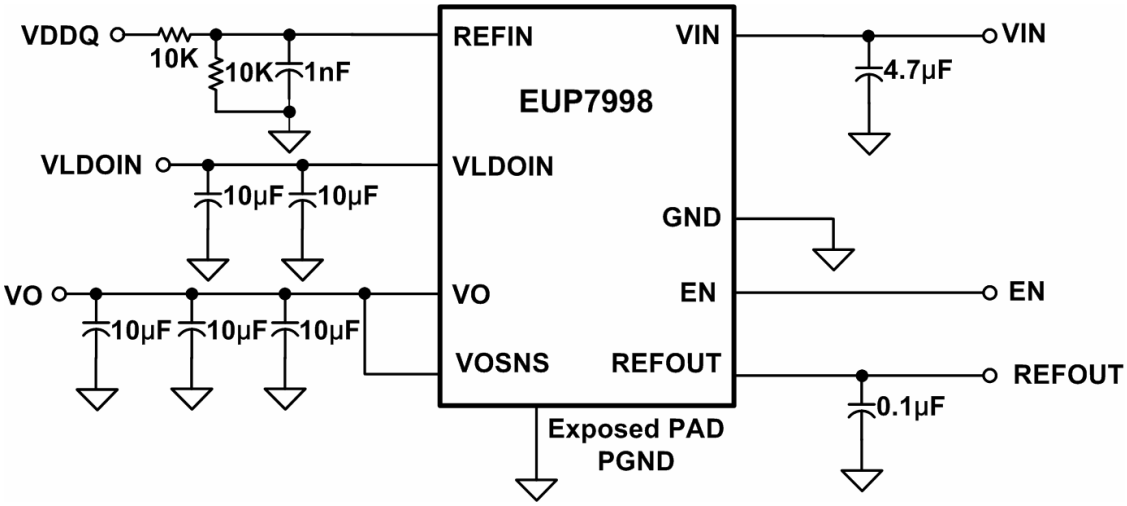
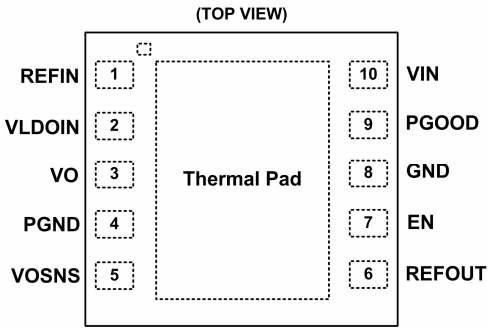
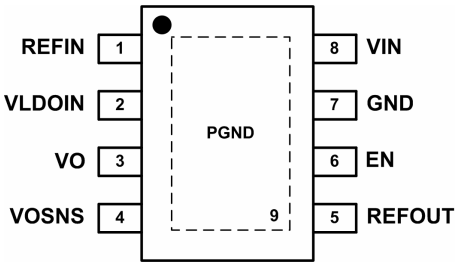


Figure 2. For SOP-8(EP) package

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
TDFN-10		SOP-8 (EP)	

Pin Description

PIN	TDFN-10	SOP-8 (EP)	DESCRIPTION
REFIN	1	1	External Reference Input
VLDOIN	2	2	Power Supply of the LDO. Internally connected to the output source MOSFET.
VO	3	3	Output of the LDO
PGND	4	9 (Thermal pad)	Power Ground
VOSNS	5	4	Voltage sense input for the LDO. Connect to positive terminal of the output capacitor.
REFOUT	6	5	Buffered Reference Output. The output of the unity-gain reference input buffer sources and sinks over 10mA. Bypass REFOUT to GND with a 0.1µF ceramic capacitor.
EN	7	6	Enable Control Input. Active High Input. For DDR VTT application, connect EN to SLP_S3.
GND	8	7	Ground
PGOOD	9	-	Open-Drain Power-Good Output
VIN	10	8	Power Supply Input. Connect to the system supply voltage. Bypass VIN to GND with a 1µF or 4.7µF ceramic capacitor.

Note(1):PGND, GND and thermal pad must be connected together outside under thermal pad.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP7998JIR1	TDFN-10	xxxxx P7998	-40 °C to +85°C
EUP7998DIR1	SOP-8 (EP)	xxxxx P7998	-40 °C to +85°C

EUP7998 □ □ □ □

Lead Free Code

1: Lead Free, Halogen Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TDFN
D: SOP (EP)

Block Diagram

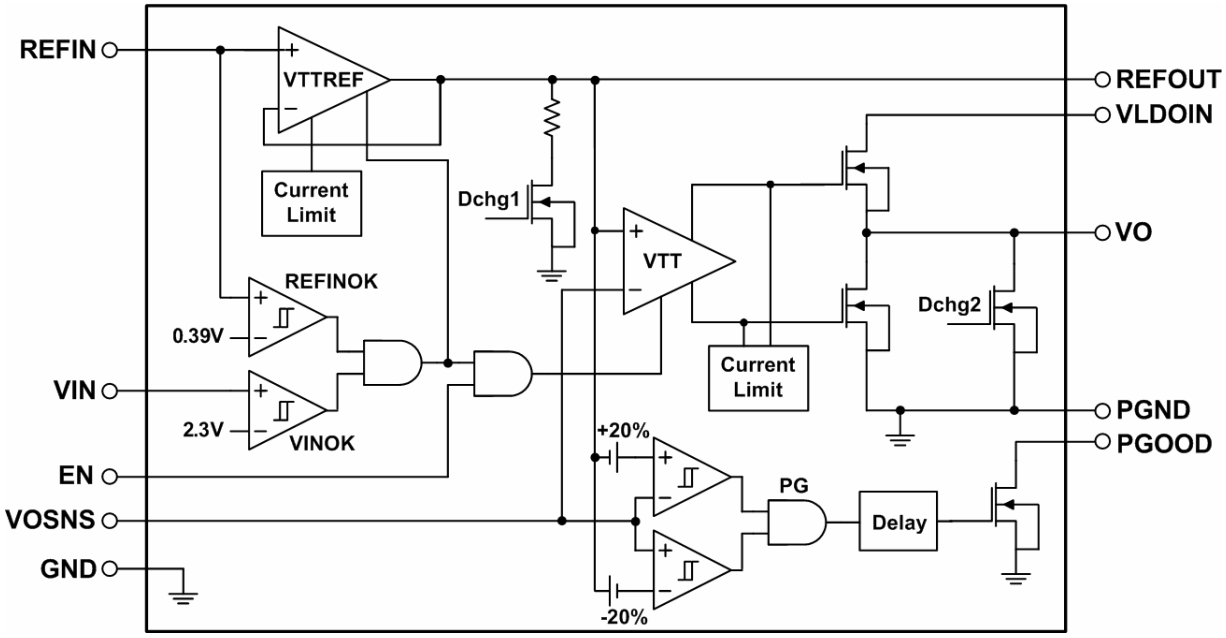


Figure3. Block Diagram

Absolute Maximum Ratings (1)

- Supply Input Voltage---------- 6V
- Power Dissipation, PD @ T_A=25°C TDFN-10---------- 1.45W
- Package Thermal Resistance TDFN-10,θ_{JA} ---------- 69°C /W
- Package Thermal Resistance SOP-8 (EP),θ_{JA} ---------- 60°C /W
- Lead Temperature (Soldering,10sec) ---------- 260°C
- Storage Temperature Range---------- -65°C to +150°C
- ESD Rating Human Body Model ----------±2kV

Recommended Operating Conditions (2)

- Supply Input Voltage ----------2.5V to 5.5V
- Enable Input Voltage ----------0V to 5.5V
- Junction Temperature Range---------- -40°C to 125°C

Note(1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note(2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

V_{VIN}=3.3V, V_{VLDOIN}=1.8V, V_{REFIN}=0.9V, V_{VOSNS}=0.9V, V_{EN}= V_{VIN}, C_{OUT}=3×10µF, T_A=-40°C to 85°C.
Unless otherwise noted.

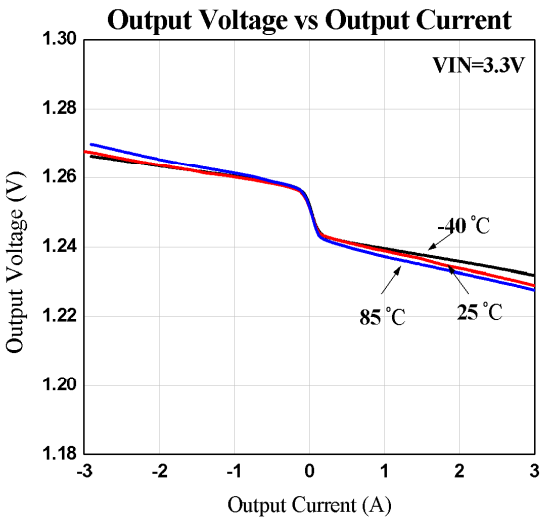
Symbol	Parameter	Conditions	EUP7998			Unit
			Min.	Typ.	Max.	
I_{VIN}	Quiescent Current	V_{EN}=3.3V, No Load, T_A=25°C		0.62	1	mA
I_{VINSD}	Shutdown Current	V_{EN}=0V,V_{REFIN}=0V, No Load, T_A=25°C		35	70	µA
		V_{EN}=0V,V_{REFIN}>0.4V, No Load, T_A=25°C		220	400	
I_{VLDOIN}	Supply current of VLDOIN	V_{EN}=3.3V, No Load, T_A=25°C		1	50	µA
$I_{VLDOINSD}$	Shutdown current of VLDOIN	V_{EN}=0V, No Load, T_A=25°C		0.1	50	µA
I_{REFIN}	Input current, REFIN	V_{EN}=3.3V			1	µA
V_{VOSNS}	Output DC voltage ,VO	V_{REFOUT}=1.25V (DDR1),I_O=0A		1.25		V
			-15		15	mV
		V_{REFOUT}=0.9V (DDR2),I_O=0A		0.9		V
			-15		15	mV
		V_{REFOUT}=0.75V (DDR3),I_O=0A		0.75		V
			-15		15	mV
ΔV_{VO}	Output Voltage Tolerance	-2A<I_{OUT}<2A	-25		25	mV
I_{VOSRCL}	VO Source Current Limit	V_{VOSNS}=90%×V_{REFOUT}	3		5	A
I_{VOSNCL}	VO Sink Current Limit	V_{VOSNS}=110%×V_{REFOUT}	3.5		5.5	A
$I_{DISCHARGE}$	Discharge Current VO	V_{REFIN}=0V, V_{VO}=0.3V, V_{EN}=0V, T_A=25°C		15	25	Ω
$V_{TH(PG)}$	PGOOD Threshold	Lower Threshold	-23.5	-20	-17.5	%
		High Threshold	17.5	20	23.5	
		Hysteresis		5		
$T_{PGSTUPDLY}$	PGOOD Startup Delay	Startup Rising edge, VOSNS within 15% of REFOUT		2		ms
T_{PGOODL}	Output Low Voltage	I_{SINK}=4mA			0.4	V
$T_{PGBADDLY}$	PGOOD Bad Delay	VOSNS is outside of the ±20% PGOOD Window		10		µs

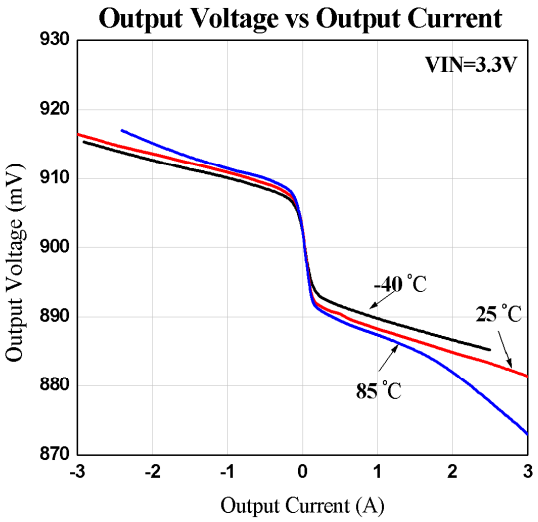
Electrical Characteristics (continued)

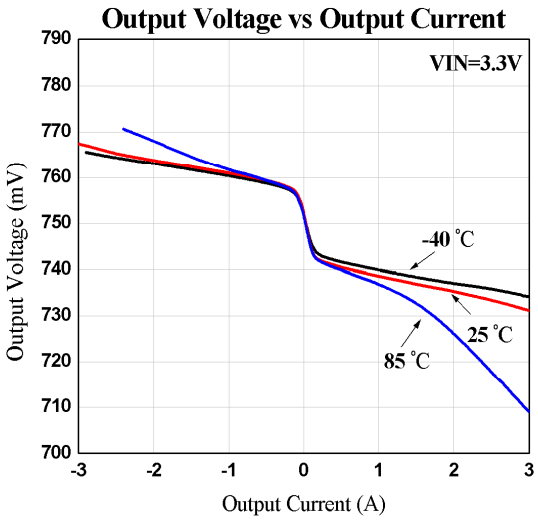
V_{VIN}=3.3V, V_{VLDOIN}=1.8V, V_{REFIN}=0.9V, V_{VOSNS}=0.9V, V_{EN}= V_{VIN}, C_{OUT}=3×10μF, T_A=-40°C to 85°C. Unless otherwise noted.

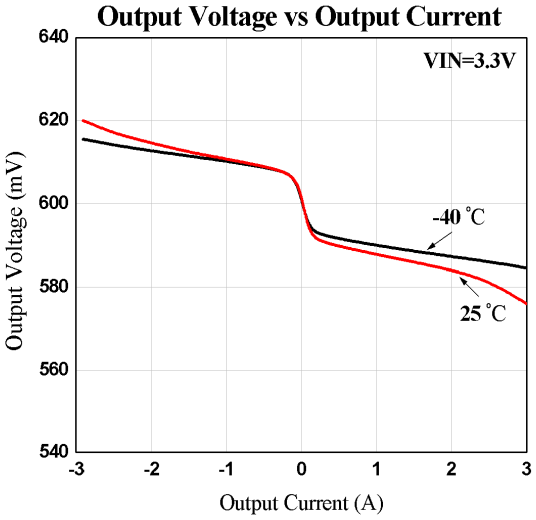
Symbol	Parameter	Conditions	EUP7998			Unit
			Min.	Typ.	Max.	
$T_{PGOODLK}$	Leakage current	V_{VOSNS}=V_{REFIN}, PGOOD=V_{VIN}+0.2V			1	μA
V_{REFIN}	REFIN Voltage Range		0.5		1.8	V
$V_{REFINUV}$	REFIN UVLO	REFIN Rising	360	390	420	mV
$\Delta V_{REFINUV}$	REFIN UVLO Hysteresis			20		mV
V_{REFOUT}	REFOUT Voltage		REFIN			V
$V_{REFOUTTOL}$	REFOUT Voltage Tolerance to REFIN	-10mA<I_{REFOUT} <+10mA, V_{REFIN}=1.25V	-15		15	mV
		-10mA<I_{REFOUT} <+10mA, V_{REFIN}=0.9V	-15		15	mV
		-10mA<I_{REFOUT} <+10mA, V_{REFIN}=0.75V	-15		15	mV
		-10mA<I_{REFOUT} <+10mA, V_{REFIN}=0.6V	-15		15	mV
$I_{REFOUTSRCL}$	REFOUT Source Current Limit	V_{REFOUT}=90%×V_{REFIN}	10	60		mA
$I_{REFOUTSNCL}$	REFOUT Sink Current Limit	V_{REFOUT}=110%×V_{REFIN}	10	60		mA
$V_{VINUVLO}$	VIN UVLO Threshold	Wake up, T_A=25°C	2.2	2.3	2.375	V
$\Delta V_{VINUVLO}$	VIN UVLO Hysteresis			50		mV
V_{ENH}	High-level Input Voltage		1.7			V
V_{ENIL}	Low-level Input Voltage				0.3	V
ΔV_{EN}	Enable Level Hysteresis			0.5		V
I_{ENLEAK}	Logic Input leakage Current	EN=VIN or GND, T_A=25°C	-1		1	μA
T_{SD}	Thermal Shutdown Temperature			165		°C
ΔT_{SD}	Thermal Shutdown Hysteresis			25		°C

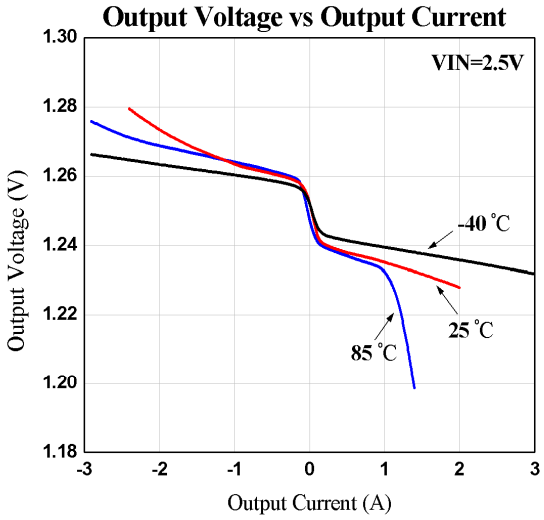
Typical Operating Characteristics

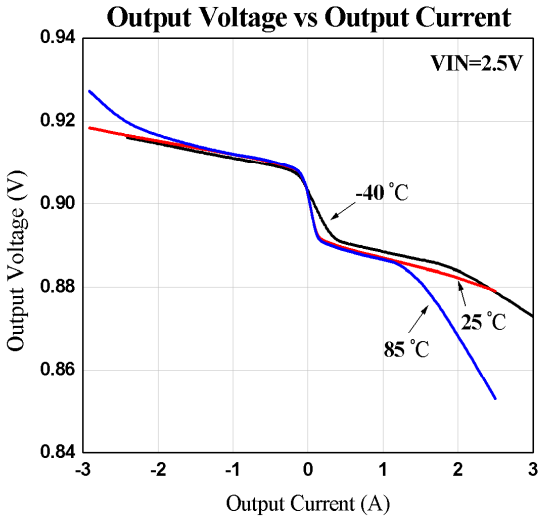




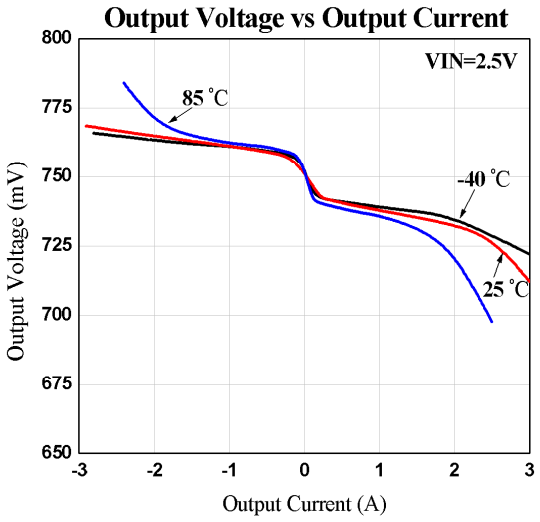


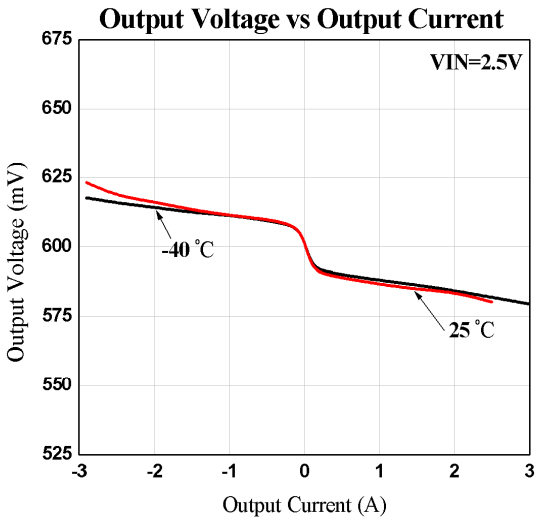


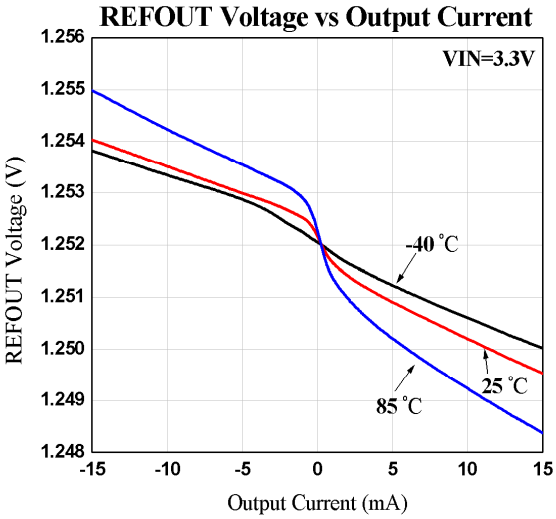


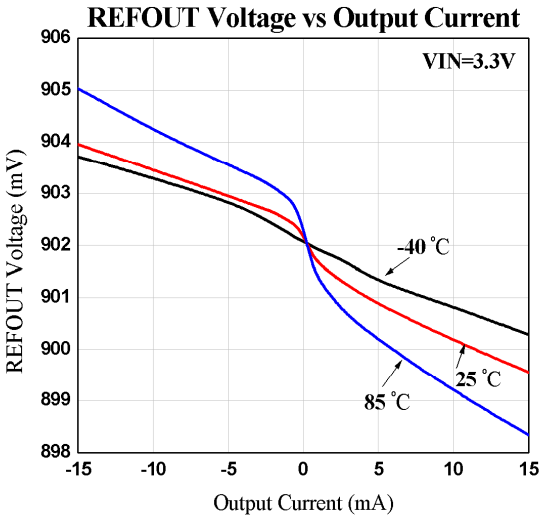


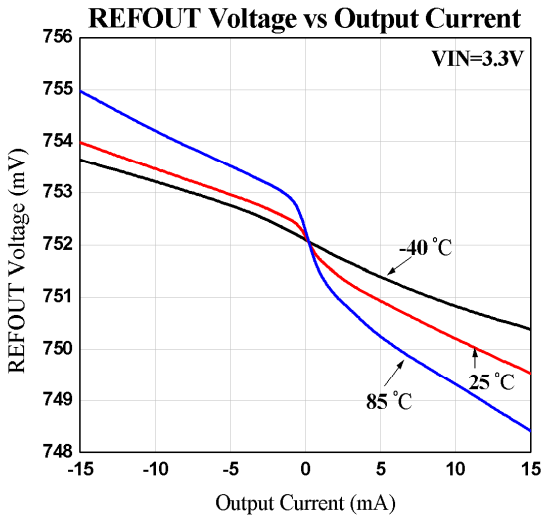
Typical Operating Characteristics (continued)

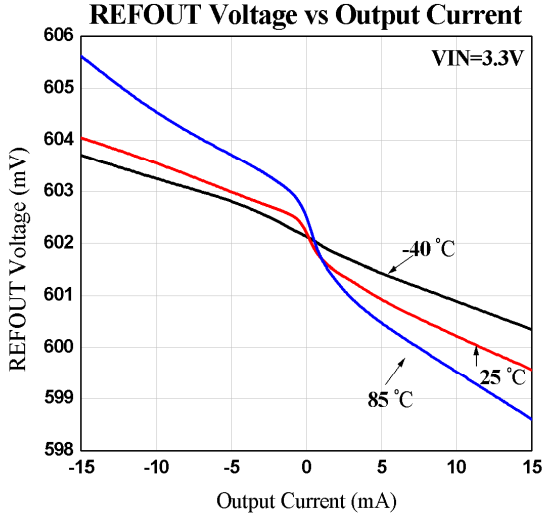












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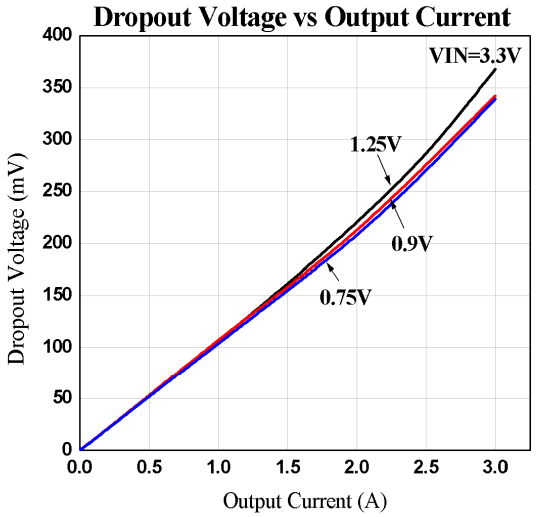
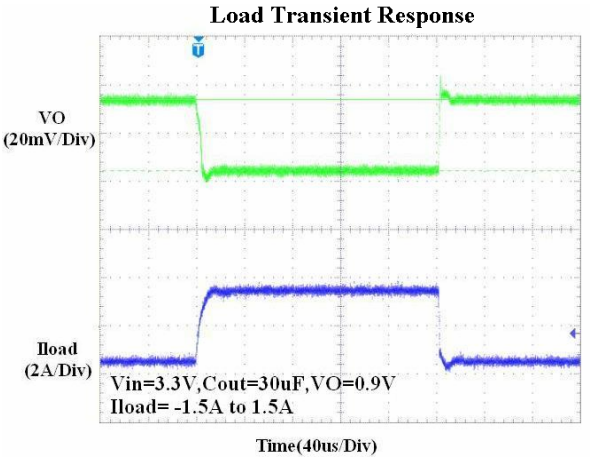




Detailed Description

The EUP7998 is a low-voltage, low-dropout DDR termination linear regulator with an external bias supply input and a buffered reference output. The VIN drives the gate of the internal pass transistor, while a lower voltage input at the drain of the transistor is regulated to provide VO. By using separate bias and power inputs, the EUP7998 can drive an n-channel high-side MOSFET and use a lower input voltage to provide better efficiency.

The EUP7998 regulates its output voltage to the voltage at REFIN. When used in DDR applications as a termination supply, the EUP7998 delivers 1.25V/0.9V/ 0.75V/0.6V at 2A peak (typ) from an input voltage of 1.1V to 3.6V. The EUP7998 sinks up to 2A peak (typ) as required in a termination supply. The EUP7998 provides shoot-through protection, ensuring that the source and sink MOSFETs do not conduct at the same time, yet produces a fast source-to-sink load transient.

VIN Input Supply

The VIN input powers the control circuitry and provides the gate drive to the pass transistors. This improves efficiency by allowing VLDOIN to be powered from a lower supply voltage. Bypass VIN with a 1uF or greater ceramic capacitor as close to the device as possible.

VIN Undervoltage Lockout (UVLO)

The VIN input undervoltage-lockout (UVLO) circuitry ensures that the regulator starts up with adequate voltage for the gate-drive circuitry to bias the internal pass transistor. The UVLO threshold is 2.375V. VIN must remain above this level for proper operation.

Reference Input (REFIN)

The EUP7998 regulates VO to the voltage set at REFIN, making the EUP7998 ideal for memory applications where the termination supply must track the supply voltage. Typically, REFIN is set by an external resistive voltage-divider connected to the memory supply (VDDQ). The EUP7998 supports REFIN voltage from 0.5V to 1.8V, making it versatile and ideal for many types of low-power LDO applications.

Reference Output (REFOUT)

REFOUT is a unity-gain amplifier that generates the DDR reference supply. It sources and sinks greater than 10mA. The reference buffer is typically connected to ceramic bypass capacitors (0.1µF). REFOUT is active when VREFIN>0.39V and VIN is above VUVLO. REFOUT is independent of EN.

Enable (EN)

Drive EN low to disable the error amplifier, gate-drive circuitry, and pass transistor. VO is discharged to PGND through an internal 15Ω MOSFET. When EN is driven high, the EUP7998 VO regulator begins normal operation.

Soft-Start

Soft-start gradually increases the internal source current limit to reduce input surge currents at startup. When VO is outside of the PGOOD window, the current limit level is one-half of the full over current limit (OCL) level. When VO rises or falls within the PGOOD window, the current limit level switches to the full OCL level.

Power-Good (PGOOD)

The EUP7998 provides an open-drain PGOOD output that goes high 2ms (typ) after the VO reaches ±20% of REFOUT. PGOOD goes low within 10µs when the output goes out of the size of the power-good window. Connect a pull-up resistor from PGOOD to VIN for a logic-level output. Use a 100k resistor to minimize current consumption.

Thermal Shutdown

Thermal-overload protection prevents the linear regulator from overheating. When the junction temperature exceeds +165°C, the VTT and VTTREF regulators are shut off. The VO and REFOUT are both pull down to GND, allowing the device to cool. This shutdown is a non-latch protection.

Application Note

Input Capacitor

Bypass VLDOIN to PGND with a 10µF or greater ceramic capacitor. Provide more input capacitance as more output capacitance is used at VO. In general, use one-half of the C value for input.

Add a ceramic capacitor, with a value between 1µF and 4.7µF, placed close to the VIN pin, to stabilize the bias supply from any parasitic impedance from the supply.

Output Capacitor

For stable operation, the total capacitance of the VO output terminal must be greater than 20µF. The EUP7998 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. Three 10µF X7R ceramic capacitors are used in the typical application circuit. The output capacitor should be located near the VO pin as close as possible.

If the ESR of the output capacitor greater than 2mΩ, an RC filter should be placed between the output and the VOSNS for stability. The RC filter time constant should be almost the same as the time constant of the output capacitor and its ESR.

Power On/Off Sequence

The EUP7998 provides S3 support by an EN function. In the end application the EN pin could be connected to an SLP_S3 signal.

The EUP7998 also supports tracking startup and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device.

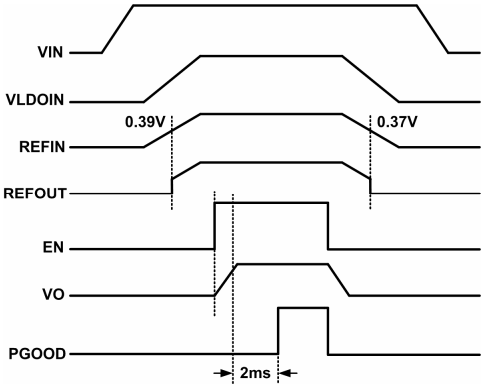


Figure4. Typical S3 and pseudo-S5 Support Timing Diagram

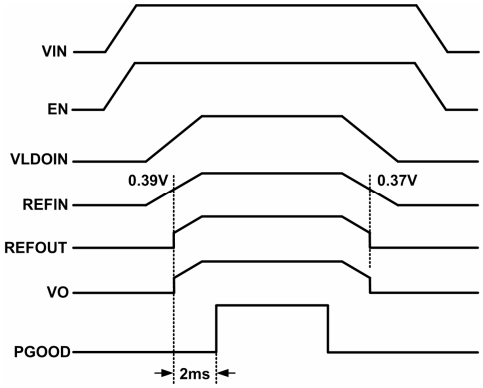


Figure5. Typical Start Up and Shutdown Timing Diagram

Power Dissipation

The maximum power dissipation of the EUP7998 depends on the thermal resistance of the 10-pin TDFN package and the circuit board, the temperature difference between the die and ambient air. For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation is:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, θ_{JA} is the thermal resistance from the case through the PC board, copper traces, and other materials to the surrounding air.

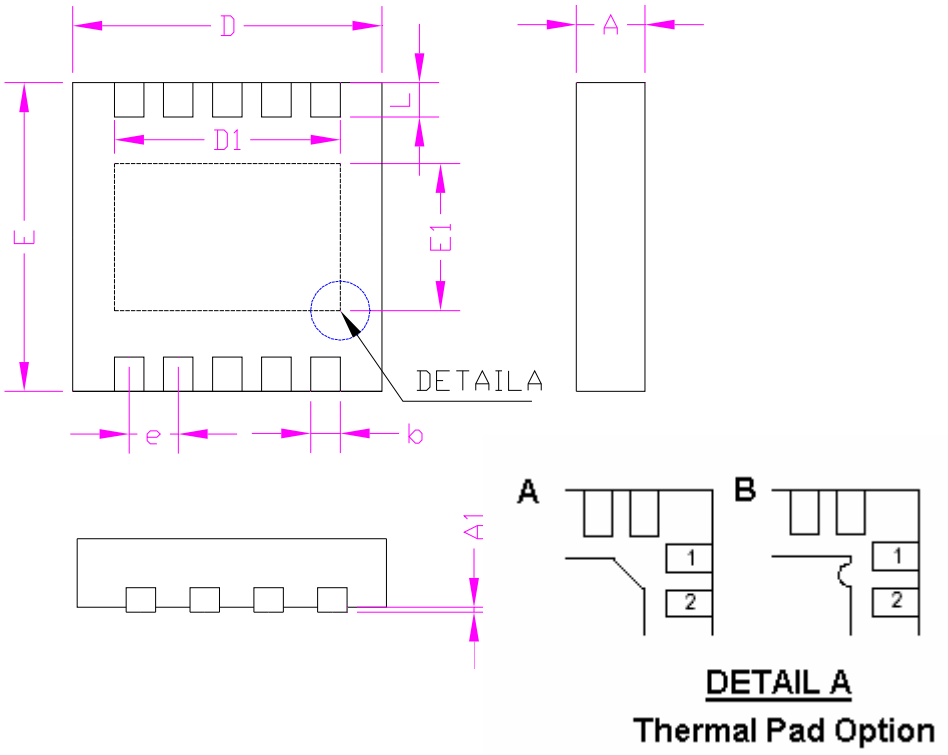
PCB Layout Considerations

For a good performance, consider the following points of EUP7998 PCB design.

1) The input and output CAP must be placed as close as possible to the pin.
2) Minimize high-current ground loops.
3) In order to minimize the ESR between the GND and the output capacitors, VOSNS should be connected to the positive node of VO output capacitors.
4) Consider adding low-pass filter at VOSNS if the ESR of the VO Output capacitor is larger than 2mΩ.
5) The GND of REFOUT capacitor and the VO capacitors should be tied together.
6) Connect the backside pad to a large ground plane.

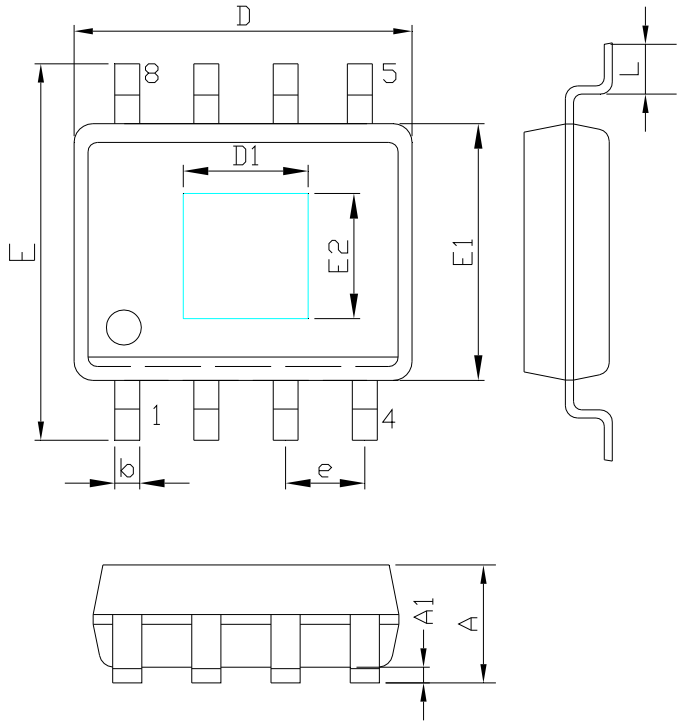
Packaging Information

TDFN-10



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
D1	2.50		0.098	
D	2.90	3.10	0.114	0.122
E1	1.70		0.067	
E	2.90	3.10	0.114	0.122
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012
e	0.50		0.020	
D1	2.40		0.094	

SOP-8 (EP)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E1	3.90		0.153	
D1	2.00		0.079	
E2	2.00		0.079	
E	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	