TFT LCD DC-DC Converter with Integrated Charge Pumps and OP-AMP

DESCRIPTION

The EUP2619 generates power supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in tablet PCs and notebooks operated from 2.5V to 5.5V input supply. The device integrates a step-up converter, positive and negative charge pumps, and a high speed V_{COM} buffer.

The external compensated step-up converter, providing the regulated supply voltage for the panel source driver ICs, features an internal power MOSFET and high frequency operation allowing to use small inductors and capacitors. The step up converter uses fixed-frequency peak current mode control architecture which provides fast load-transient response and easy compensation. A 2.8A peak current limit for the internal switch protects power supply fault condition.

The regulated positive and negative charge pump regulators generate the positive and negative supply rails for the TFT LCD gate resistive voltage-divider ICs.

The high speed V_{COM} buffer features 500mA short circuit current, 20MHz bandwidth, fast slew rate 45V/μs, and rail-to-rail inputs and outputs.

A built-in voltage detector generates a reset signal when the input voltage drops below 2.4V. The reset signal is active low and has a 120ms blanking time during power-on. The EUP2619 includes internal power-up sequencing, over/under voltage protections of the boost converter, and over temperature protection to ensure in safe operating.

The EUP2619 are available in a 16-pin 3mm×3mm TQFN package.

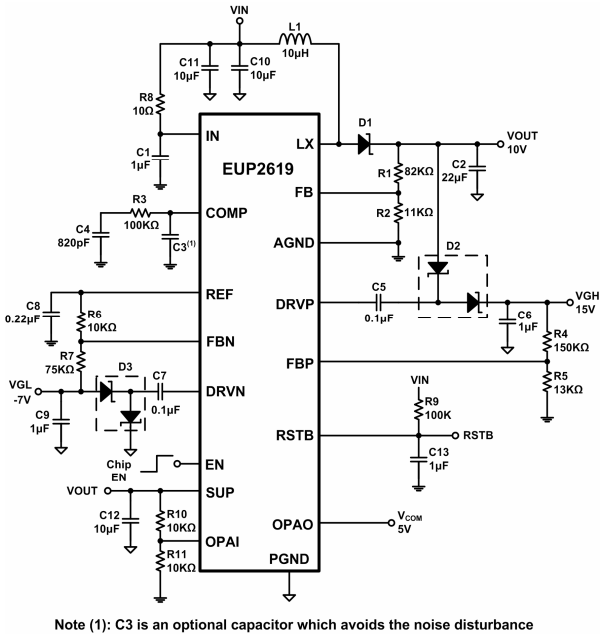
FEATURES

- 2.5V to 5.5V Input Supply Range
- 1.2MHz Current-Mode Step-Up Converter
  - Built-In 20V/2.8A, 0.16Ω N-Channel MOSFET
  - High Efficiency Up to 90%
  - ±1% Accurate Output Voltage
  - Fast Transient Response to Pulse Load
  - Over-Current Protection
  - Output Under-Voltage Protection
- 600kHz Negative Charge Pump Driver for VGL
- 600kHz Positive Charge Pump Driver for VGH
- High Speed High Current 18V V_{COM} Buffer
  - ±500mA Output Short-Circuit Current
  - 45V/μs Slew Rate
  - 20MHz, -3dB Bandwidth
  - Rail-to-Rail Input and Output
- Power-On Sequence Control
- Thermal-Overload Protection
- 3mm×3mm TQFN-16 Package
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

APPLICATIONS

- Tablet PCs
- Notebook Displays

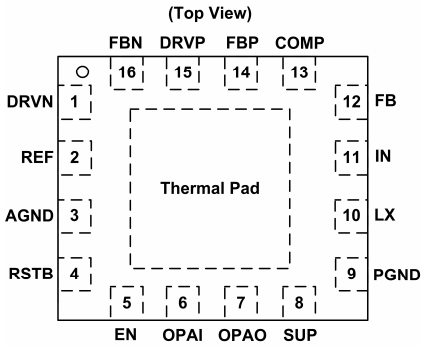
Typical Application Circuit



Note (1): C3 is an optional capacitor which avoids the noise disturbance

Figure 1.

Pin Configurations

Package Type	Pin Configurations
TQFN-16	

Pin Description

PIN	TQFN-16	DESCRIPTION
1	DRVN	Driver output pin of the negative charge pump.
2	REF	Reference bypass terminal. Bypass REF to AGND with a minimum of 0.22μF close to this pin.
3	AGND	Analog Ground.
4	RSTB	Voltage detector output for Reset. RSTB is an active-low open-drain output.
5	EN	Active-High Enable Control Input.
6	OPAI	VCOM buffer input pin. If OP function is not used, connect this pin to AGND.
7	OPAO	VCOM buffer output pin. If OP function is not used, make sure this pin floating.
8	SUP	VCOM buffer, V_{GH}, and V_{GL} charge pump power input. Positive supply rail for the operational amplifiers.
9	PGND	Power Ground.
10	LX	Switching pin. Drain of the internal power NMOS for the main step-up regulator.
11	IN	Supply Input.
12	FB	Main Boost Regulator Feedback Input. FB regulates to 1.2V nominal. Connect FB to the center of a resistive voltage-divider between the main output and the analog ground (AGND). Place the resistive voltage-divider close to the pin.
13	COMP	Compensation error amplifier pin.
14	FBP	Feedback pin of positive charge pump. Regulates to 1.2V nominal.
15	DRVP	Driver output pin of the positive charge pump.
16	FBN	Feedback pin of negative charge pump. Regulates to 0.24V nominal.
-	Thermal Pad	Exposed pad should be soldered to PCB board and connected to AGND.

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUP2619JIR1	TQFN-16	xxxxx P2619	2500	-40 °C to +105°C

EUP2619 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free
- Packing
  R: Tape & Reel
- Operating Temperature Range
  I: Industry Standard
- Package Type
  J : TQFN

Block Diagram

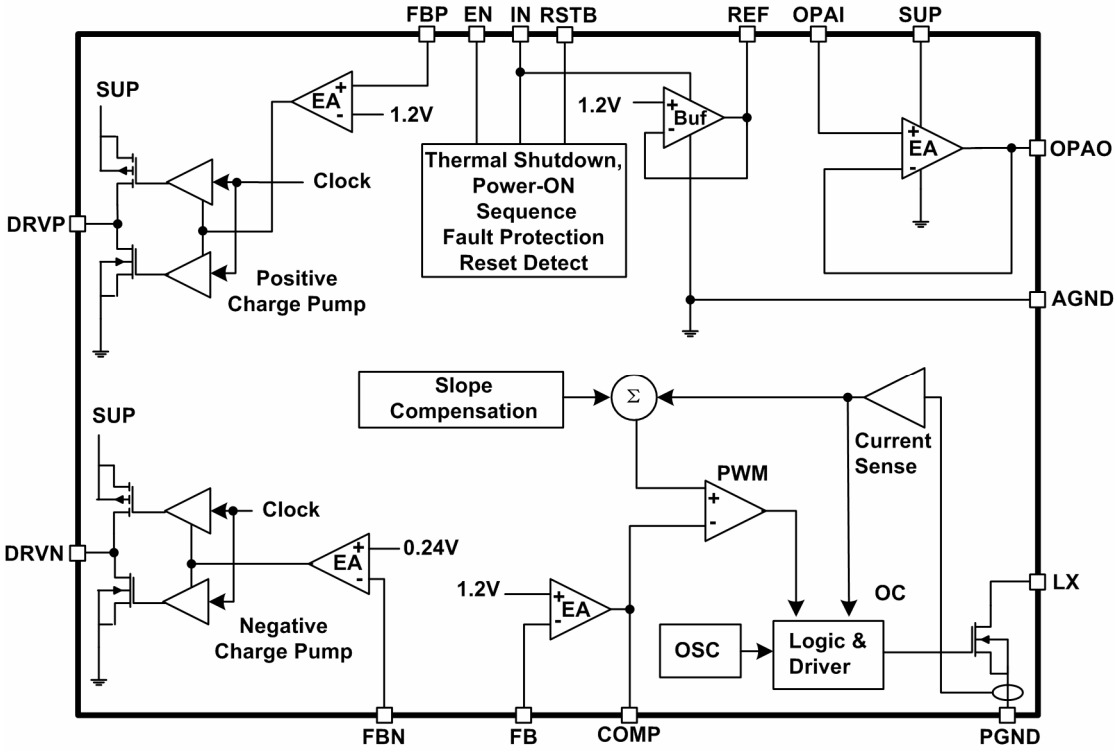


Figure 2.

Absolute Maximum Ratings (1)

- V_{IN} ---------- 6V
- IN to GND ---------- -0.3V to +6V
- LX to GND ---------- -0.3V to +20V
- PGND to GND ---------- -0.3V to -0.3V
- SUP to PGND ---------- -0.3V to +20V
- OPAI, OPAO to GND ---------- -0.3V to (SUP+0.3V)
- DRVP, DRVN to PGND ---------- -0.3V to (SUP+0.3V)
- REF, COMP, FB, FBN, FBP, EN, RSTB to GND ---------- -0.3V to (VIN+0.3V)
- Continuous Power Dissipation (T_A= +25°C) TQFN-16 ---------- 1.92W
- Junction Temperature ---------- +150°C
- Storage Temperature Range ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec) ---------- 260°C
- Thermal Resistance
  θ_{JA} (TQFN-16) ---------- 65°C/W
- ESD Susceptibility (HBM) ---------- 2kV

Recommend Operating Conditions (2)

- Supply Voltage (VIN) ---------- 2.5V to 5.5V
- Operating Temperature ---------- -40°C to +105°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

The ● denote the parameter apply over the full operating temperature range, otherwise the values are tested at T_A=+25 ºC. V_{IN}=3.3V, V_{OUT}=8.5V, unless otherwise noted.

Symbol	Parameter	Conditions		EUP2619			Unit
				Min.	Typ.	Max.	
General Section							
V_{IN}	Input Supply Voltage		●	2.5		5.5	V
UVLO_H	V_{IN} Under Voltage Lockout Threshold	V_{IN} Rising		1.8	2	2.2	V
UVLO_L		Hysteresis			0.1		
I_Q	V_{IN} Quiescent Current	V_{FB}=1.3V, LX no switching			1		mA
		V_{FB}=1.1V, LX switching			4		mA
I_{SHUT}	V_{IN} Shutdown Current	V_{EN}=0	●			1	µA
V_{ENH}	EN Threshold					2	V
V_{ENL}				0.8			
T_{SD}	Thermal Shutdown Temperature				150		ºC
$\triangle T_{SD}$	Thermal Shutdown Hysteresis				25		ºC
Reference							
V_{REF}	Reference Voltage		●	1.176	1.2	1.224	V
	Reference Load Regulator	0<I_{REF}<50µA	●			6	mV
I_{REF}	Reference Current Capability	At VREF-1.5%	●	100			µA
	Reference Undervoltage Lockout Threshold	Rising edge. Hysteresis(typ)=200mV			0.8		V
Oscillator							
f_{OSC}	Operation Frequency		●	900	1200	1500	kHz
D_{MAX}	Oscillator Maximum Duty Cycle			87	90	93	%

Electrical Characteristics (Continued)

The ● denote the parameter apply over the full operating temperature range, otherwise the values are tested at T_A=+25 ºC. V_{IN}=3.3V, V_{OUT}=8.5V, unless otherwise noted.

Symbol	Parameter	Conditions		EUP2619			Unit
				Min.	Typ.	Max.	
Main Step-Up Regulator							
V_{OUT}	Output Voltage Range		●	V_{IN}		18	V
V_{FB}	Feedback Voltage	No load	●	1.176	1.2	1.224	V
				1.188	1.2	1.212	
	FB Load Regulation	0<I_{LOAD}<Full, transient only			-1		%
	FB Line Regulation	V_{IN}=2.5V to 5.5V			0.15	0.25	%/V
	FB Input Bias Current	V_{FB}=1.2V		50	125	200	nA
Gm	Transconductance of Error Amplifier				70		μA/V
$R_{LX(ON)}$	LX ON-Resistance	I_{LX}=200mA			0.16	0.25	Ω
	Current Sense Transconductance			3.3	5	10	A/V
I_{LIM}	Current Limit				2.8		A
	N-MOSFET Leakage Current	V_{LX}=19V	●		1	10	μA
	Soft-start period	7 bit current ramp			8		ms
V_{COM} Buffer							
V_{SUP}	Supply Voltage Range		●	6		18	V
	V_{SUP} Undervoltage Threshold			3.8	4	4.2	V
I_{OP}	Supply Current	Buffer configuration, V_{OPAI}=V_{SUP}/2, no load	●		4	6.5	mA
V_{OS}	Input Offset Voltage	V_{OPAO}, V_{OPAI}=V_{SUP}/2				8	mV
I_{BIAS}	Input Bias Current	V_{OPAO}, V_{OPAI}=V_{SUP}/2	●	-1		1	μA
	Input Common Mode Voltage Range		●	0		V_{SUP}	V
	Input Common Mode Rejection Ratio				80		dB
V_{OH}	Output Voltage Swing High	I_{OUT}=1mA		V_{SUP}-50			mV
		I_{OUT}=50mA		V_{SUP}-300			
V_{OL}	Output Voltage Swing Low	I_{OUT}=-1mA				50	mV
		I_{OUT}=-50mA				300	
	Short-Circuit Current	Sourcing	●	500			mA
		Sinking	●	500			
F_{3dB}	-3dB Bandwith				20		MHz
SR	Slew Rate				45		V/μs
	Large Signal Voltage Gain	V_{OUT}=1V to (V_{SUP}-1)V			80		dB
Gate-High Regulator							
	V_{SUP} Input Supply Range		●	6		18	V
	V_{SUP} Over Voltage Threshold	V_{SUP}=Rising, Hystersis=200mV		19	20	21	V
	FBP Line Regulation Error	V_{SUP}=8V to 18V, V_{GH}=15V				0.2	%/V
	FBP Input Bias Current	V_{FBP}=1.5V		-50		50	nA
	DRVP Current Limit	Not in dropout			400		mA
V_{FBP}	Feedback Reference Voltage	No load		1.176	1.2	1.224	V

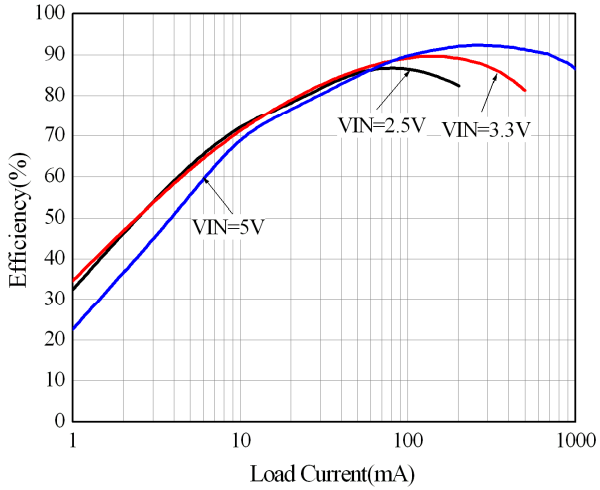
Electrical Characteristics (Continued)

The ● denote the parameter apply over the full operating temperature range, otherwise the values are tested at T_A=+25 ºC. V_{IN}=3.3V, V_{OUT}=8.5V, unless otherwise noted.

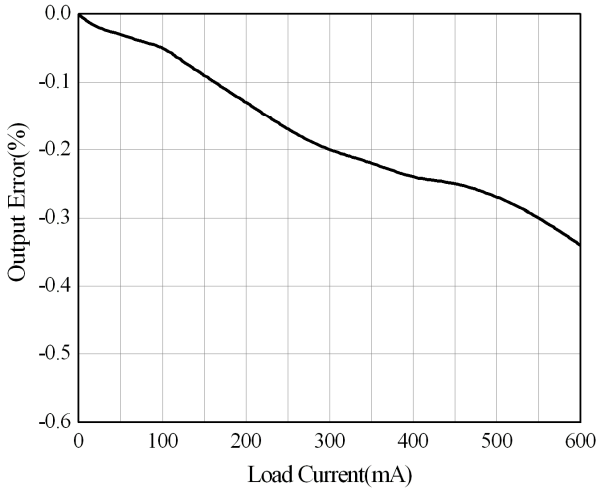
Symbol	Parameter	Conditions		EUP2619			Unit
				Min.	Typ.	Max.	
Gate High Regulator							
R_{ONP_P}	DRVP Switch On-Resistance				4	6	Ω
R_{ONP_N}					1.5	3	
fsw_P	Switching Frequency				600		kHz
	Positive Charge Pump Soft-start Period	7 bit voltage ramp with filtering to prevent high peak currents			3	5	ms
Gate-Low Regulator							
	V_{SUP} Input Supply Range			6		18	V
	FBN Line Regulation Error	V_{SUP}=9V to 18V, V_{GL}=-7V				0.2	%/V
	FBN Input Bias Current	V_{FBN}=0.24V		-50		50	nA
	DRVN Current Limit	Not in dropout			400		mA
V_{FBN}	Feedback Reference Voltage	No load		0.21	0.24	0.27	V
R_{ONN_P}	DRVN Switch On-Resistance				4	6	Ω
R_{ONN_N}					1.5	3	
fsw_N	Switching Frequency				600		kHz
	Negative Charge Pump Soft-start Period	7 bit voltage ramp with filtering to prevent high peak currents			3	5	ms
Fault Detector							
	FB Fault Trip Level	V_{FB} Falling			0.95		V
	FBN Fault Trip Level	V_{FBN} Rising			0.42		V
	FBP Fault Trip Level	V_{FBP} Falling			0.95		V
	Fault Delay				100		ms
RESETB Control							
V_{RSTB_VTH}	RESETB Threshold	VIN Falling			2.4		V
	Hysteresis				0.14		V
V_{RSTB}	RESETB Output Voltage	I_{sink}=1mA				0.4	V
T_{RSTB_DLY}	RESETB Blanking Time				120		ms

Typical Operating Characteristics

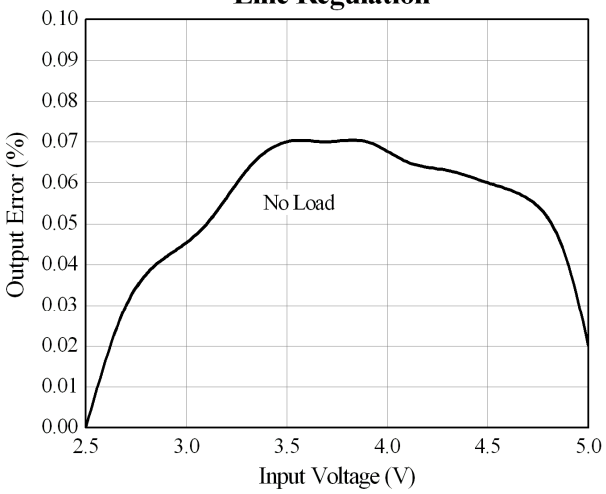
Step-up Regulator Efficiency vs. Load Current



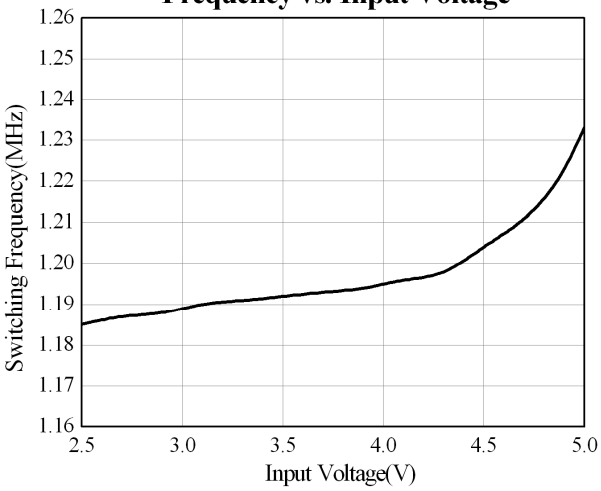
Step-up Regulator Output Voltage vs. Load Current



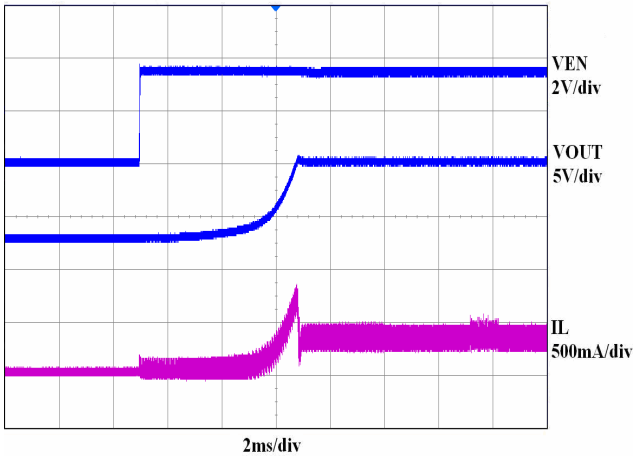
Step-up Regulator Line Regulation



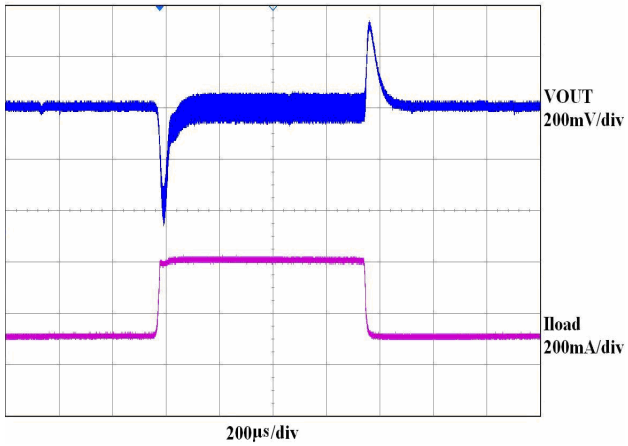
Step-up Regulator Switching Frequency vs. Input Voltage



Step-up Regulator Startup with 100mA Load

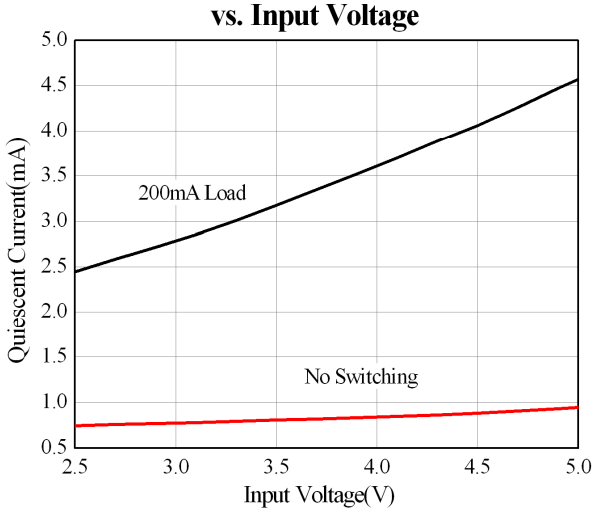


Step-up Regulator Load-Transient Response (100mA to 400mA)

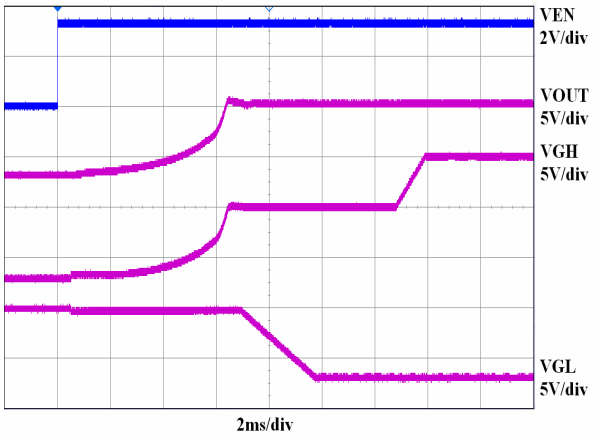


Typical Operating Characteristics (continued)

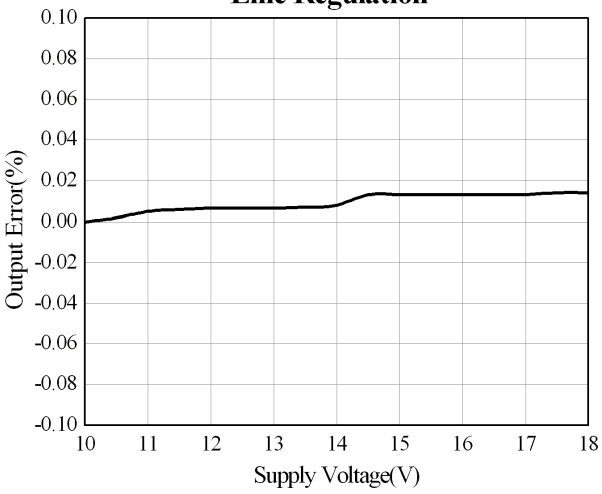
Quiescent Current vs. Input Voltage



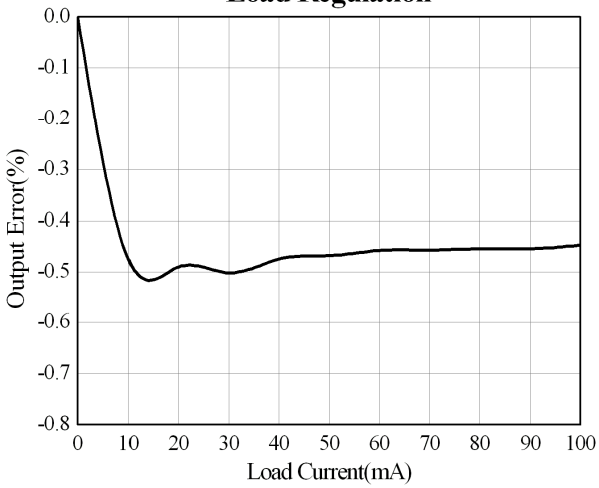
Power-up Sequence of Boost and Charge Pump



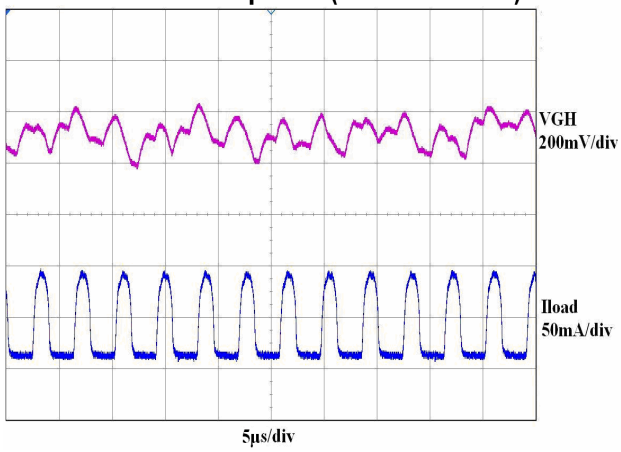
Positive Charge-Pump Regulator Line Regulation



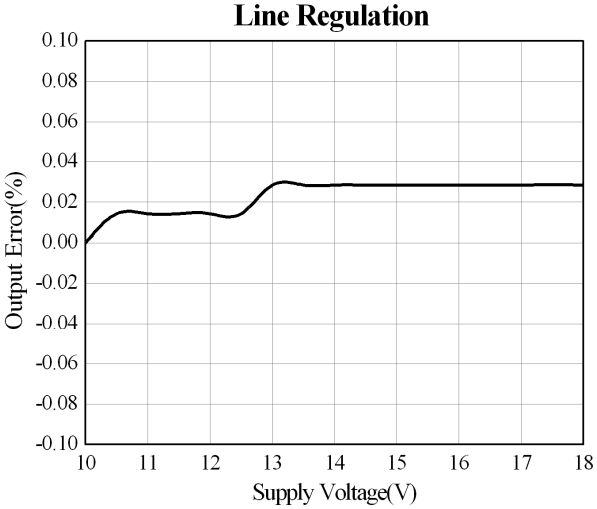
Positive Charge-Pump Regulator Load Regulation



Positive Charge-Pump Regulator Load-Transient Response (10mA to 90mA)

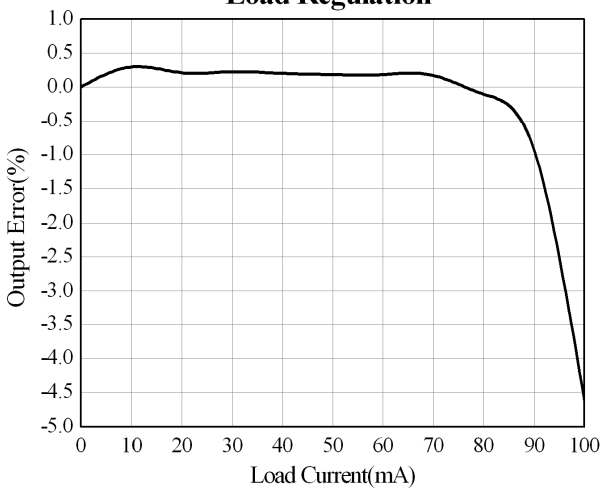


Negative Charge-Pump Regulator Line Regulation

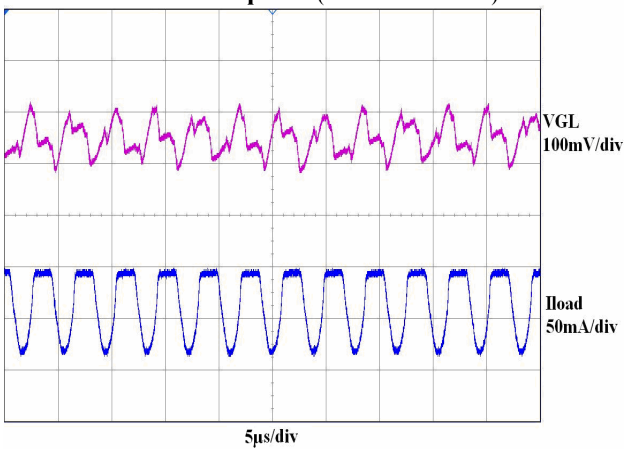


Typical Operating Characteristics (continued)

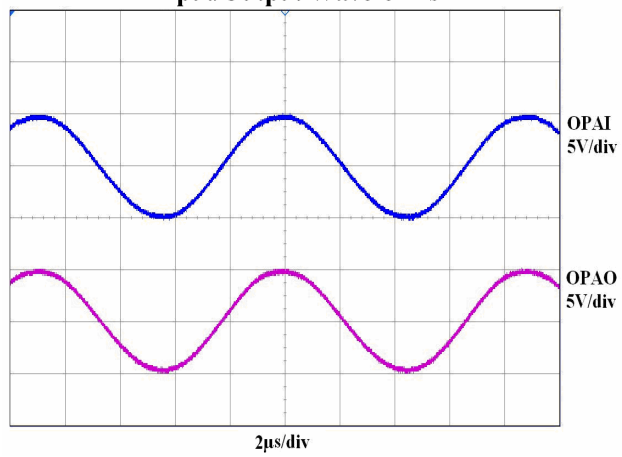
Negative Charge-Pump Regulator Load Regulation



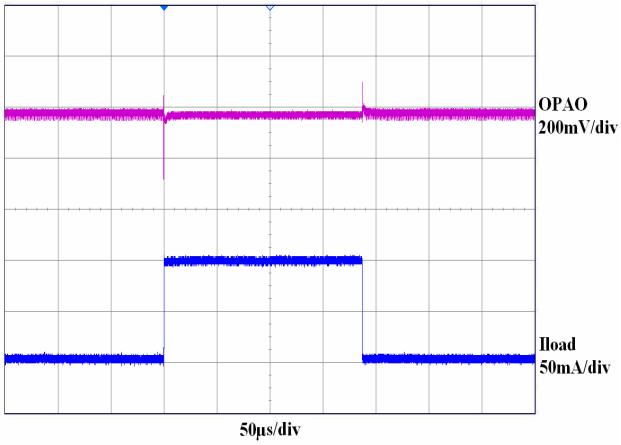
Negative Charge-Pump Regulator Load-Transient Response (10mA to 80mA)



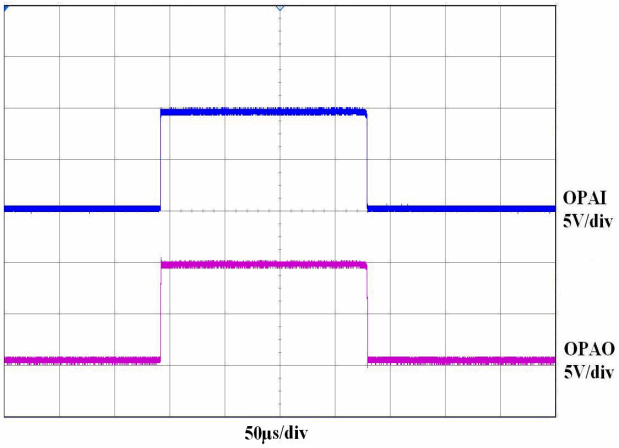
Operational Amplifier Rail-to-Rail Input/Output Waveforms



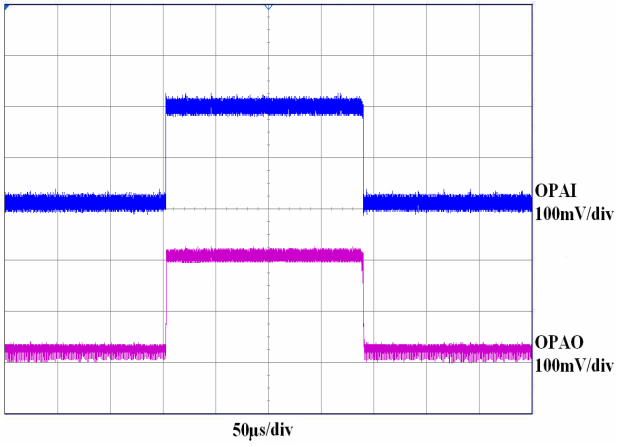
Operational Amplifier Load-Transient Response



Operational Amplifier Large-signal Step Response



Operational Amplifier Small-signal Step Response



Typical Operating Characteristics (continued)

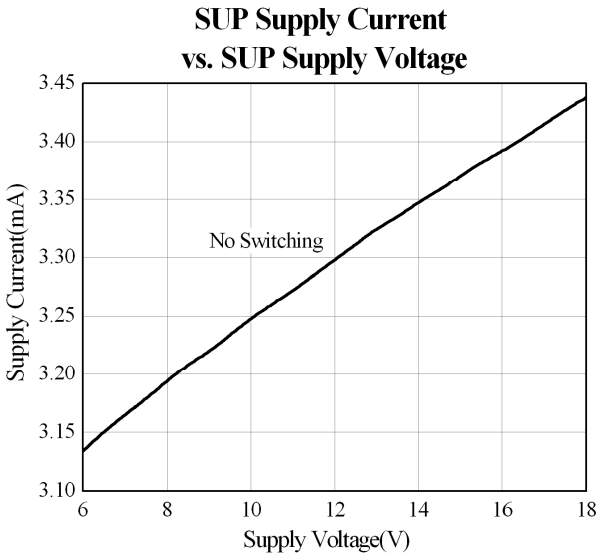


Table 1. Component List (Figure1)

Designation	Description
C1	1μF, 6.3V, X7R ceramic capacitor
C2	22μF, 25V, X5R ceramic capacitor
C4	820pF, 6.3V, X7R ceramic capacitor
C5, C7	0.1μF, 25V, X7R ceramic capacitors
C6, C9	1μF, 25V, X7R ceramic capacitors
C8	220nF, 6.3V, X7R ceramic capacitor
C10, C11	10μF, 6.3V, X5R ceramic capacitors
C12	10μF, 25V, X5R ceramic capacitor
D1	Schottky diode 30V, 3A DIODES B330A
D2, D3	Dual diodes 30V, 200mA(3 SOT23) Zetex BAT54S Fairchild BAT54S
L1	Inductor, 10μH, 3A/50mΩ

Function Description

The EUP2619 contains a high performance current mode boost regulator, a gate-on charge pump driver and a gate-off charge pump driver. It also includes of a high-current rail-to-rail operation amplifier. The following content contains the detailed description and the information of the component selection.

Step-Up Converter

The Step-up regulator is a high efficiency current-mode PWM architecture with 1.2MHz operation frequency. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows smaller components to minimize the thickness of LCD panel. The Step-up Converter can operate in continuous conduction mode and steady state operation, where the inductor current is continuously. In the first half cycle, the power MOSFET is on and Schottky diodes are reverse biased, the output current is provided by output capacitor, inductor voltage is VIN, and its current increase at the rate of VIN/L; during the other half cycle, MOSFET is off and Schottky diodes are forward biased, the energy stored in the inductor is released. The inductor current ripple is:

$$\Delta I_L = \Delta T2 \times \frac{V_{IN} - V_{OUT}}{L}$$

$$\Delta T2 = \frac{1 - D}{F_{SW}}$$

Where L is self-inductance, the energy of inductor is stored by electromagnetic induction.

In the steady state operation, the energy stored in inductor must be converted equally, so the inductor current ripples in two half cycle are identical.

$$\frac{D}{F_{SW}} \times \frac{V_{IN}}{L} + \frac{1-D}{F_{SW}} \times \frac{V_{IN} - V_{OUT}}{L} = 0$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

Output Voltage

The output voltage is reduced to a reference voltage 1.2V by external feedback resistor divider. The resistors maximum value is limited by feedback output biased current and potential coupling noise of feedback pin.

Output voltage of Step up Converter can be set according to the following equations:

$$V_{OUT} = 1.2 \times \left(1 + \frac{R1}{R2}\right)$$

The recommended range of R2 is from 10kΩ to 50kΩ. Place the resistor divider as close as possible to the chip can reduce noise sensitivity.

Inductor Selection

The output voltage ripple, transient response, capacity and efficiency of output current supply are decided by inductor selection and the inductor value is influenced by input and output voltage, switching frequency and the maximum output current. A 4.7μH or 10μH inductor is recommended for small ripple applications.

Output Capacitor Selection

Small value of ESR capacitor can minimum the output voltage ripple. So it is recommended that multi-layer ceramic capacitors（X5R or X7R）are used to be output capacitor because of its low ESR characteristics and small size in package. ESR determines the output voltage ripple according to the equation:

$$\Delta V_O = \frac{I_O \times D}{F_{SW} \times C_O} + I_O \times ESR$$

Diode Selection

Schottky diodes, with their low forward voltage drop and fast reverse recovery, are the ideal choices for EUP2619 applications. It must be chosen correctly depending on some parameters such as reverse breakdown voltage, forward current and forward voltage drop. A Schottky diode rated at 3A is sufficient for most EUP2619 applications.

Input Capacitor Selection

Input capacitors, which are decided by input and output voltage, maximum output current, inductor and supply noise, are important in restraining input voltage ripple and enhancing chip performance. In most application, a 20μF capacitor is suitable. Care must be taken to make sure that chip is normal operated, a 10Ω resistor and a 1μF bypass capacitor should be taken next to the VIN pin to decrease the high frequency noise of power wire.

Loop Compensation

The feedback loop of EUP2619 contains a trans-conductance amplifier, which makes the chip achieve better transient response and regulation. The EUP2619 employs current mode control architecture, which features rapid current sense loop and slow voltage feedback loop. Compensation is not required for rapid current sense loop but is necessary for slow voltage feedback loop to insure that the device is in the steady state. RC network connected between the COMP pin and AGND is a compensation network. In the network, resistors play a decisive role in achieving a high gain of high-frequency and obtain fast transient response. Capacitor sets the zero of the integrator. Assuring about loop stabilization, capacitor must be chosen between 220pF~10nF and resistor must be chosen accurately in the range of 2kΩ ~100kΩ.

Dual Charge-Pump Regulator

The EUP2619 contain two individual low-power charge pumps. One charge pump inverts the supply voltage (SUP) and provides a regulated negative output voltage. The second charge pump doubles the supply voltage (SUP) and provides a regulated positive output voltage. The EUP2619 contain internal p-channel and n-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant 600kHz ($0.5\times F_{sw}$).

Negative Charge Pump

During the first half-cycle, the p-channel MOSFET turns on and the flying capacitor C7 charges to VSUP minus a diode drop. During the second half-cycle, the p-channel MOSFET turns off, and the n-channel MOSFET turns on, level shifting C9. This connects C7 in parallel with the reservoir capacitor C9. If the voltage across C9 minus a diode drop is higher lower than the voltage across C7, charge flows from C9 to C7 until the diode turns off. The amount of charge transferred to the output is controlled by the variable n-channel on-resistance. The output voltage of negative charge pump is set by:

$$VGL = 0.24\times\left(1+\frac{R7}{R6}\right)-1.2\times\left(\frac{R7}{R6}\right)$$

Positive Charge Pump

During the first half-cycle, the n-channel MOSFET turns on and charges the flying capacitor C5 to the VOUT voltage. During the second half-cycle, the n-channel MOSFET turns off and the p-channel MOSFET turns on to charge the DRVP pin up to the SUP voltage. At this cycle, C5 is connected in parallel with C6 and pumps the maximum output voltage to (VSUP+VOUT). The output voltage of positive charge pump is set by:

$$VGH = 1.2\times\left(1+\frac{R4}{R5}\right)$$

Operational Amplifier

Operational Amplifier provides V_{COM} voltage for LCD monitor. The operational amplifier is capable of ±100mA continuous output current, 45V/μs slew rate, 20 MHz -3dB bandwidth and rail to rail input/output voltage.

Reference Voltage

The reference voltage is nominally 1.2V, which can deliver up to 100μA with good regulation. Connect a 0.22μF bypass capacitor between REF and AGND.

Fault Protection

EUP2619 has over current protection and over temperature protection. When the chip working, integrated over temperature protection circuit continuous detects the chip temperature, and the chip would be turn off if the chip temperature exceed the over temperature protection threshold.

During steady-state operation, if the output of the boost converter or any of the charge pump outputs exceeds its respective fault-detection threshold, the EUP2619 activates an internal fault timer. If any condition or combination of conditions indicates a continuous fault for the fault-timer duration (100ms typ), the EUP2619 sets the fault latch to shut down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) or EN pin to clear the fault latch and reactivate the device.

Power-Up Sequence

The EUP2619 employs soft-start circuitry to reduce supply inrush current during start up conditions. Once the voltage on IN exceeds approximately 2V, the reference turns on. With a 0.22μF REF bypass capacitor, the reference reaches its regulation voltage of 1.2V. When the reference voltage exceeds 0.8V, the ICs enable the boost regulator. Once the FB voltage is above 1V, the gate-off charge pump driver is enabled immediately, and gate-on charge pump driver starts up after 4ms (TYP) delay time.

Voltage Detector Circuit

During power-up, once the chip is enabled (VIN>UVLO and EN is high), the IC initiates a 120ms blanking time period. During which the RSTB pin is floated to high impedance. While floating, RSTB is pulled high by an external pull-up resistor. After this blanking period the reset function is enabled, with RSTB pin driven low if VIN below 2.4V, or floated high if VIN rises above 2.54V.

Timing Diagram

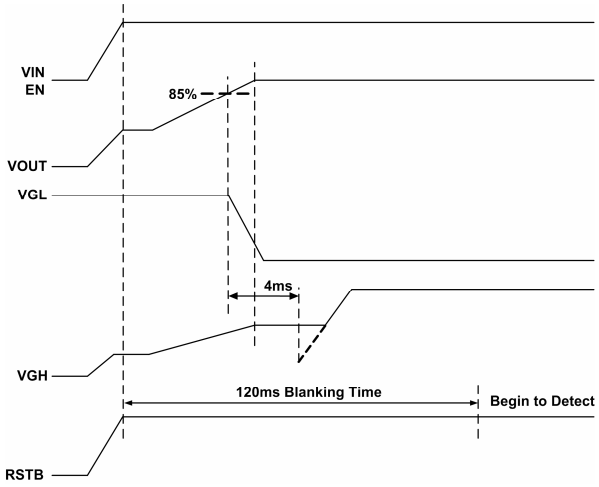


Figure 3.

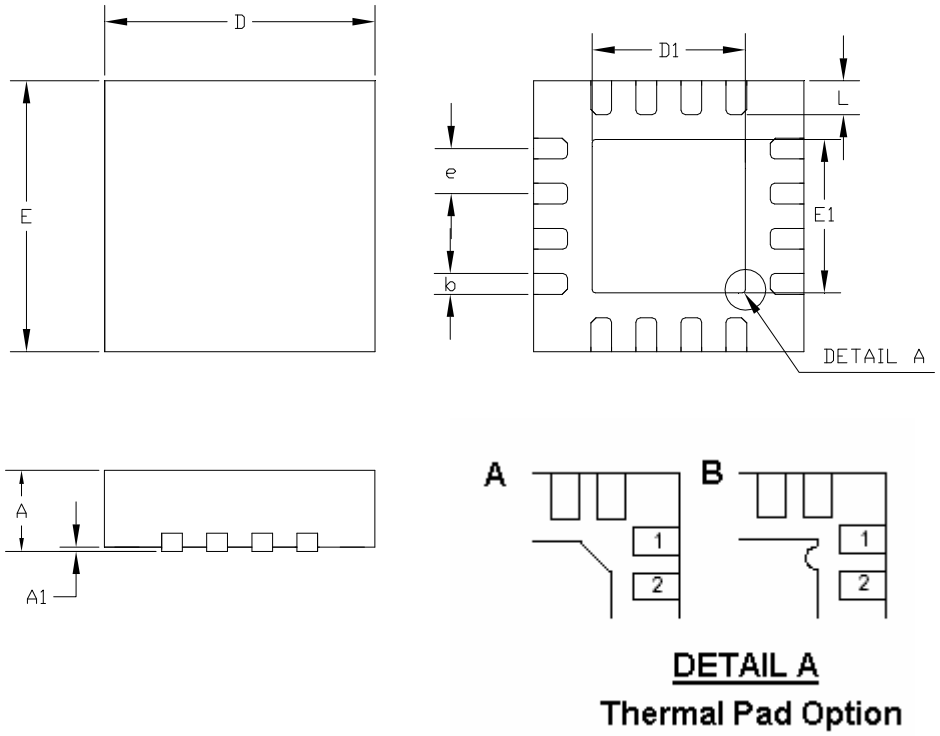
PCB Layout

To obtain high performance including good regulation, high efficiency and stability, high power switching supply, a good PCB layout is expected. The PCB layout must be evaluated strictly. Power element should be placed as close as possible ensuring the traces are short, straight and wide. Put power element together enough, and connect them by using asteroid in the element layer, then connect the asteroid to external Ground using some vias. Do not connect the GND pin of power element to external Ground. There are some general guidelines for layout:

1. Place the VIN pin and REF pin bypass capacitors as close as possible to the device.
2. Keep the traces of the main current paths as short and wide as possible.
3. Put all the feedback resistances within the 5mm scope of the corresponding feedback pin of them and keep the traces short enough to avoid switching noise. Keep feedback traces as close as possible to LX prevent a shield come into being.
4. Keep the traces between output capacitance and load as short and wide as possible to get a best transient response.
5. LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.

Packaging Information

TQFN-16



Note: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
E	2.90	3.00	3.10	0.114	0.118	0.122
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	1.40	1.70	1.75	0.055	0.067	0.069
E1	1.40	1.70	1.75	0.055	0.067	0.069
e	0.50 REF			0.020 REF		
L	0.30	0.40	0.50	0.012	0.016	0.020