

## 15-W Stereo Class-D Audio Power Amplifier with Speaker Protection

### DESCRIPTION

The EUA2310B is a high efficiency, 2 channel bridged-tied load (BTL), class-D audio power amplifier. Operating from a 16V power supply, EUA2310B is capable of delivering 15W/ channel of continuous output power to a 8Ω load with 10% THD+N. The EUA2310B features a differential input architecture offering improved noise immunity over a single-ended (SE) input amplifier. Amplifier gain is internally configured and can be selected to 20, 26, 32 or 36dB utilizing the G0 and G1 gain select pins. Advanced EMI suppression technology enables the use of inexpensive ferrite bead at the outputs while meeting EMC requirements.

The speaker protection circuitry is integrated into EUA2310B to limit the amount of current through the speaker. Meanwhile, the AGC detects output signal clip due to the over level input signal and suppresses it automatically. The EUA2310B also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2310B is available in thermally efficient 28-pin TSSOP package.

### FEATURES

- Wide Supply Voltage: 5.5V to 26V
- Unique Modulation Scheme Reduces EMI Emission
- 15-W/ch into an 8-Ω Load From a 16-V Supply
- 10-W/ch into an 8-Ω Load From a 13-V Supply
- 30W into a 4-Ω Mono Load From a 16-V Supply
- 87% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Four Selectable, Gain Settings
- Differential Inputs
- Speaker Protection Circuitry
- Auto Gain Control and Power Clamp
- Thermal and Short-Circuit Protection
- 28-pin TSSOP Package with Thermal Pad
- RoHS compliant and 100% lead(Pb)-free Halogen-Free

### APPLICATIONS

- Televisions

### Typical Application Circuit

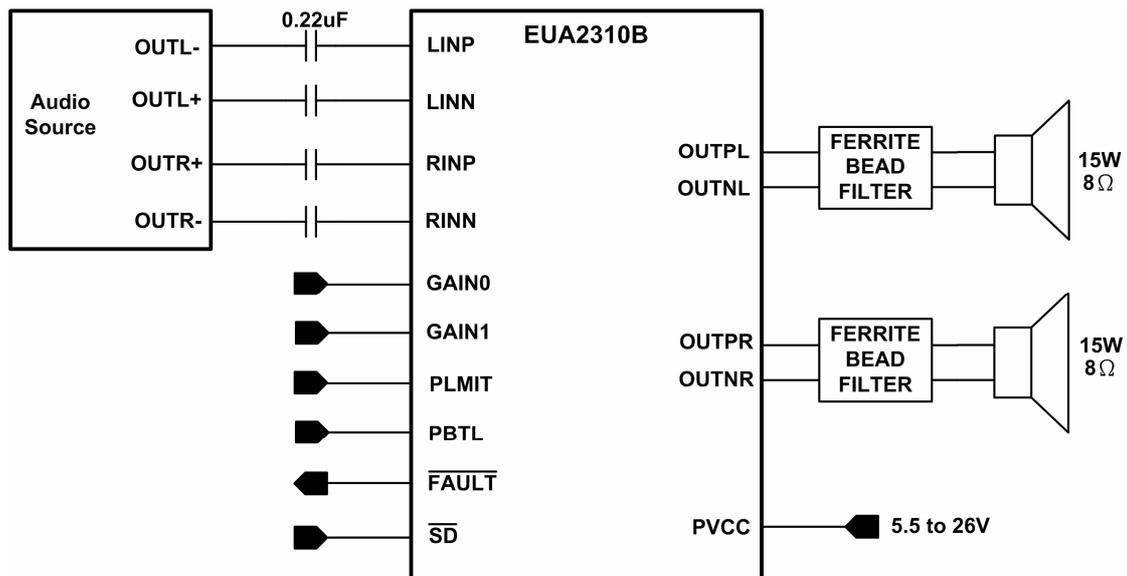


Figure1. Simplified Application Schematic

## Pin Configurations

Package Type	Pin Configurations
TSSOP-28 (EP)	<p>(Top View)</p>

## Pin Description

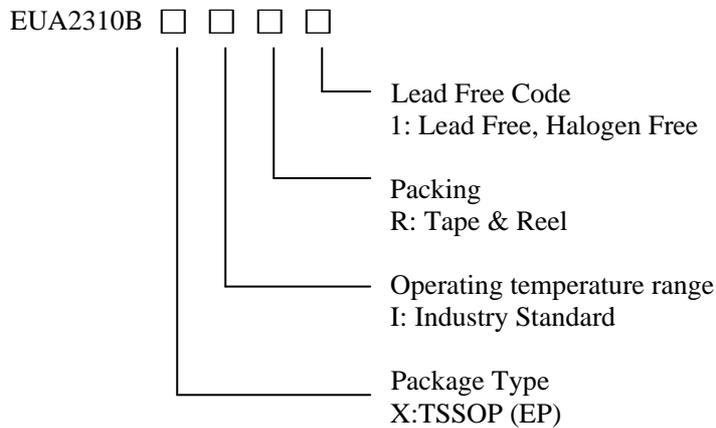
PIN	TSSOP-28(EP)	I/O/P	DESCRIPTION
$\overline{SD}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC.
LINP	3	I	Positive audio input for left channel.
LINN	4	I	Negative audio input for left channel.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply
AGND	8	P	Analog signal ground. Connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 4.5V. Also should be used as supply for PLIMIT function.
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Negative audio input for right channel.
RINP	12	I	Positive audio input for right channel.
NC	13	P	Power limit mode select. Defaulted low level for AGC function.
PBTL	14	I	Parallel BTL mode switch
PVCCR	15,16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19		Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.

## Pin Description (Continued)

PIN	TSSOP-28(EP)	I/O	DESCRIPTION
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24		Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	27,28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

## Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2310BXIR1	TSSOP-28 (EP)	 xxxxx EUA2310B	-40 °C to +85°C



## Absolute Maximum Ratings

- Supply Voltage, AVCC,PVCC, ----- -0.3 V to 30V
- Input Voltage,  $\overline{SD}$ , GAIN0,GAIN1,PBTL,  $\overline{FAULT}$  ----- -0.3 V to  $V_{CC} + 0.3V$
- Input Voltage, PLIMIT ----- -0.3 V to  $GVDD + 0.3V$
- Input Voltage, RINN,RINP,LINN,LINP ----- -0.3 V to 6.3V
- Thermal Resistance  $\theta_{JA}$  (TSSOP-28\_EP) ----- 34°C /W
- Free-air Temperature Range,  $T_A$  ----- -40°C to +85°C
- Junction Temperature Range,  $T_J$  ----- -40°C to +150°C
- Storage Temperature Rang,  $T_{stg}$  ----- -65°C to +150°C
- Lead Temperature ----- 260°C
- Load Resistance,  $R_{LOAD}$  ----- 3.2Ω Minimum

## Recommended Operating Conditions

		Min.	Max.	Unit
Supply voltage, $V_{CC}$	PVCC,AVCC	5.5	26	V
High-level input voltage, $V_{IH}$	$\overline{SD}$	2		V
	GAIN0,GAIN1,PBTL,NC	4		
Low-level input voltage, $V_{IL}$	$\overline{SD}$ , GAIN0,GAIN1,PBTL,NC		0.8	V
High-level input current, $I_{IH}$	$\overline{SD}$ , GAIN0,GAIN1,PBTL, $V_I=2V, V_{CC}=18V$		50	μA
Low-level input current, $I_{IL}$	$\overline{SD}$ , GAIN0,GAIN1,PBTL, $V_I=0.8V, V_{CC}=18V$		5	μA
Low-level output voltage, $V_{OL}$	$\overline{FAULT}$ , $R_{PULL-UP}=100k, V_{CC}=26V$		0.8	V
Oscillator frequency, $f_{OSC}$		230	330	kHz
Operating free-air temperature, $T_A$		-40	85	°C

## DC Characteristics $T_A = +25^\circ C, V_{CC}=24V, R_L=8\Omega$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2310B			Unit	
			Min.	Typ.	Max.		
$ V_{OS} $	Class-D output offset voltage (measured differentially)	$V_I = 0V$ , Gain = 36dB		5	50	mV	
$I_{CC}$	Quiescent supply current	$\overline{SD} = 2V$ , no load, $PV_{CC}=24V$			65	mA	
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD} = 0.8V$ , no load, $PV_{CC}=24V$		200	1000	μA	
$r_{DS(on)}$	Drain-source on-state resistance	$V_{CC}=12V$ , $I_O=500mA, T_J=25^\circ C$	High Side		240	mΩ	
			Low Side		240		
G	Gain	GAIN1=0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=4V	25	26	27	
		GAIN1=4V	GAIN0=0.8V	31	32	33	dB
			GAIN0=4V	35	36	37	
$t_{ON}$	Turn-on time	$\overline{SD} = 2V$		28		ms	
$t_{OFF}$	Turn-off time	$\overline{SD} = 0.8V$		28		ms	
GVDD	Gate Drive Supply	$I_{GVDD}=100\mu A$	4.2	4.5	4.8	V	
$t_{DCDET}$	DC Detect time	$V_{(RINN)}=5V, VRINP=0V$		420		ms	

## DC Characteristics $T_A = +25^\circ\text{C}$ , $V_{CC}=12\text{V}$ , $R_L=8\Omega$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2310B			Unit	
			Min.	Typ.	Max.		
$ V_{OS} $	Class-D output offset voltage (measured differentially)	$V_I=0\text{V}$ , Gain =36dB		5	50	mV	
$I_{CC}$	Quiescent supply current	$\overline{SD}=2\text{V}$ , no load, $PV_{CC}=12\text{V}$			45	mA	
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}=0.8\text{V}$ , no load, $PV_{CC}=12\text{V}$		200	1000	$\mu\text{A}$	
$r_{DS(on)}$	Drain-source on-state resistance	$V_{CC}=12\text{V}$ , $I_O=500\text{mA}$ , $T_J=25^\circ\text{C}$	High Side	240		m $\Omega$	
			Low Side	240			
G	Gain	GAIN1=0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=4V	25	26	27	
		GAIN1=4V	GAIN0=0.8V	31	32	33	dB
			GAIN0=4V	35	36	37	
$t_{ON}$	Turn-on time	$\overline{SD}=2\text{V}$		28		ms	
$t_{OFF}$	Turn-off time	$\overline{SD}=0.8\text{V}$		28		ms	
GVDD	Gate Drive Supply	$I_{GVDD}=2\text{mA}$	4.2	4.5	4.8	V	
$V_O$	Output voltage maximum under PLIMIT control	$V_{(PLIMIT)}=1.3\text{V}$ , $V_I=1\text{V}_{rms}$	6.75	7.90	8.75	V	

## AC Characteristics $T_A = +25^\circ\text{C}$ , $V_{CC}=24\text{V}$ , $R_L=8\Omega$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2310B			Unit
			Min.	Typ.	Max.	
$K_{SVR}$	Power supply ripple rejection	200mV <sub>PP</sub> ripple at 1kHz, Gain= 20dB, Inputs ac-coupled to AGND		-60		dB
$P_O$	Continuous output power	THD+N=10%, f=1kHz, $V_{CC}=16\text{V}$		15		W
THD+N	Total harmonic distortion +noise	$V_{CC}=16\text{V}$ , f=1kHz, $P_o=7.5\text{W}$ ( half-power)		0.2		%
$V_n$	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain=20dB		200		$\mu\text{V}$
				-74		dBV
	Crosstalk	$V_O=1\text{V}_{rms}$ , Gain=20dB, f=1kHz		-100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N< 1%, f=1kHz, Gain=20dB, A-weighted		90		dB
$f_{osc}$	Oscillator frequency		230	280	330	kHz
	Thermal trip point			150		$^\circ\text{C}$
	Thermal hysteresis			30		$^\circ\text{C}$

## AC Characteristics $T_A = +25^\circ\text{C}$ , $V_{CC}=12\text{V}$ , $R_L=8\Omega$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2310B			Unit
			Min.	Typ.	Max.	
$K_{SVR}$	Power supply ripple rejection	200mV <sub>PP</sub> ripple from 20Hz ~1kHz, Gain= 20dB, Inputs ac-coupled to AGND		-60		dB
$P_O$	Continuous output power	THD+N=10%, f=1kHz, $V_{CC}=13\text{V}$		10		W
THD+N	Total harmonic distortion +noise	$R_L=8\Omega$ , f=1kHz, $P_o=5\text{W}$ ( half-power)		0.2		%
$V_n$	Output integrated noise	20Hz to 22kHz, A-weighted filter, Gain=20dB		200		$\mu\text{V}$
				-74		dBV
	Crosstalk	$P_o=1\text{W}$ , Gain=20dB, f=1kHz		-100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N< 1%, f=1kHz, Gain=20dB, A-weighted		90		dB
$f_{OSC}$	Oscillator frequency		230	280	330	kHz
	Thermal trip point			150		$^\circ\text{C}$
	Thermal hysteresis			30		$^\circ\text{C}$

## Block Diagram

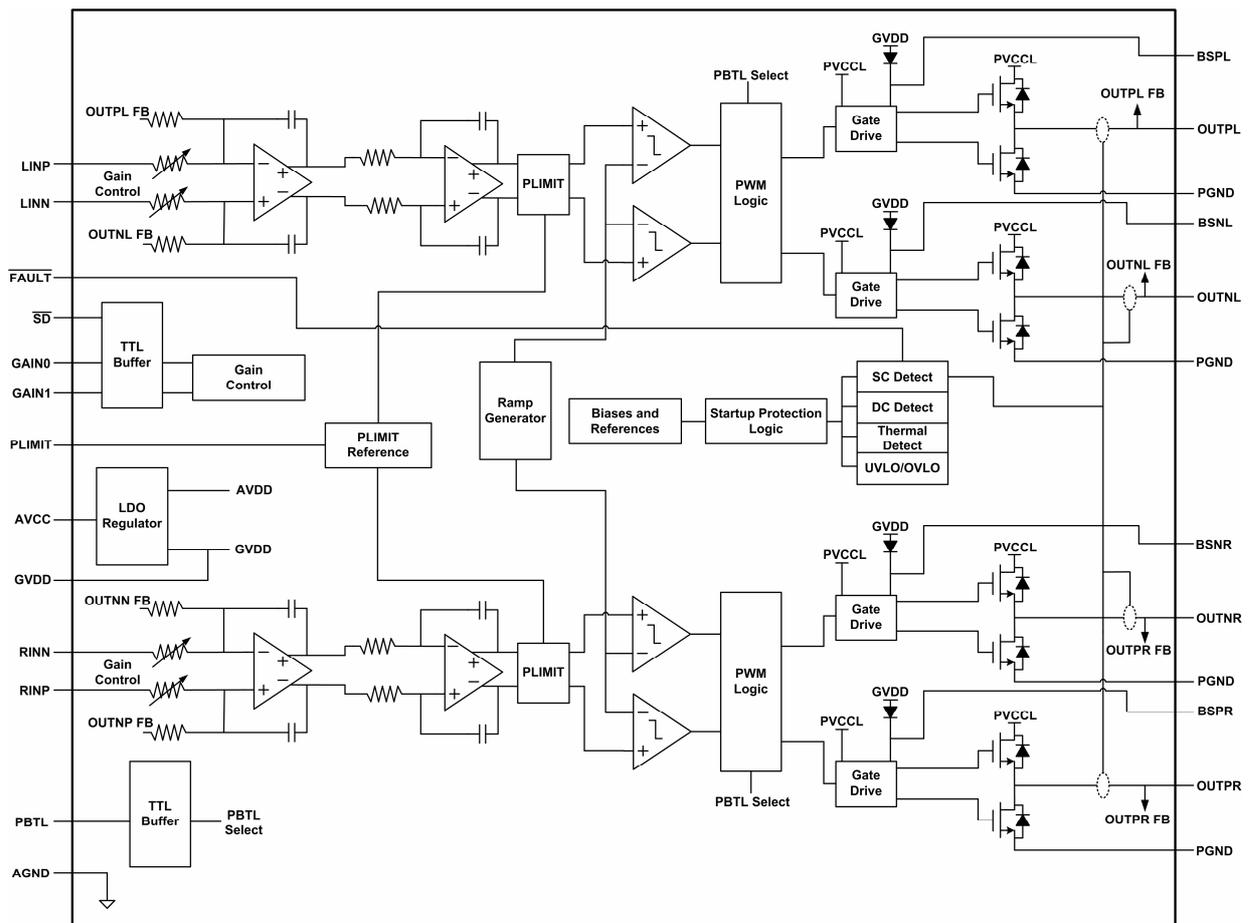


Figure2.

## Typical Characteristics

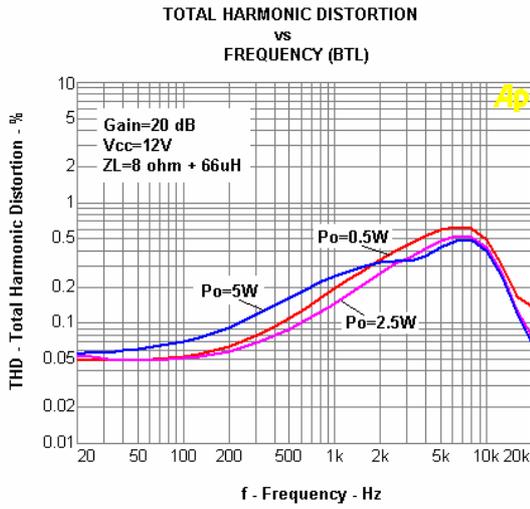


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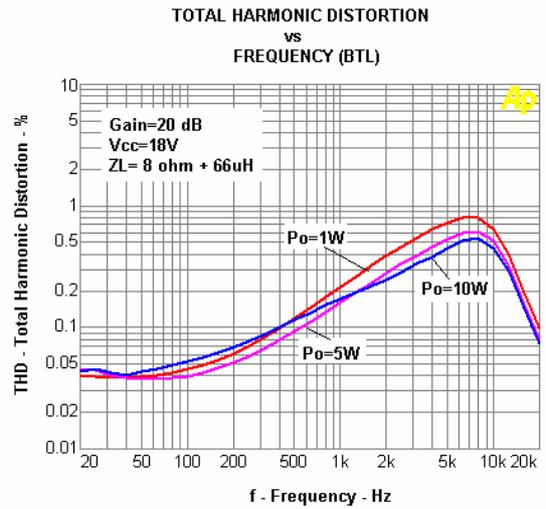


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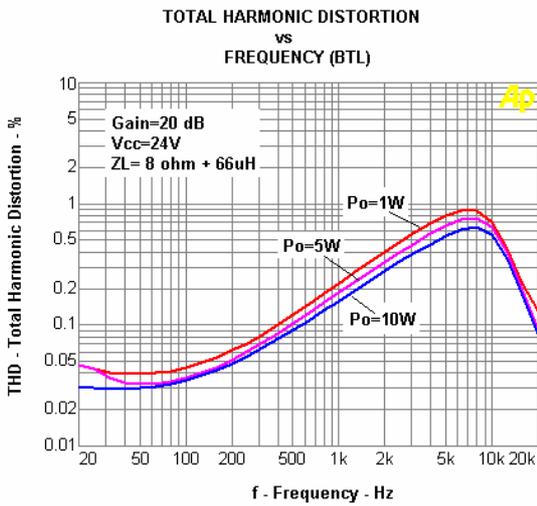


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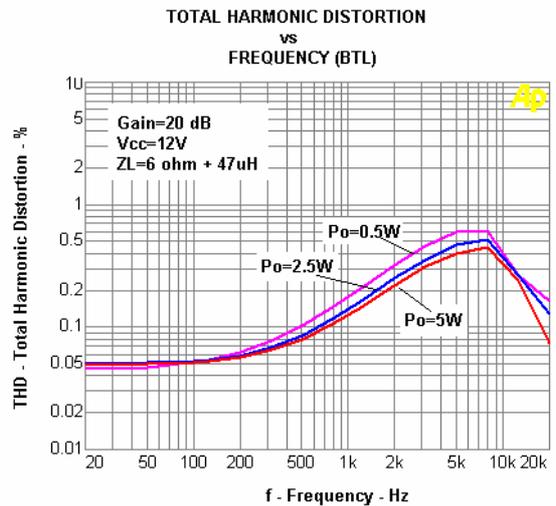


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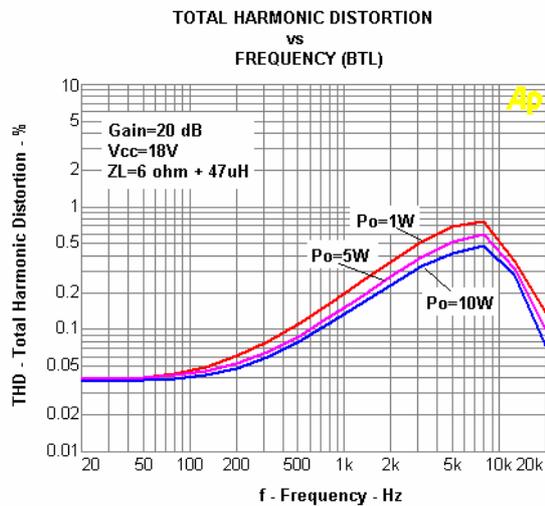


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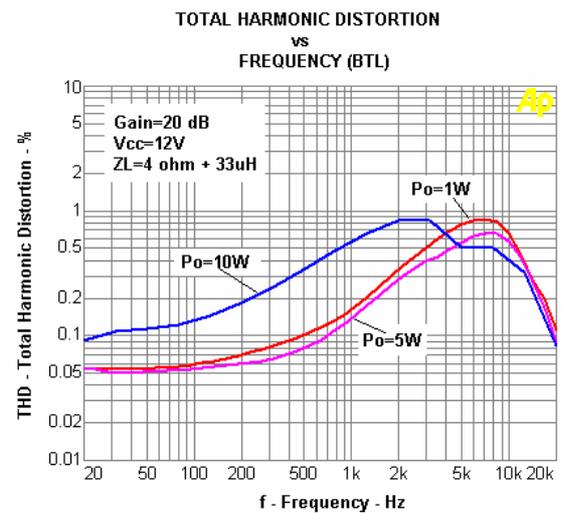
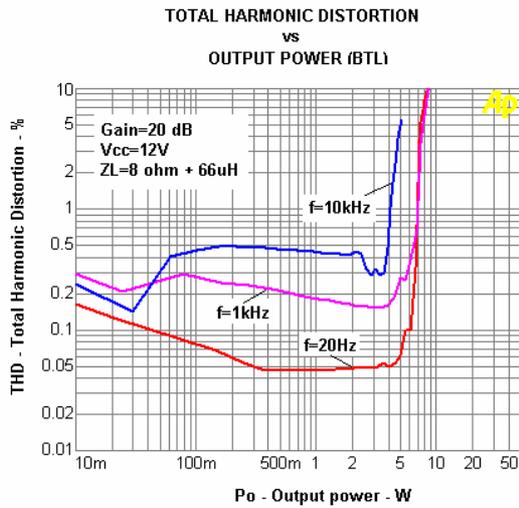
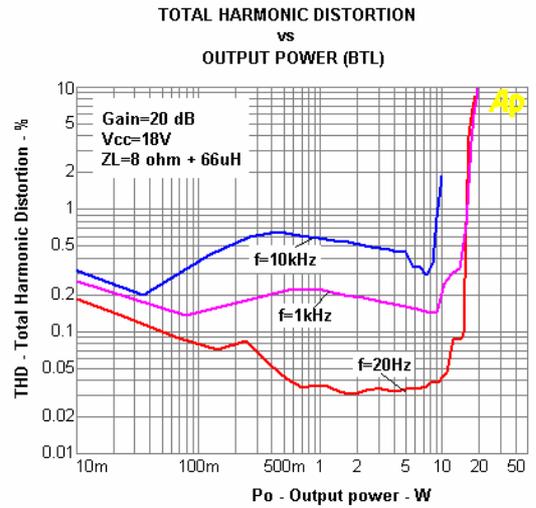


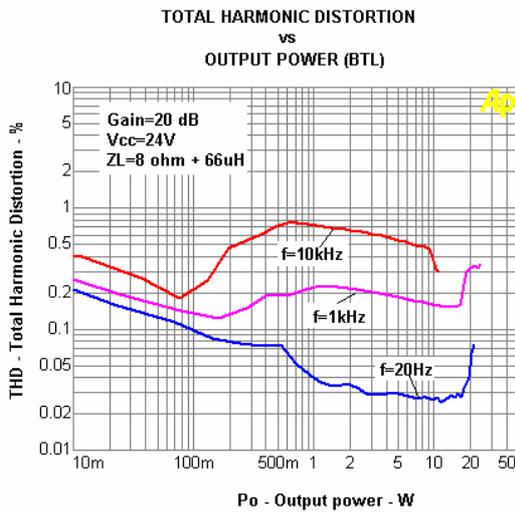
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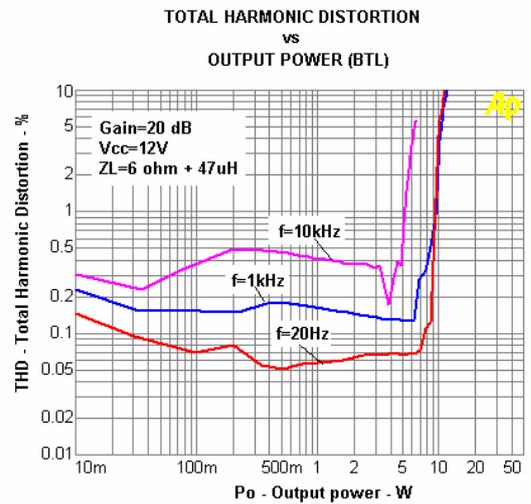
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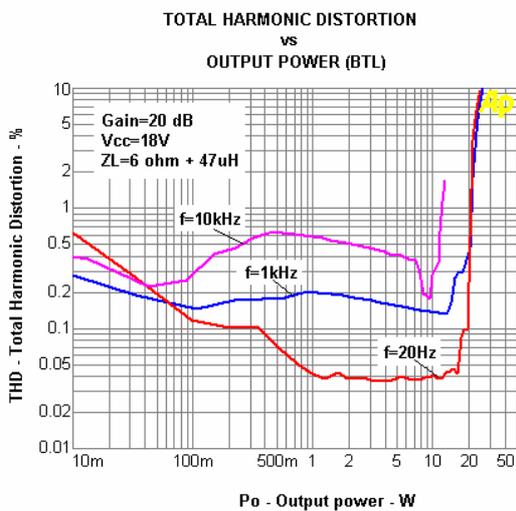
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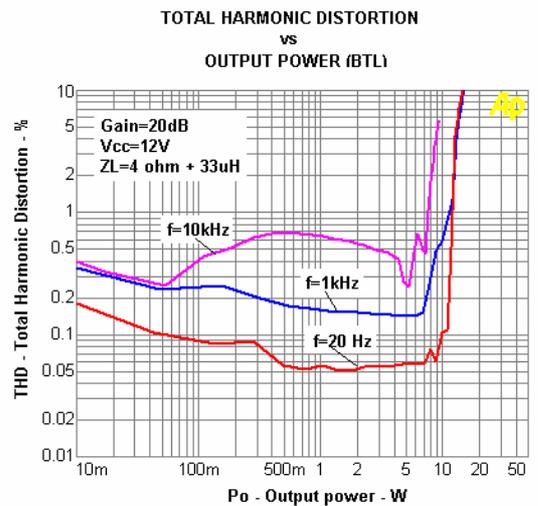
**Figure11.**



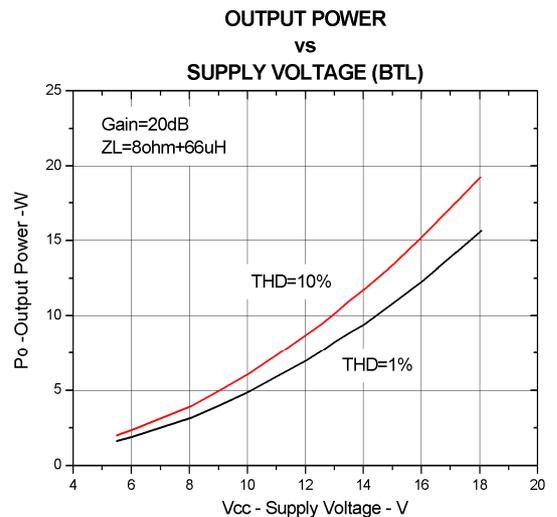
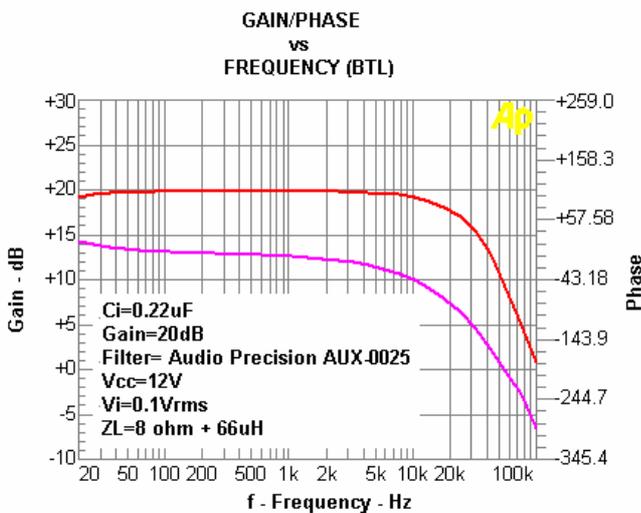
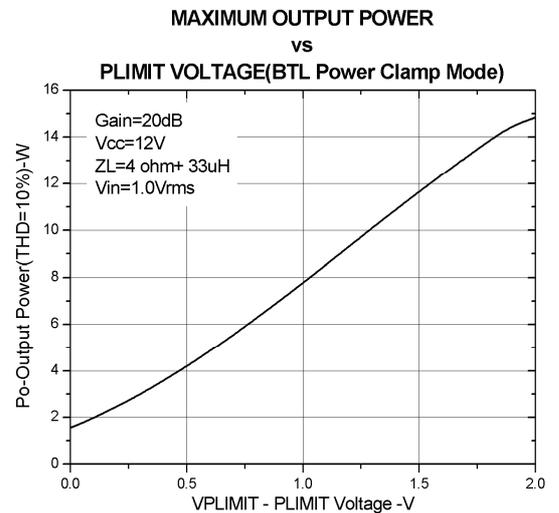
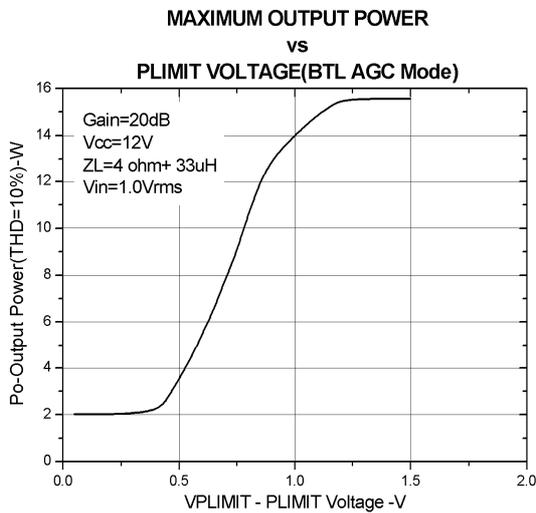
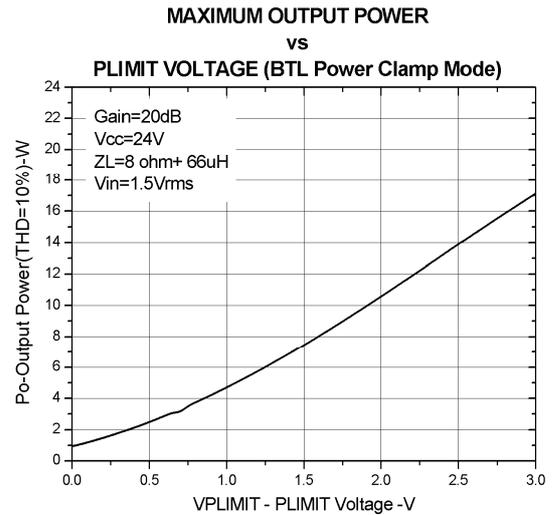
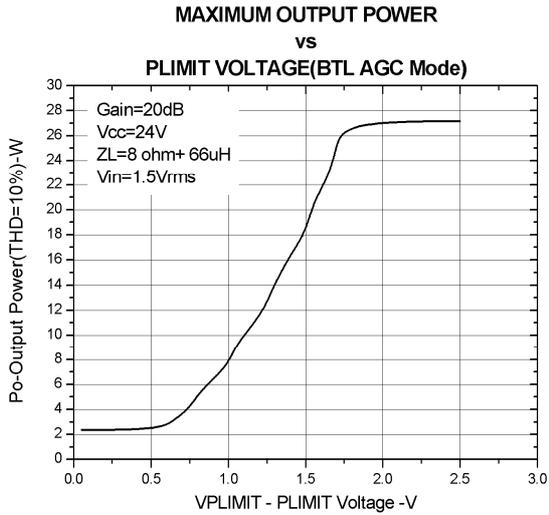
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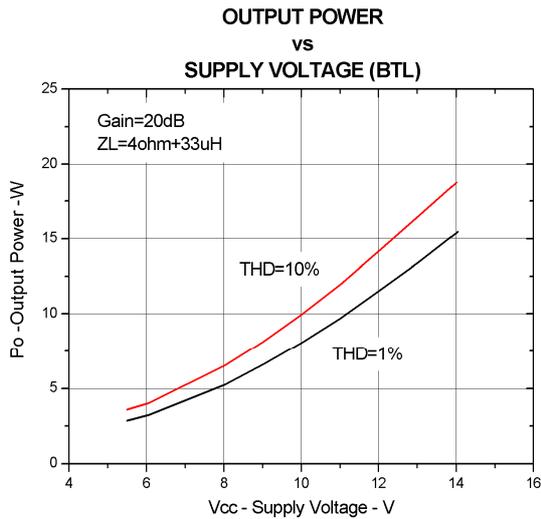


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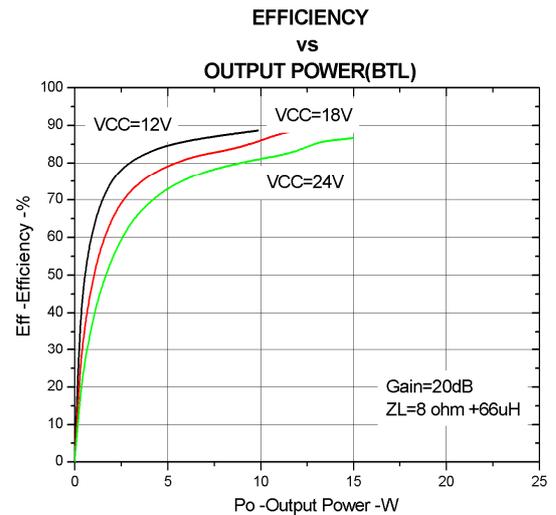


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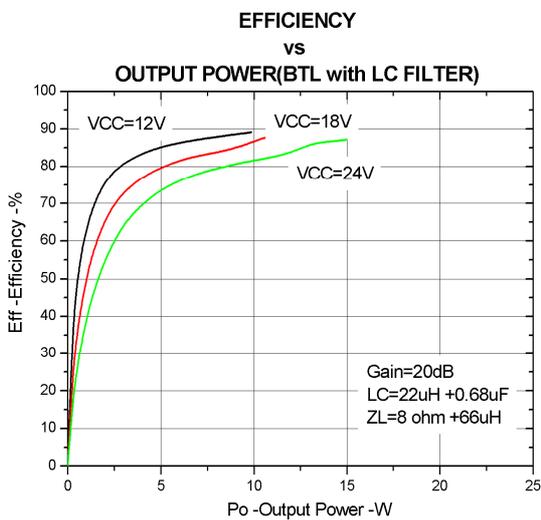




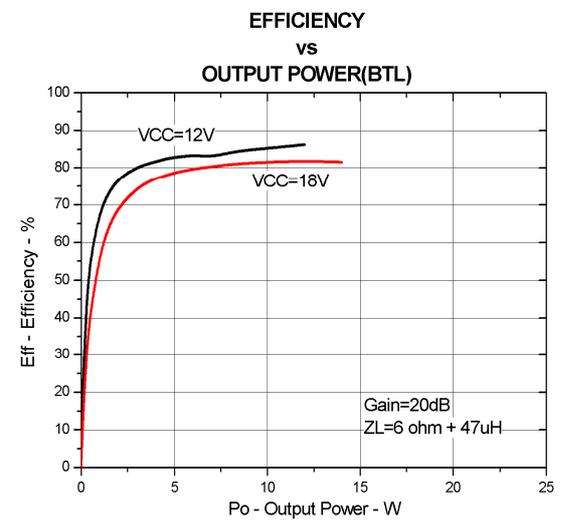
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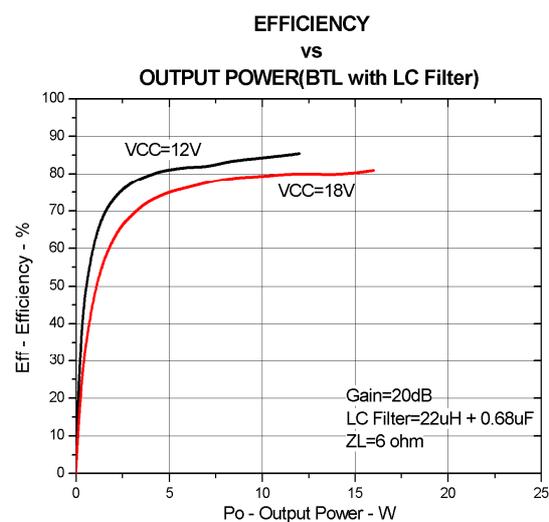
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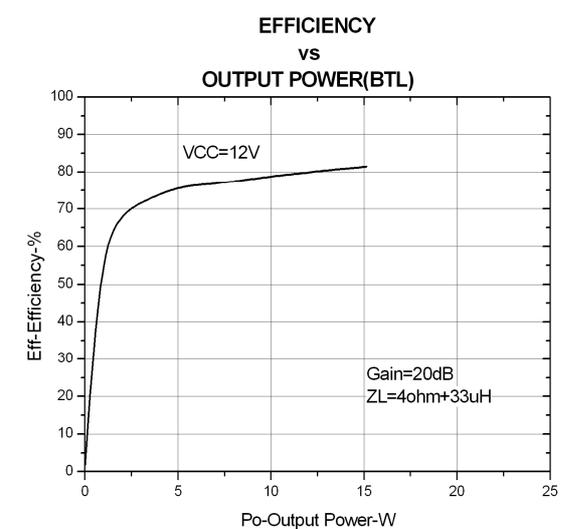
**Figure23.**



**Figure24.**



**Figure25.**



**Figure26.**

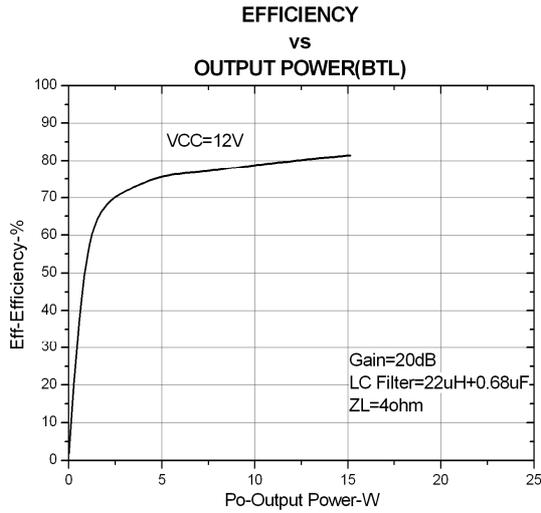


Figure27.

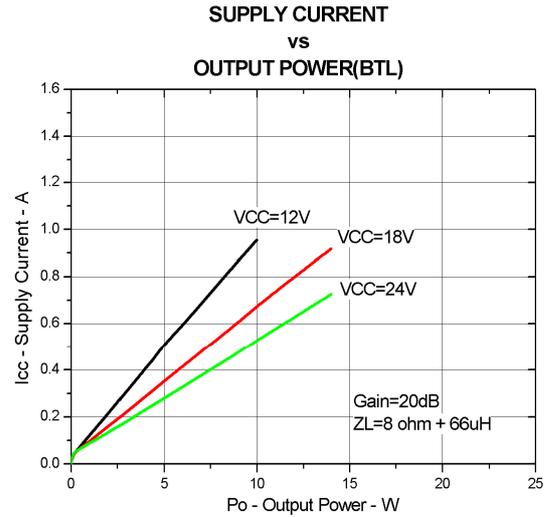


Figure28.

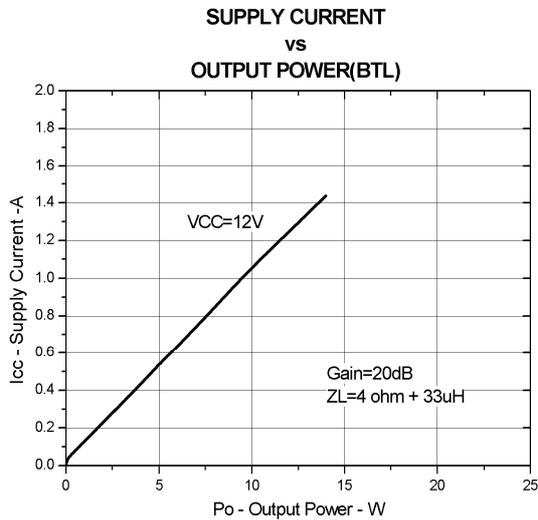


Figure29.

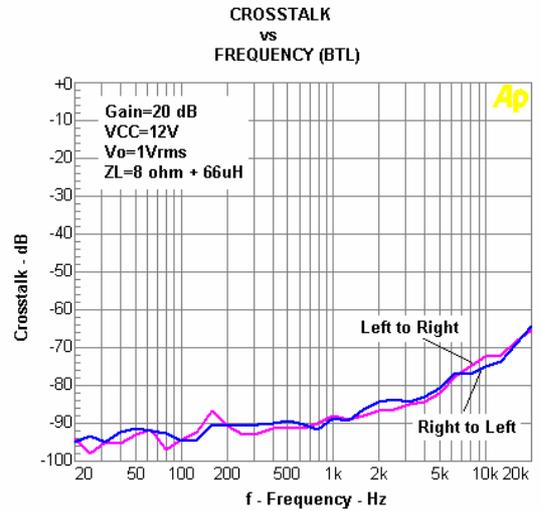


Figure30.

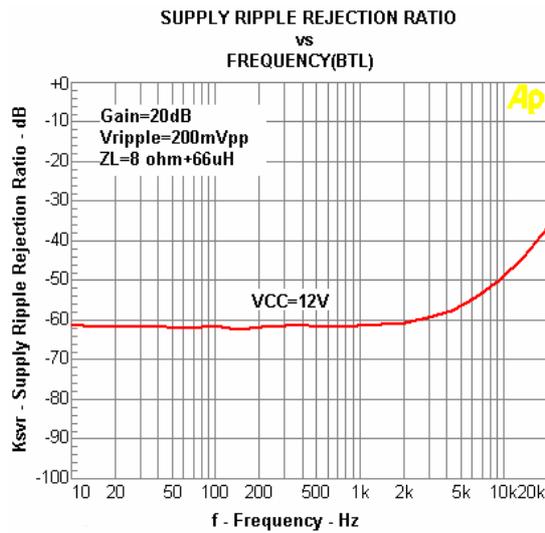


Figure31.

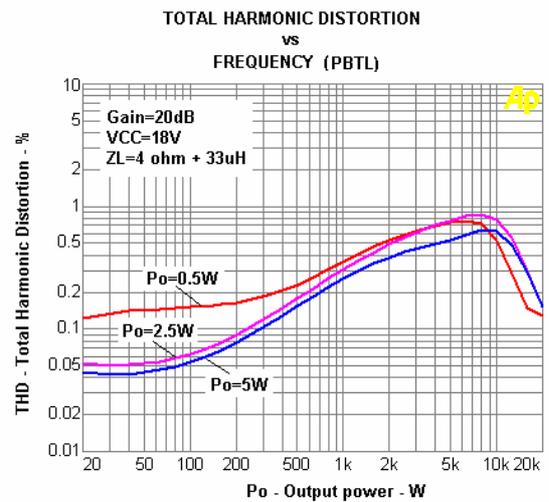


Figure32.

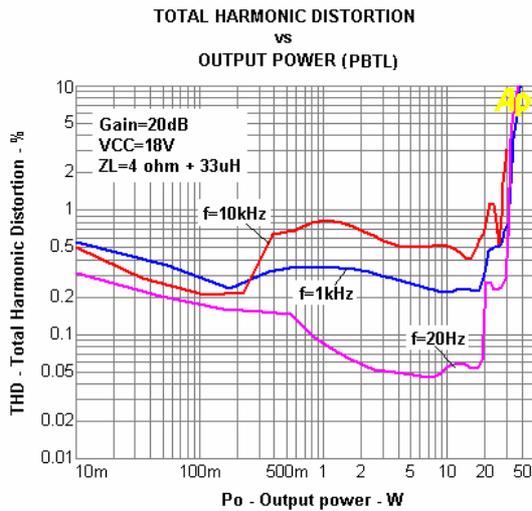


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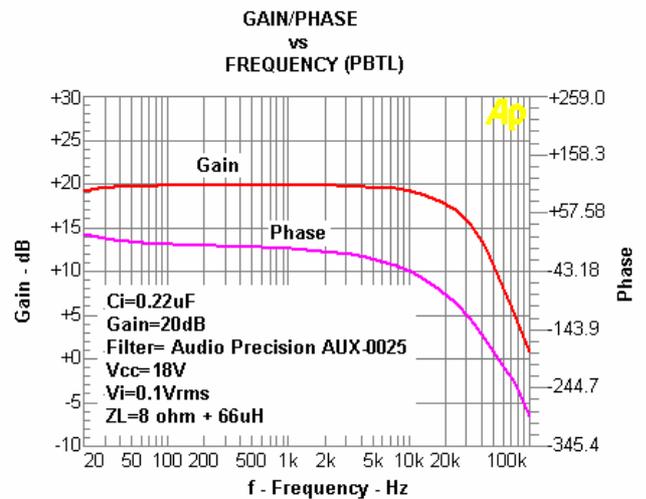


Figure34.

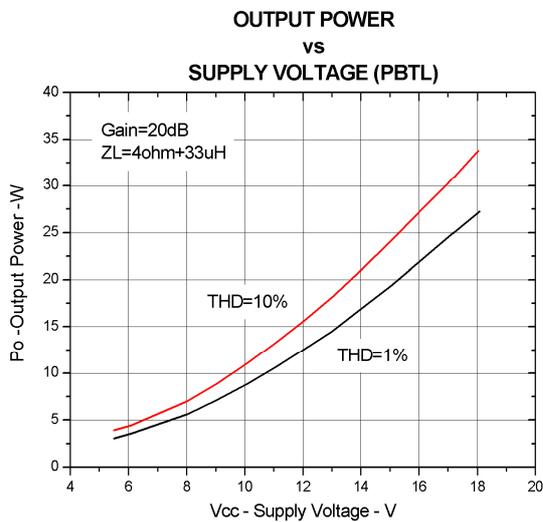


Figure35.

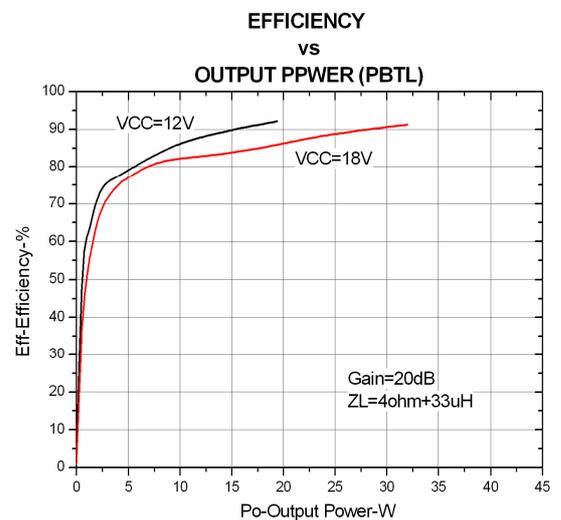


Figure36.

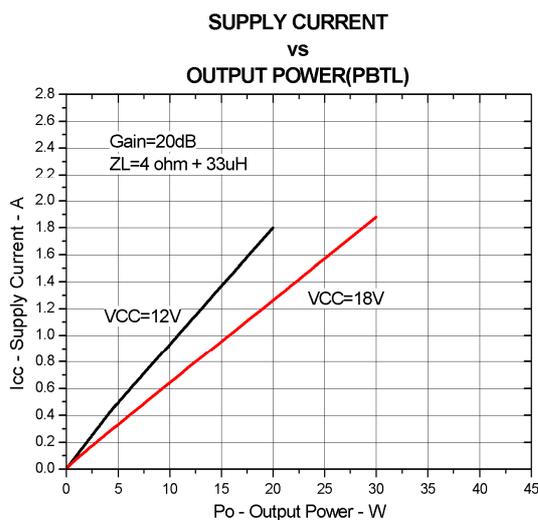


Figure37.

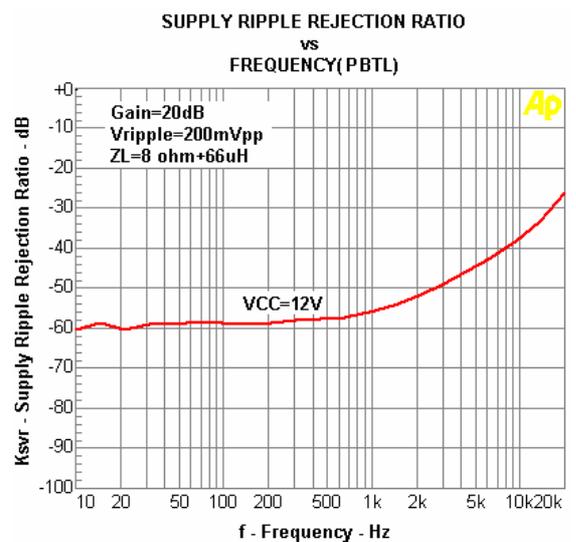
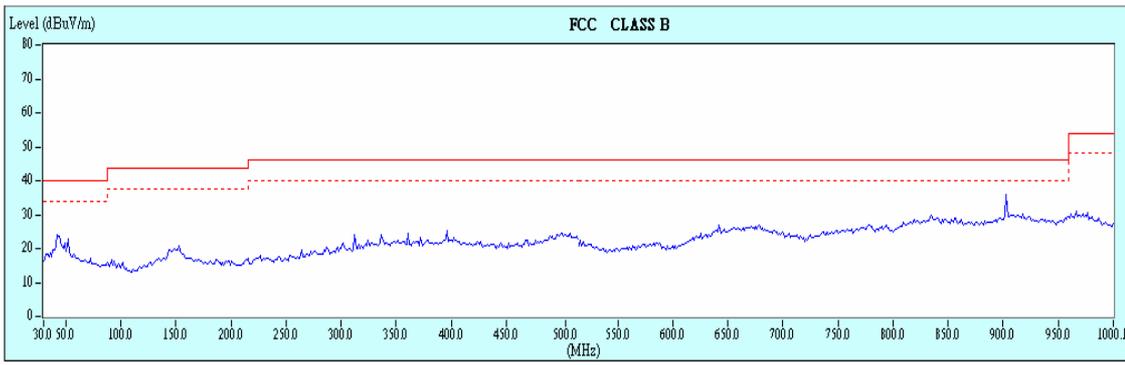


Figure38.



**Figure39. EMI Test and FCC Limits**

## Application Information

### Differential Input

The differential input stage of the amplifier cancels any common-mode noise that appears on both input lines of the audio channel. To use the EUA2310B with a differential source, connect the positive signal of the audio source to the INP pin and the negative signal from the audio source to the INN pin (Figure 40).

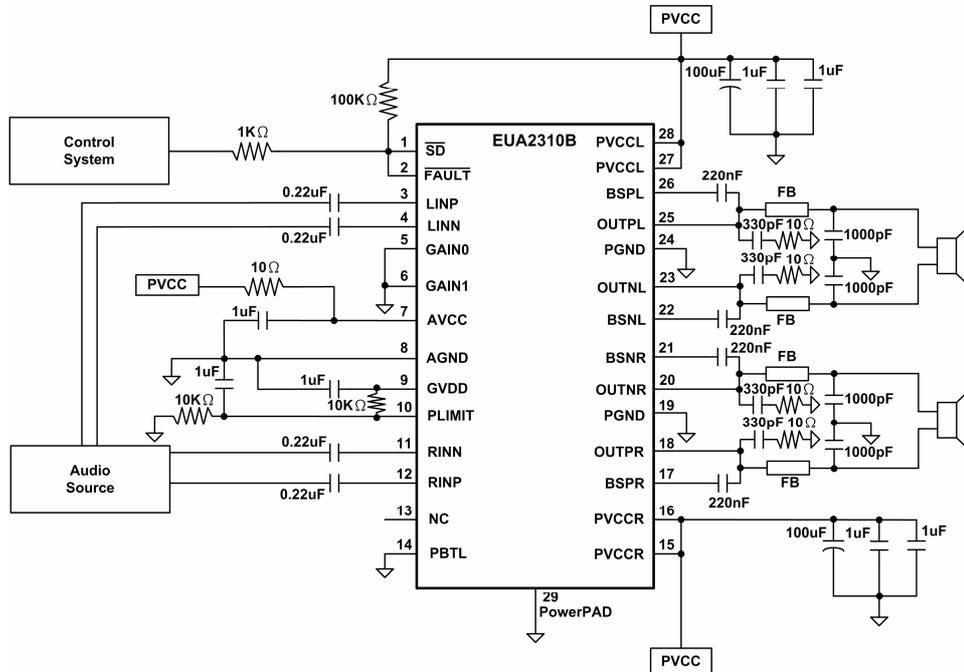


Figure 40. Differential Input

### Single-Ended Input

When using an audio source with a single-ended “out”, it is important to connect the RINN and LINN pins to the GND of the audio source with coupling capacitors. (Figure 41).

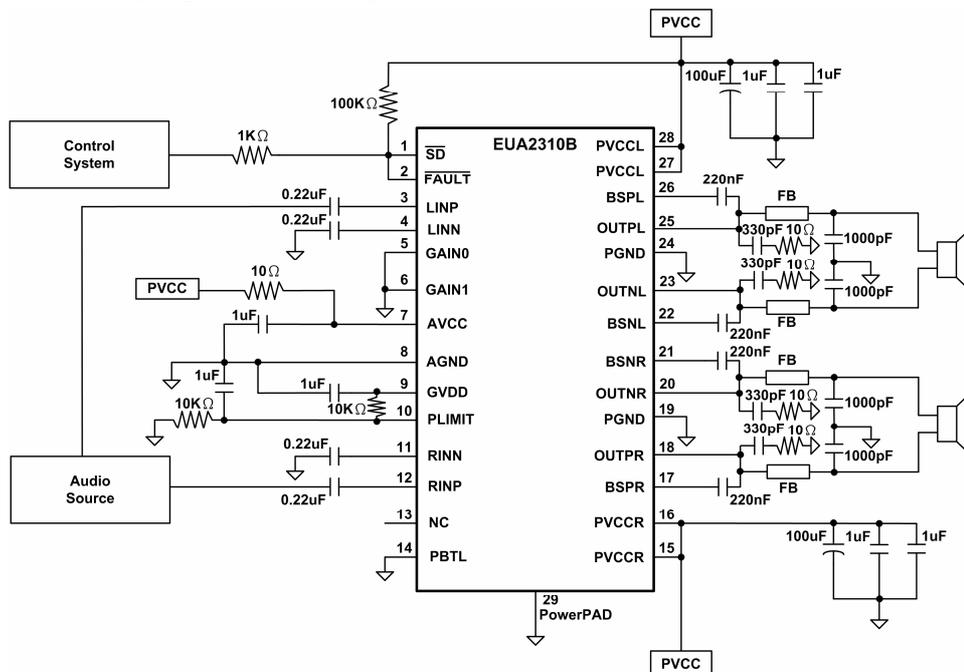


Figure 41. Single Ended Input

## Application Information (continued)

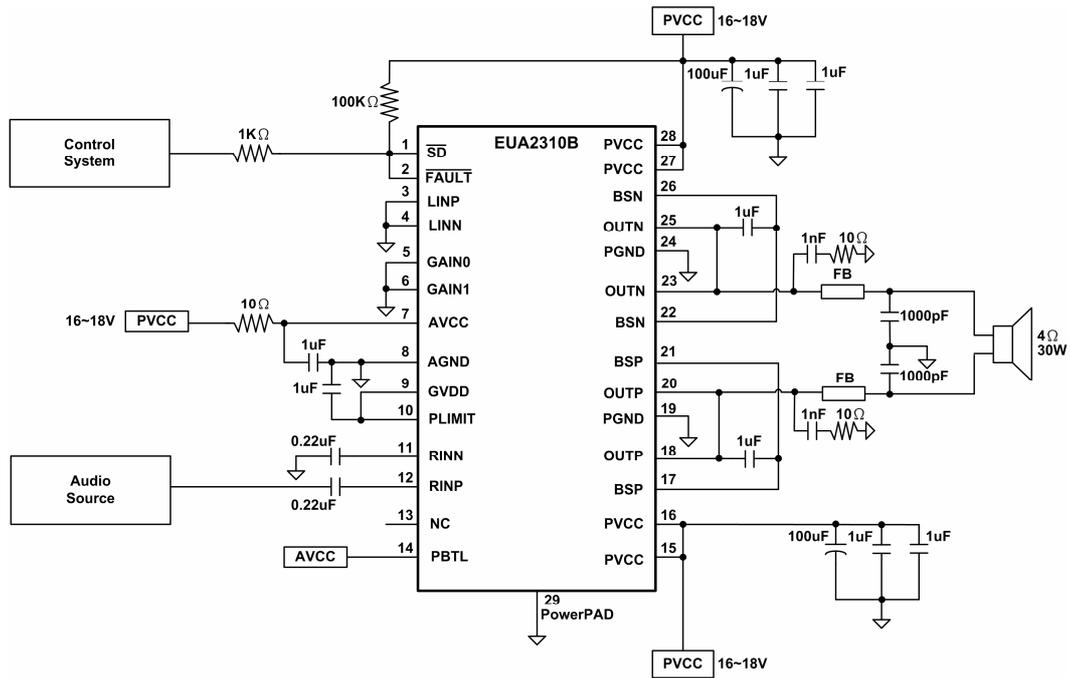


Figure 42. 4Ω/30W PBTL Output

## Gain Selection

The gain of the EUA2310B is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance ( $Z_i$ ) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by  $\pm 20\%$  due to shifts in the actual resistance of the input resistors.

For design purposes, the input network should be designed assuming an input impedance of 40 k $\Omega$ , which is the absolute minimum input impedance of the EUA2310B. At the lower gain settings, the input impedance could increase as high as 120 k $\Omega$ .

**Table.1 Gain Setting**

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (k $\Omega$ )
		TYP	TYP
0	0	20	100
0	1	26	50
1	0	32	50
1	1	36	50

## $\overline{SD}$ Operation

Connect  $\overline{SD}$  to a logic high for normal operation. Pulling  $\overline{SD}$  low causes the outputs to mute and the amplifier to enter a low-current state. Never leave  $\overline{SD}$  unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown prior to removing the power supply voltage.

## PLIMIT Mode Select

The power limit mode is set by the pin 13 NC. The NC pin is default set to logical low and the auto gain control circuit is activated. Connect NC pin to high level for power clamp function.

## PLIMIT

The voltage at pin 10 can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1 $\mu$ F capacitor from pin 10 to ground.

Auto Gain Control circuit is included to limit the output peak-to-peak voltage, by adjusting the gain of the amplifier. The gain changes depending on the amplitude, the PLIMIT level, and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases to suppress the clipped output signal. The Power clamp circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the

duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left( \left( \frac{R_L}{R_L + 2 \times R_S} \right) \times 2 V_P \right)^2}{2 \times R_L} \quad \text{----- (1)}$$

For unclipped power

Where:

$R_S$  is the total series resistance including  $R_{DS(on)}$ , and any resistance in the output filter.

$R_L$  is the load resistance.

$V_P$  is the peak amplitude of the output,  $V_{IN}$  is the input amplitude.

For auto gain control mode:

$$V_P = \begin{cases} 6.5 \times V_{PLIMIT} & \text{If } 0.65 \times V_{PLIMIT} < \frac{V_{INP}}{2} < 2.6 \times V_{PLIMIT} \\ 2.5 \times \frac{V_{INP}}{2} & \text{If } \frac{V_{INP}}{2} > 2.6 \times V_{PLIMIT} \end{cases} \quad \text{----- (2)}$$

For power clamp mode :

$$V_P = 4 \times V_{PLIMIT} \quad \text{if } V_{PLIMIT} < 4 \times V_P \quad \text{----- (3)}$$

$$P_{OUT} (10\% THD) = 1.25 \times P_{OUT} (\text{unclipped})$$

**Table.2 PLIMIT Typical Operation (AGC mode)**

Test Conditions	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude ( $V_{P-P}$ )
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=26dB	4.5	35.2	43.6
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=26dB	1.6	18.4	35.4
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=26dB	1.31	13.1	30
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=26dB	1.01	8.8	25.2
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=26dB	0.102	4.05	17.2
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=20dB	4.5	12.2	29.2
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=20dB	1.2	11.2	28
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=20dB	1.024	8.1	24
PVCC=24V, VIN=1Vrms, RL=8 $\Omega$ , Gain=20dB	0.1	1.05	9.2

**Table.2 PLIMIT Typical Operation (AGC mode)**

Test Conditions	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (V <sub>P-P</sub> )
PVCC=12V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	4.5	9.25	22.8
PVCC=12V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	0.75	4.18	17.6
PVCC=12V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	0.1	1.07	9.4

**Table.3 PLIMIT Typical Operation (Power Clamp mode)**

Test Conditions	PLIMIT Voltage	Output Power (W)	Output Voltage Amplitude (V <sub>P-P</sub> )
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=26dB	4.5	24.5	34.8
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=26dB	1.6	8.51	20
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=26dB	1.31	6.65	17.6
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=26dB	1.01	4.95	15.2
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=26dB	0.102	1.22	8.4
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	4.5	12.1	29.2
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	1.2	4.9	16.4
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	1.024	4.2	15.2
PVCC=24V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	0.1	1.09	8
PVCC=12V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	4.5	9.2	23
PVCC=12V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	0.75	3.1	12.8
PVCC=12V, VIN=1Vrms, R <sub>L</sub> =8Ω, Gain=20dB	0.1	1.05	8

### Auto Gain Control Function

The AGC works by detecting the audio input envelope. The gain changes depending on the amplitude, the power supply level, and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases to suppress the clipped output signal. The maximum attenuation is -12dB. The attack time is 24mSec and the released time is 24mSec per step.

### GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT voltage divider circuit. Add a 1μF capacitor to ground at this pin.

### DC Detect

EUA2310B has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z. To clear the DC Detect it is necessary to cycle the PVCC supply. Cycling SD will NOT clear a DC detect fault.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 20% (for example, +60%, -40%) for more than 420 mSec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

### PBTL Select

EUA2310B offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency. For an example of the PBTL connection, see the schematic in the APPLICATION INFORMATION section.

For normal BTL operation, connect the PBTL pin to local ground.

### Short-Circuit Protection and Automatic Recovery Feature

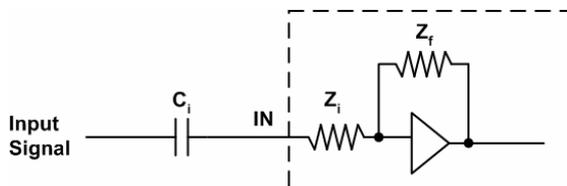
The EUA2310B has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-VCC shorts. When a short circuit is detected on the outputs, the part disables the output drive. A latched fault flag is resulted. The EUA2310B can automatic recover for normal operation if short was removed. If the short was not removed, the protection circuitry again activates.

### Thermal Protection

Thermal protection on the EUA2310B prevents damage to the device when the internal die temperature exceeds 150°C. There is a 10°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. The device begins normal operation at this point with no external system interaction.

## Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 50 kΩ ±20%, to the largest value, 100 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

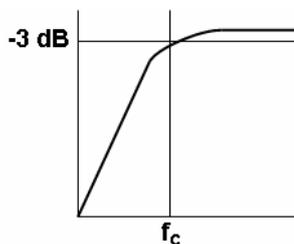


The -3dB frequency can be calculated using Equation 4. Use the Zi values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad \text{----- (4)}$$

## Input Capacitor, Ci

In the typical application, an input capacitor (Ci) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, Ci and the input impedance of the amplifier (Zi) form a high-pass filter with the corner frequency determined in Equation 5.



$$f_c = \frac{1}{2\pi Z_i C_i} \quad \text{----- (5)}$$

The value of Ci is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Zi is 50 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 5 is reconfigured as Equation 6.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad \text{----- (6)}$$

In this example, Ci is 0.16μF; so, one would likely choose a value of 0.22μF as this value is commonly used. If the gain is known and is constant, use Zi from Table 1 to calculate Ci.

## Power Supply Decoupling, Cs

The EUA2310B is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also

prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF to 1μF placed as close as possible to the device VCC lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220μF or greater placed near the audio power amplifier is recommended. The 220μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220μF or larger capacitor should be placed on each PVCC terminal. A 10μF capacitor on the AVCC terminal is adequate.

## BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors, that require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF~1uF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. (See application circuit diagram in Figure 38,39.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

## Using Low-ESR Capacitors

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance. For best performance over the extended temperature range, select X7R capacitors.

## Output Filter

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI-sensitive circuits and/or there are long wires from the amplifier to the speaker.

When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

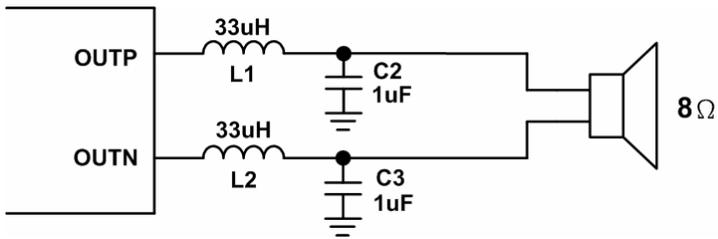


Figure43.

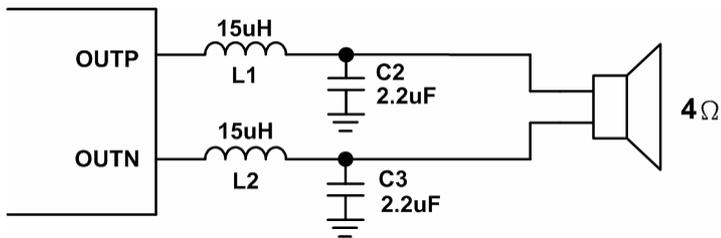


Figure44.

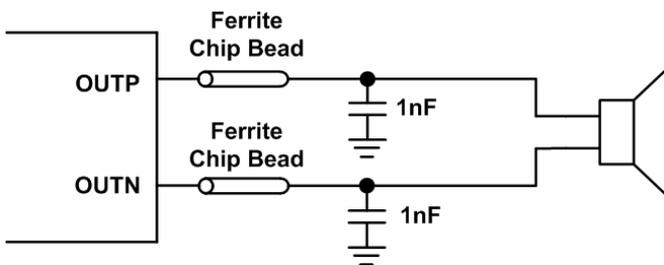
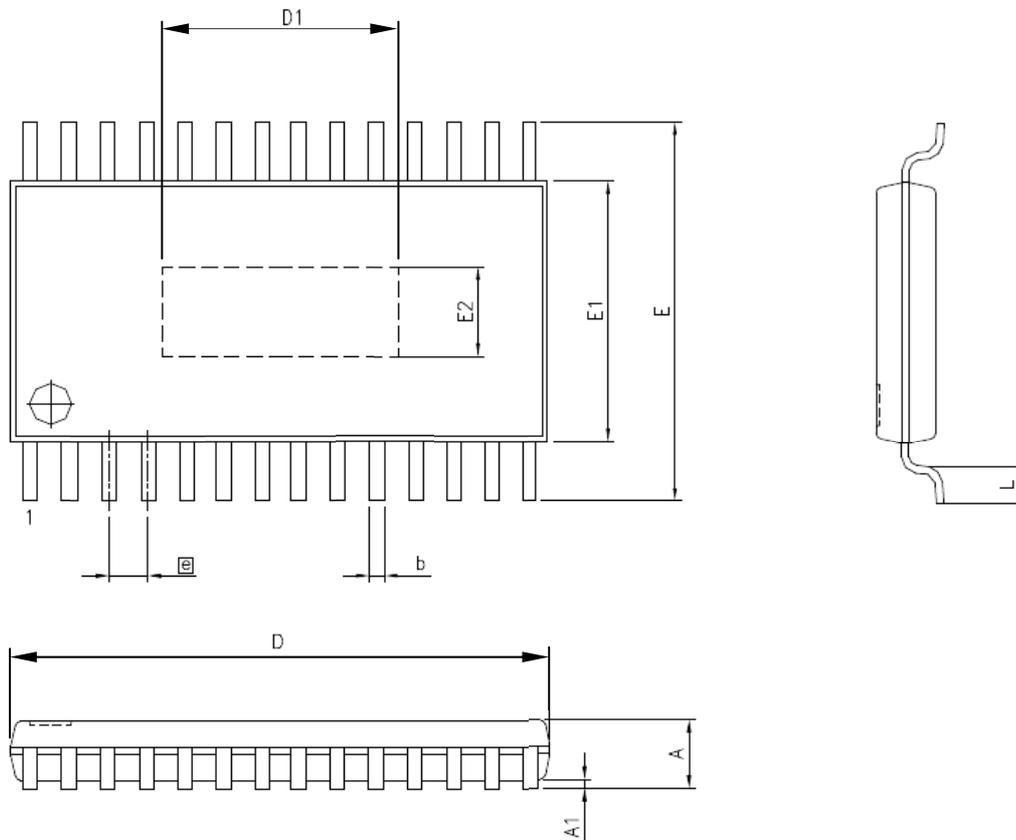


Figure45.

**Package Information****TSSOP-28 (EP)**

Note: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40 REF		0.173 REF	
D	9.60	9.80	0.378	0.386
D1	2.80	6.30	0.110	0.248
E	6.20	6.60	0.244	0.260
E2	2.10	3.30	0.083	0.130
e	0.65 REF		0.026 REF	
L	0.45	0.75	0.018	0.030