SGM62110/SGM62111
2.5A Buck-Boost Converters with I²C Interface

GENERAL DESCRIPTION

The SGM62110 and SGM62111 are 4-switch Buck-Boost converters with programmable I²C interface for simple configuration of integrated rich features. Synchronous rectification improves system efficiency which is friendly for battery operated applications. In addition, the programmable light load PFM (pulse frequency modulation) mode and low quiescent current offer above 90% efficiency in the 10mA to 2A output current range.

The SGM62110 and SGM62111 are capable to regulate the output voltage when the input voltage is below, above or equal to the output voltage. The mode transition is also optimized to ensure smooth operation and reduce output voltage ripple.

Dynamic voltage scaling is enabled via VSEL pin and I²C controlled output voltage registers which allows the device to toggle output voltages based on application needs.

The SGM62110 and SGM62111 implement robust protection features such as over-temperature, input over-voltage and output over-current protections to protect device against unexpected system failure.

The SGM62110 and SGM62111 are available in a small Green WLCSP-2.21×1.40-15B package. High integration provides a compact solution with only four external components, allowing implementation in a PCB area as small as 39mm².

FEATURES

- **2.2V to 5.5V Input Voltage Range**
- **1.8V to 5.2V Output Voltage Range**
  - **2.5A Output Current for V_{IN} ≥ 2.5V, V_{OUT} = 3.3V**
  - **2.5A Output Current for V_{IN} ≥ 2.8V, V_{OUT} = 3.5V**
  - **2A Output Current for V_{IN} ≥ 2.5V, V_{OUT} = 3.5V**
- **3.3V or 3.45V Pre-Programmed Output Voltage (SGM62110)**
- **Programmed Output Voltage Prior to Startup (SGM62111)**
- **Above 90% Efficiency for I_{OUT} from 10mA to 2A**
- **18μA (TYP) Quiescent Current**
- **User-Selectable PFM Mode**
- **Real Buck, Boost and Buck-Boost Modes**
- **Automatic Mode Transition**
- **I²C Interface (Up to 1MHz Clock Speed)**
- **Internal Soft-Start**
- **OTP, Input OVP and Output OCP**
- **True Shutdown Function with Load Disconnect and Active Output Discharge**
- **Available in a Green WLCSP-2.21×1.40-15B Package**

APPLICATIONS

Smartphones and Tablets
Pre-regulators and USB VCONN Supplies
TWS Earbud Chargers
General-Purpose Point-of-Load Regulators

TYPICAL APPLICATION

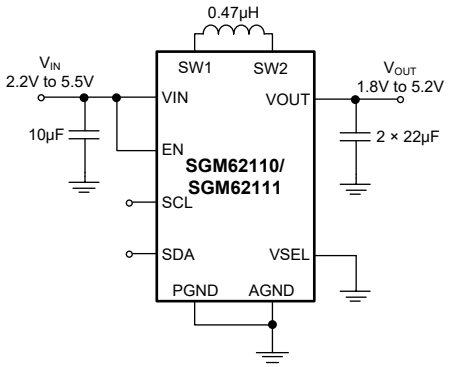


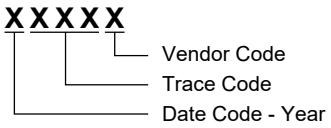
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM62110	WLCSP-2.21×1.40-15B	-40℃ to +85℃	SGM62110YG/TR	62110 XXXXX	Tape and Reel, 3000
SGM62111	WLCSP-2.21×1.40-15B	-40℃ to +85℃	SGM62111YG/TR	62111 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage
VIN, SW1, SW2, VOUT, SCL, SDA, EN, VSEL..... -0.3V to 6V
SW1, SW2 (for Less than 10ns) ..... -3V to 9V
Package Thermal Resistance
WLCSP-2.21×1.40-15B, θ_{JA} ..... 102℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....2500V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .....2.2V to 5.5V
Low Range Output Voltage.....1.8V to 4.975V
High Range Output Voltage.....2.025V to 5.2V
High-Level Input Voltage..... 1.3V to V_{IN}
Low-Level Input Voltage .....0V to 0.3V
EN Voltage..... 0V to V_{IN}
Output Current (1)
V_{OUT} = 3.3V, V_{IN} ≥ 2.5V.....2.5A
V_{OUT} = 3.5V, V_{IN} ≥ 2.5V.....2A
V_{OUT} = 3.5V, V_{IN} ≥ 2.8V.....2.5A
Capacitance at V_{IN} = 2.5V to 5V, V_{OUT} = 3.3V, I_{OUT} = 2.5A
Input Capacitance (2) ..... 5μF (MIN)
Output Capacitance (2) .....16μF (13μF MIN)
Inductance ..... 390nH to 560nH (470nH TYP)
Operating Junction Temperature Range.....-40℃ to +125℃

NOTES:

1. Sustained operation at maximum recommended output current results in the device's junction temperature to exceed the thermal shutdown threshold. Application's ambient temperature range should be tested when the device is expected to operate at maximal output current.

2. DC bias effect has been taken into account.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

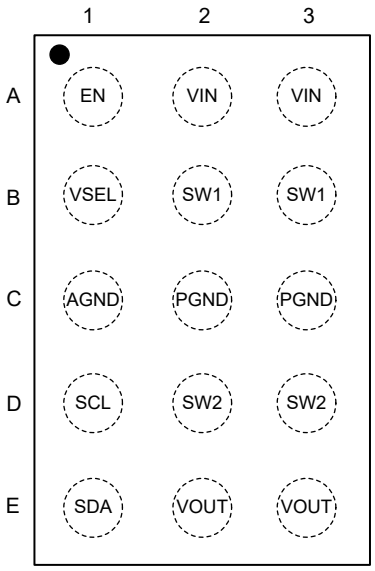
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.21×1.40-15B

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
A1	EN	I	Enable Input Pin. Pulling this pin logic high enables the device, logic low disables the device.
A2, A3	VIN	P	Input Power Supply.
B1	VSEL	I	VOUTx Register Select Pin. VOUT1 register is selected by VSEL = low and VOUT2 register is selected by VSEL = high to set the output voltage.
B2, B3	SW1	P	Buck Switch Node Pin.
C1	AGND	G	Analog Ground Pin. Connect it to the PGND pins under the chip.
C2, C3	PGND	G	Power Ground Pin.
D1	SCL	I/O	I^2C Bus Clock Signal.
D2, D3	SW2	P	Boost Switch Node Pin.
E1	SDA	I/O	I^2C Bus Data Signal.
E2, E3	VOUT	O	Buck-Boost Converter Output Pin.

NOTE: I: input, O: Output, I/O: Input and Output, G: Ground, P: Power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, V_{OUT} = 3.3V, T_J = -40℃ to +125℃ and typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Supply Current into VIN	I_Q	V_{OUT} = V_{EN} = 3.6V, not switching		18		μA
Shutdown Current into VIN	I_{SD}	V_{OUT} = V_{EN} = 0V		0.1		μA
UVLO Rising Threshold Voltage	V_{IT+}		1.95	2.1	2.25	V
UVLO Falling Threshold Voltage	V_{IT-}		1.75	1.9	2.05	V
UVLO Hysteresis Voltage	V_{HYS}			200		mV
I/O Signals						
Logic Voltage Rising Threshold	V_{IH}				1.2	V
Logic Voltage Falling Threshold	V_{IL}		0.4			V
High-Level Input Current	I_{IH}	For SCL, SDA, VSEL, V_{SCL} = V_{SDA} = V_{VSEL} = 1.8V, no pull-up resistor		0.01	0.5	μA
Low-Level Input Current	I_{IL}	For SCL, SDA, VSEL, V_{SCL} = V_{SDA} = V_{VSEL} = 0V, no pull-up resistor		0.01	0.5	μA
Input Bias Current	I_{IB}	V_{EN} = 0V to 5.5V		0.01	1	μA
Power Stage						
Output Voltage Range	V_{OUT}	RANGE = 0	1.8		4.975	V
		RANGE = 1	2.025		5.2	
Output Voltage Accuracy		PWM operation	-1.5		1.5	%
		PFM operation	-1.5		3.5	%
Default Output Voltage	V_{OUT}	RANGE = 0, VSEL = low		3.3		V
		RANGE = 0, VSEL = high		3.45		
Switch Current Limit	I_{LIM}	V_{IN} = 5V, PWM operation, output source current		5.4		A
		V_{IN} = V_{OUT} = 5V, FPWM operation, output sink current		-1.3		
PFM Entry Threshold (Peak) Current	I_{T-_PFM}	V_{IN} = 4.2V		0.9		A
Output Discharge Current	I_{DIS}	V_{OUT} ≥ 0.8V	35			mA
Output Voltage Rising Power-Good Threshold	V_{T+}			95		%
Output Voltage Falling Power-Good Threshold	V_{T-}			90		%
VIN Rising Over-Voltage Threshold				5.7		V
I²C Interface						
7-Bit Slave Address				75		h
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	T_J rising		150		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

TIMING REQUIREMENTS

(Over operating junction temperature range and recommended supply voltage range, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
SCL Clock LOW Period	t_{LOW}	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus	0.5			
SCL Clock HIGH Period	t_{HIGH}	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Bus Free Time between a STOP and a START Conditions	t_{BUF}	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus	0.5			
Setup Time for a Repeated START Condition	$t_{SU,STA}$	Standard mode	4.7			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Hold Time (Repeated) START Condition	$t_{HD,STA}$	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Data Setup Time	$t_{SU,DAT}$	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
Data Hold Time	$t_{HD,DAT}$	Standard mode	0			μs
		Fast mode	0			
		Fast mode plus	0			
Rise Time of SDA and SCL Signals	t_R	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
Fall Time of SDA and SCL Signals	t_F	Standard mode			300	ns
		Fast mode	$20 \times V_{DD}/5.5$		300	
		Fast mode plus	$20 \times V_{DD}/5.5$		120	
Setup Time for STOP Condition	$t_{SU,STO}$	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
Data Valid Time	$t_{VD,DAT}$	Standard mode			3.45	μs
		Fast mode			0.9	
		Fast mode plus			0.45	
Data Valid Acknowledge Time	$t_{VD,ACK}$	Standard mode			3.45	μs
		Fast mode			0.9	
		Fast mode plus			0.45	
Capacitive Load on Each Bus Line	C_B	Standard mode			400	pF
		Fast mode			400	
		Fast mode plus			550	
VSEL Pulse Duration	t_{w_VSEL}	VSEL = high or low	5			μs

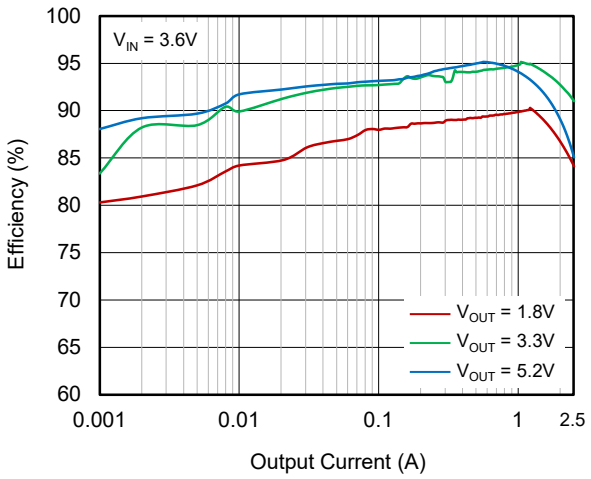
SWITCHING CHARACTERISTICS

(V_{IN} = 3.6V, V_{OUT} = 3.3V and T_J = +25℃, unless otherwise noted.)

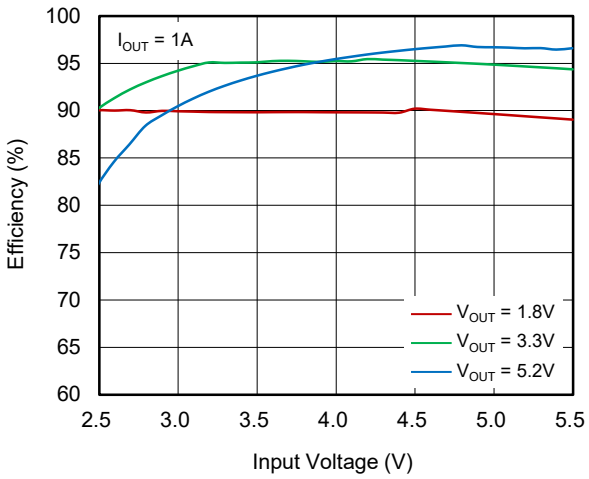
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Rising Edge to Output Ramp Start Delay	t_{D_EN}	T_J = +25℃, V_{IN} = 3.6V		229		μs
Power-Good Delay	t_{D_PG}	V_{OUT} falling		50		μs
Slew Rate of Internal Ramp during Dynamic Voltage Scaling	SR	SLEW[1:0] = 00, FPWM operation		±1		V/ms
		SLEW[1:0] = 01, FPWM operation		±2.5		
		SLEW[1:0] = 10, FPWM operation		±5		
		SLEW[1:0] = 11, FPWM operation		±10		
Switching Frequency	f_{SW}	PWM operation, I_{OUT} = 100mA		3		MHz
VSEL Rising Edge to DVS Ramp Start Delay	t_{D_VSEL}	Measured from rising edge of VSEL to the start of the ramp in Dynamic Voltage Scaling			5	μs

TYPICAL PERFORMANCE CHARACTERISTICS

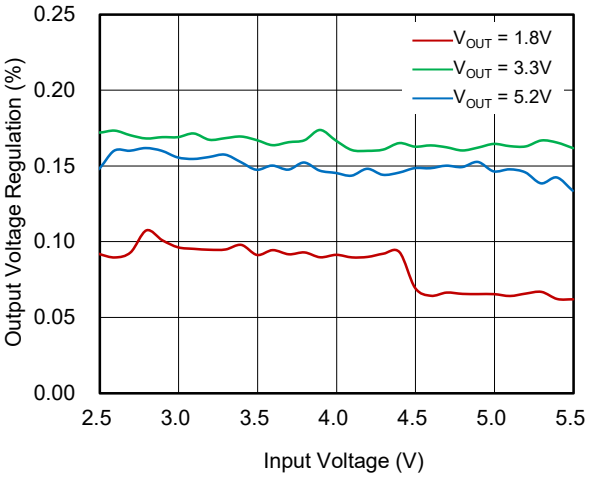
Efficiency vs. Output Current



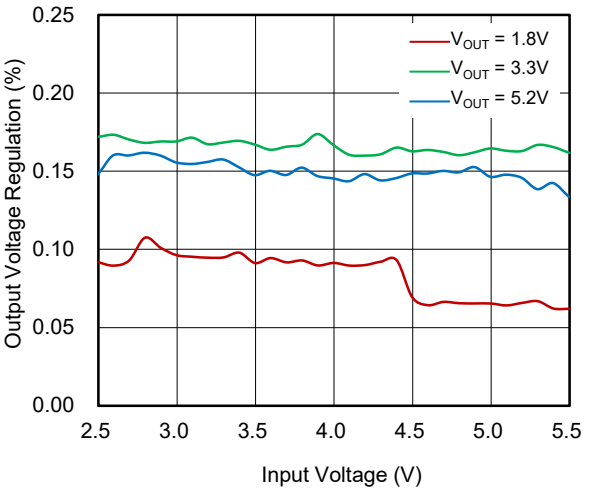
Efficiency vs. Input Voltage



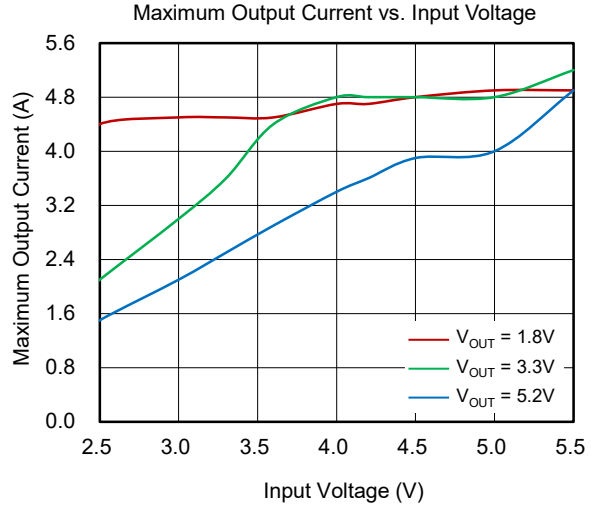
Load Regulation under PFM



Line Regulation



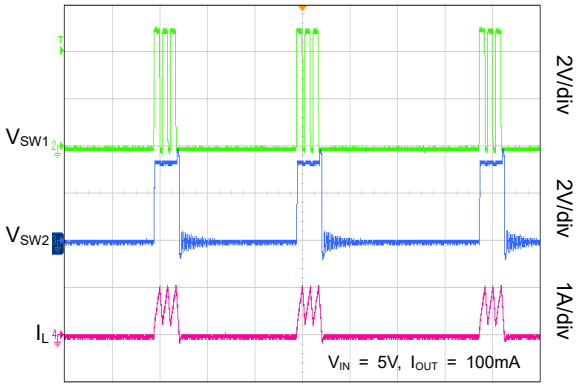
Maximum Output Current vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

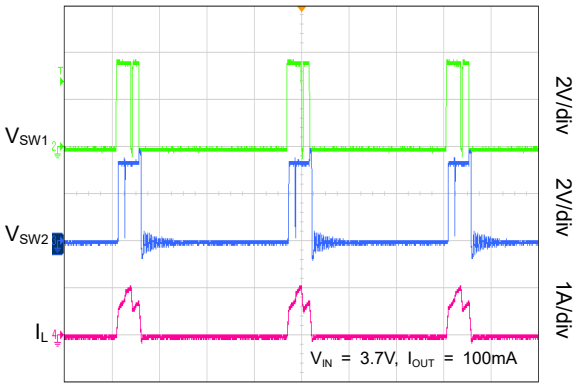
V_{OUT} = 3.3V, T_J = +25℃, unless otherwise noted.

PFM Switching Waveforms in Buck Mode



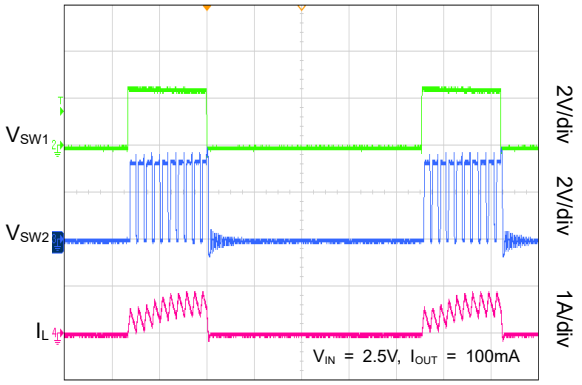
Time (2μs/div)

PFM Switching Waveforms in Buck-Boost Mode



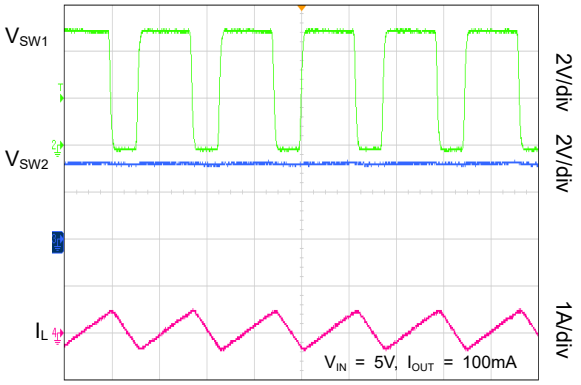
Time (2μs/div)

PFM Switching Waveforms in Boost Mode



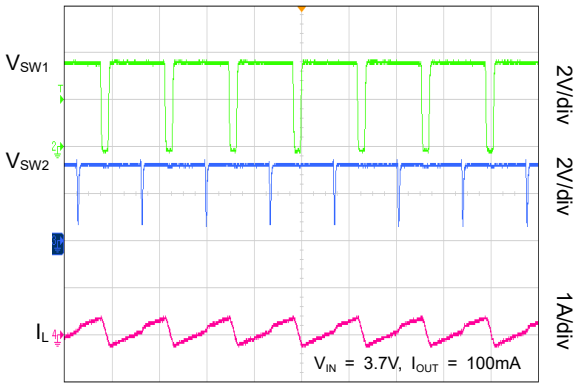
Time (2μs/div)

FPWM Switching Waveforms in Buck Mode



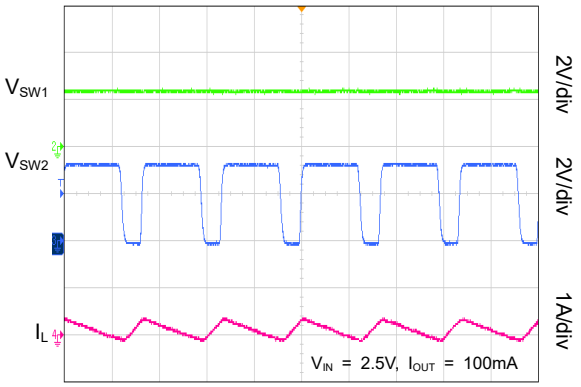
Time (200ns/div)

FPWM Switching Waveforms in Buck-Boost Mode



Time (500ns/div)

FPWM Switching Waveforms in Boost Mode

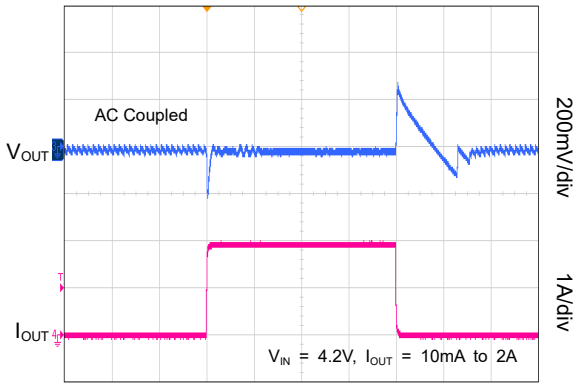


Time (200ns/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

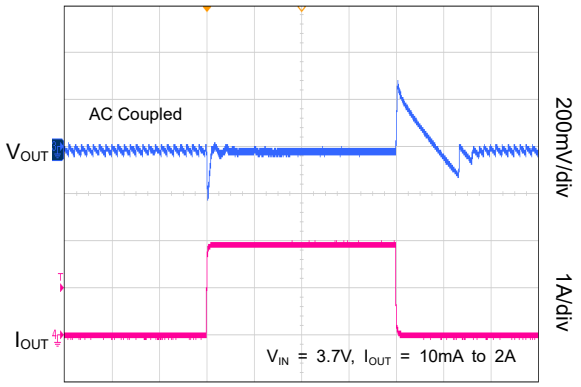
V_{OUT} = 3.3V, T_J = +25℃, unless otherwise noted.

Load Transient Response in Buck Mode



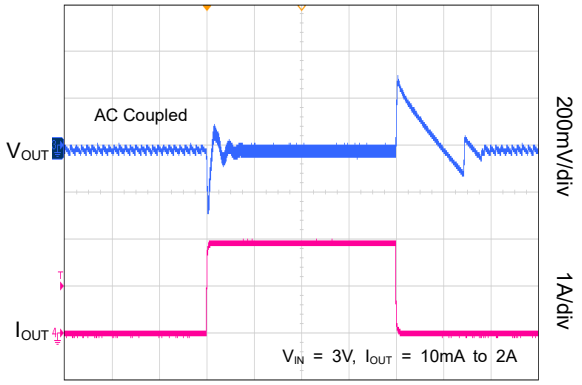
Time (200μs/div)

Load Transient Response in Buck-Boost Mode



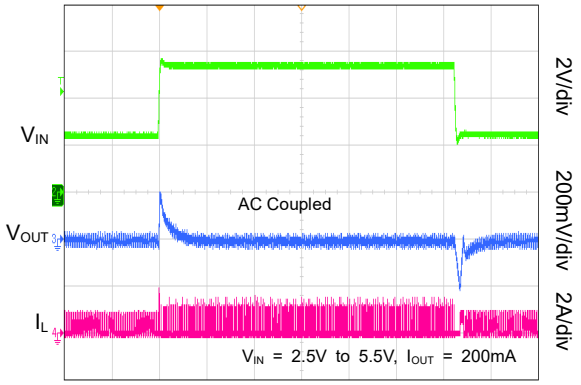
Time (200μs/div)

Load Transient Response in Boost Mode



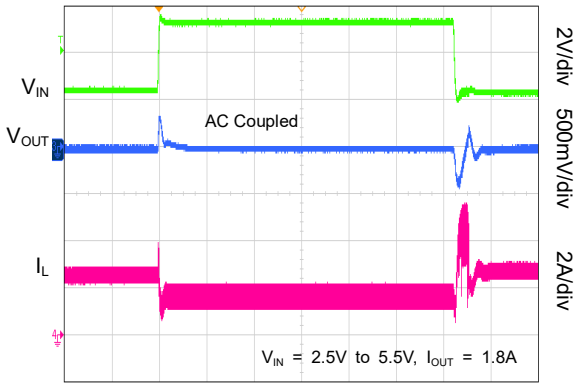
Time (200μs/div)

Line Transient Response



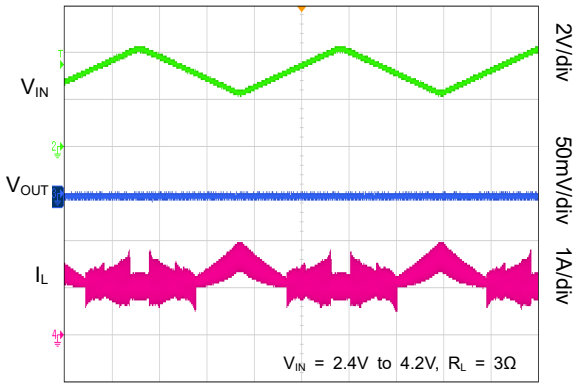
Time (200μs/div)

Line Transient Response



Time (200μs/div)

Line Sweep under PFM

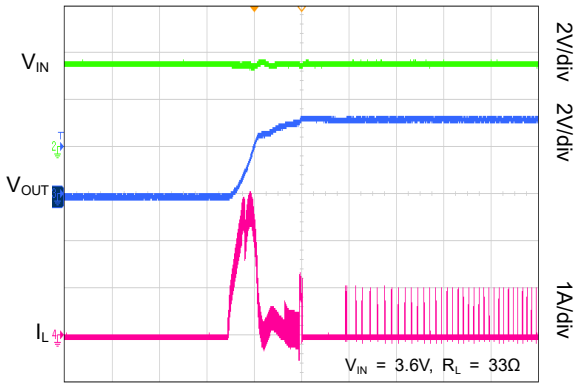


Time (500ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

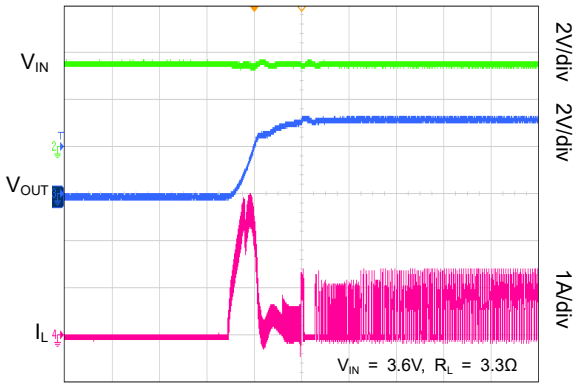
V_{OUT} = 3.3V, T_J = +25℃, unless otherwise noted.

Startup under Light Load



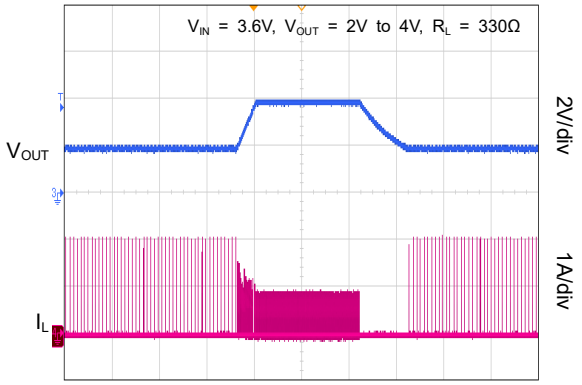
Time (100μs/div)

Startup under Heavy Load



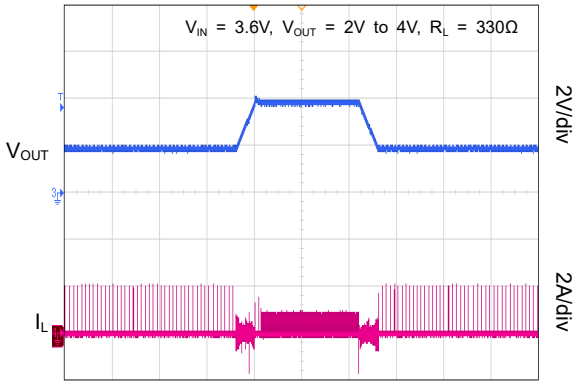
Time (100μs/div)

Dynamic Voltage Scaling under PFM



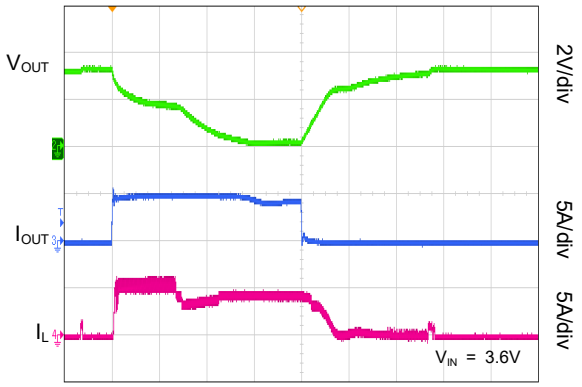
Time (5ms/div)

Dynamic Voltage Scaling under FPWM



Time (5ms/div)

Over-Current Protection



Time (50μs/div)

FUNCTIONAL BLOCK DIAGRAM

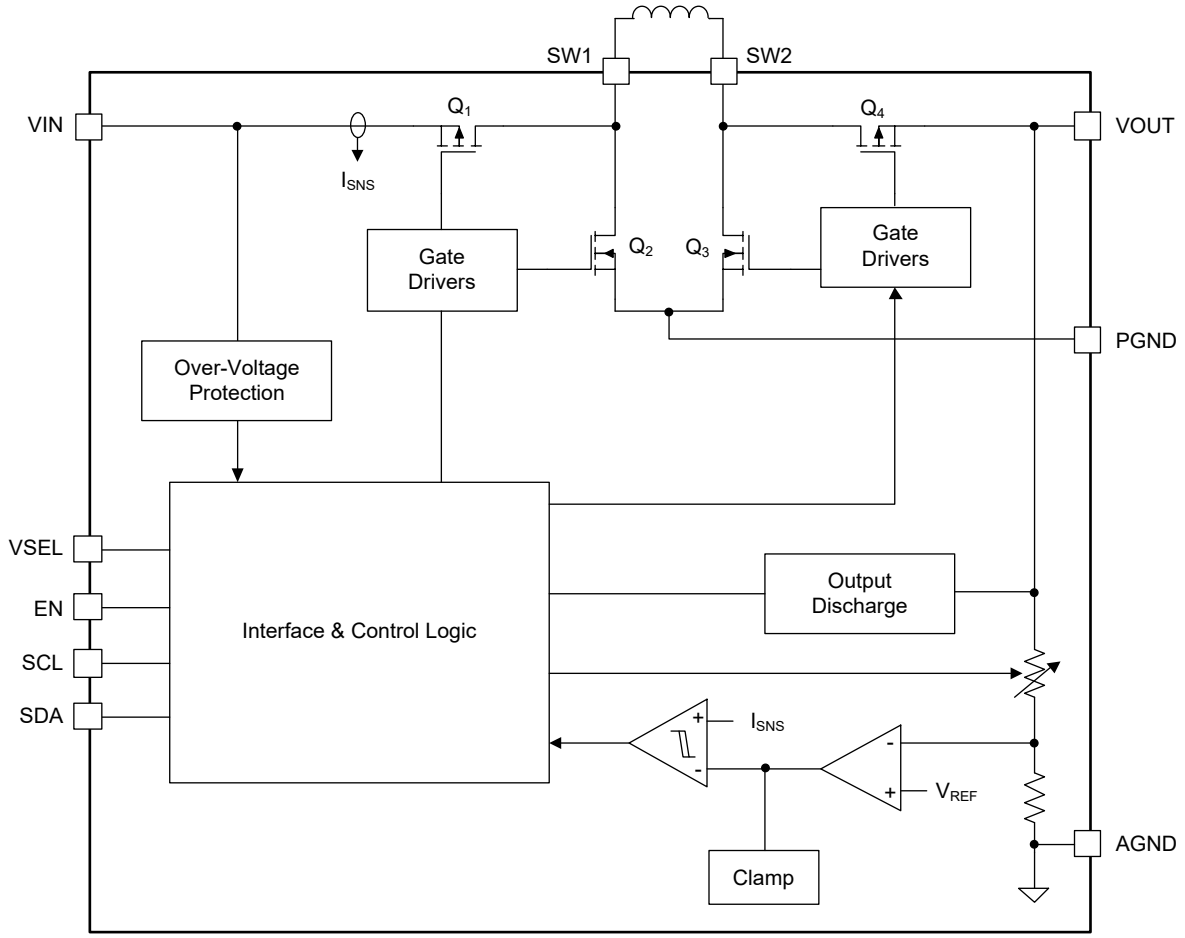


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM62110 and SGM62111 are synchronous Buck-Boost converters with integrated switches that can operate over a wide input voltage and output current range with high efficiency. Both devices are capable to change mode automatically among Buck, Boost and Buck-Boost depending on the input and output condition. When $V_{IN} > V_{OUT} + 0.7V$, the devices is in Buck mode, When $V_{IN} \leq V_{OUT}$, the device is in Boost mode, and When $V_{OUT} < V_{IN} < (V_{OUT} + 0.7V)$, the device is in 4-cycle Buck-Boost mode. In the Buck-Boost mode, the 4-cycle operation controls the four switches to turn on/off alternately to reduce the RMS current in the inductor and output capacitors to maintain low output voltage ripple and achieve high efficiency across entire input voltage range.

Mode Toggle

The SGM62110 and SGM62111 automatically select the operation mode based on the input and output voltages.

Buck Mode

When $V_{IN} > V_{OUT} + 0.7V$, the device operates as a Buck converter as shown in Figure 3. Q_1 is the control switch, Q_2 is the synchronous rectifier, Q_3 is off and Q_4 is always on. In Buck mode, each switching cycle has two phases (switch on and off). Note that Q_1 and Q_4 are P-channel MOSFETs, which eliminates the need for external boot-strap capacitors.

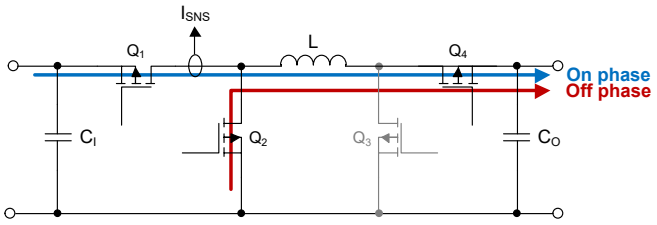


Figure 3. Buck Mode Switching

Boost Mode

If $V_{IN} \leq V_{OUT}$, the device operates as a Boost converter (see Figure 4). In the Boost mode, Q_1 is always on, Q_2 is off, Q_3 is the control switch, and Q_4 acts as the synchronous rectifier. Each cycle has two phases (switch on and off).

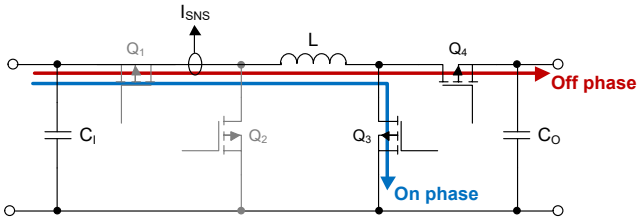


Figure 4. Boost Mode Switching

Buck-Boost Mode

When $V_{OUT} < V_{IN} < (V_{OUT} + 0.7V)$, all four switches are controlled in a continuously on manner. The internal control loop controls all 4 switches adaptively based on the load, input voltage and output voltage. The inductor current is regulated to ensure output voltage regulation and load current delivery.

Control Scheme

The SGM62110 and SGM62111 employ peak current mode control scheme. The error amplifier (EA) output of the output voltage loop sets the desired current loop threshold for PWM duty cycle control as well as modes of operation. The on phase is terminated and the next phase(s) of the switching cycle will start if the sensed peak inductor current (I_{LM}) reaches the reference signal from the error amplifier.

The off-time is a function of V_{IN} and V_{OUT} and the Buck, Boost or Buck-Boost operating mode of the converter.

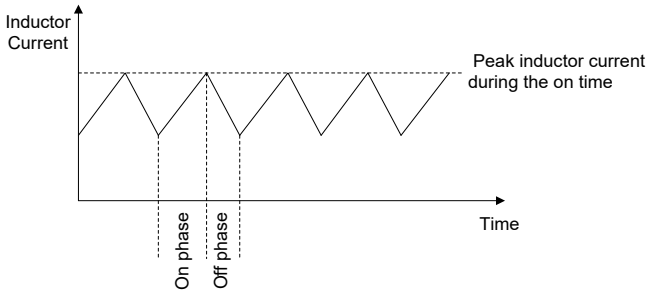


Figure 5. Buck or Boost Modes Peak Current Control

DETAILED DESCRIPTION (continued)

When the forced PWM (FPWM) mode is configured in the control register, the SGM62110 and SGM62111 remain in continuous conduction mode even if the inductor current is negative, which causes current to flow in the reversed direction. During the negative current phase, the error amplifier will provide a negative current threshold (-1.3A, TYP) for the inner current loop which causes the inductor's average current in reversed direction to become more negative. Therefore, as shown in Figure 6, smaller current limit levels must be used for the reverse current.

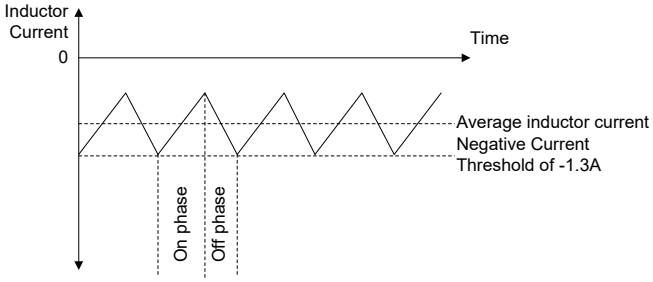


Figure 6. Buck or Boost Mode Reverse Peak Current Control

Power-Save Mode (PSM)

During startup, the device will force to operate in PSM mode until power-good status is reached for the first time. The default value for FPWM bit is 0 for PSM mode.

When PSM mode is configured, in medium to heavy load condition, the SGM62110 and SGM62111 operate in the continuous current mode with constant switching frequency mode. To improve the efficiency at light load condition, the device switches to the pulse frequency modulation (PFM) mode. In the PFM mode, a sequence of burst switching cycles occurs to maintain the output voltage followed by an off period as shown in Figure 7.

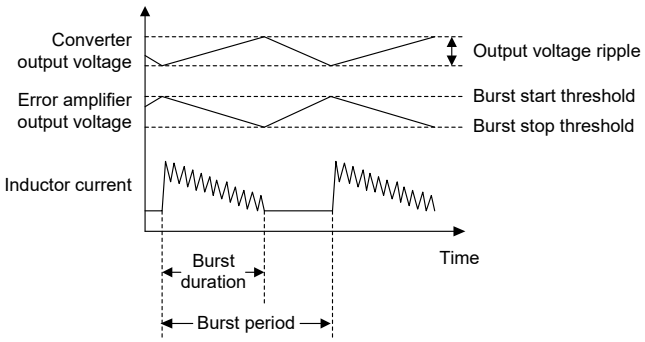


Figure 7. PFM Mode

The burst sequence is issued when the output of the error amplifier exceeds the PFM threshold voltage. The device dynamically adjusts the burst mode switching frequency based on the load to ensure the output voltage regulation accuracy.

In PFM mode, switching loss is reduced due to the reduced switching cycles. Some of the internal blocks are turned off in PFM mode to further improve the light load efficiency, however, output voltage ripple, DC output voltage accuracy and load transient performance are reduced in PFM mode (see Table 1).

Table 1. Comparison of the FPWM and PFM Performances

Parameter	Best Operating Mode
Low-Power Efficiency	PFM
DC Output Voltage Accuracy	FPWM
Transient Response	FPWM
Output Voltage Ripple	FPWM

Forced PWM Operation (FPWM)

Force PWM mode is enabled via setting the FPWM bit to 1 in the control register. In the FPWM mode, in light load condition, the synchronous switches are not turned off when the inductor current goes negative to maintain a constant switching frequency. FPWM operation has lower output voltage ripple and better transient response compared to PFM. However, in the lower output currents, FPWM results in higher switching and conduction loss thus lower efficiency.

DETAILED DESCRIPTION (continued)

Ramp PWM Operation (RPWM)

Ramp PWM mode is configured via the RPWM bit and programs the device to operate in FPWM mode when the output ramps from one voltage to another. In light load condition and PFM mode is configured, when ramping from a higher voltage to a lower voltage, load cannot sink enough current to discharge the output capacitors. It is recommended to enable RPWM bit to control the output voltage ramp down in a controlled manner.

Set the RPWM bit in the control register to enable RPWM operation.

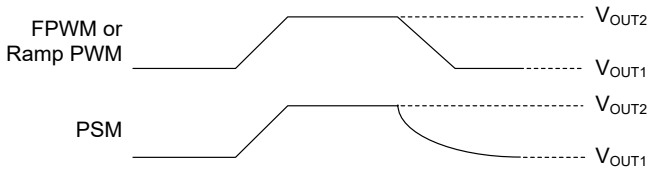


Figure 8. RPWM Operation

Device Enable (EN)

There are two ways to enable the SGM62110 and SGM62111, one is to apply a logic high signal on the EN pin, and the other is to configure the ENABLE bit via I²C. The truth table is shown in Table 2.

Table 2. Enable Truth Table

EN Pin	ENABLE Bit	Device State	Output State
0	×	Device in Shutdown	Output Discharge Active
1	0	Programming Interface Active	Output Discharge Active
1	1	Device Active	Output Enabled

Under-Voltage Lockout (UVLO)

The under-voltage lockout feature disables the device when the input supply voltage is too low to prevent device malfunction.

Soft-Start

During startup, the built-in soft-start function will minimize the inrush current and limit the output voltage overshoot. When the device is turned on or enabled, the switch current limit is increased gradually to the maximum to prevent large input currents at startup. With the gradual increase of the current limit, the inrush current for no-load conditions is minimized while it is still possible to start into heavy loads (as long as the load is within the device current limit).

The output voltage rise time depends on the application and operating conditions. V_{OUT} rise time will increase if the output capacitance and load are large or if the device operates in Boost mode. More information can be found in the Application Information section.

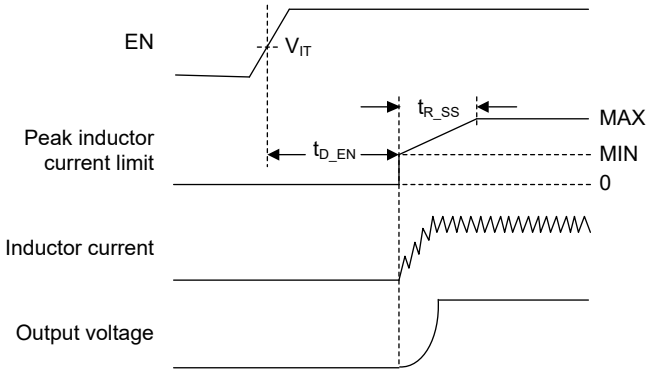


Figure 9. Startup Performance

Output Voltage Control

The device output voltage can be programmed between 1.8V to 5.2V with a resolution of 25mV.

The RANGE bit in the control register is used to select the output voltage range.

When RANGE = 0, the output voltage is programmed from 1.8V to 4.975V. When RANGE = 1, the output voltage is programmed from 2.025V to 5.2V.

The VSEL pin selects the VOUTx register used to set the output voltage. The 7-bit value of the selected VOUT1[6:0] and VOUT2[6:0] registers determine the output value as follows:

When RANGE = 0, V_{OUT} = VOUTx[6:0] × 0.025 + 1.8V. When RANGE = 1, V_{OUT} = VOUTx[6:0] × 0.025 + 2.025V

Logic low on VSEL pin corresponds to VOUT1 register setting, while logic high on VSEL pin corresponds to VOUT2 register setting.

DETAILED DESCRIPTION (continued)

Dynamic Voltage Scaling (DVS)

Dynamic voltage scaling (DVS) allows changing of the output voltage with a controlled rate. Figure 10 explains the DVS function. The ramp control block changes the output voltage towards the target value in 25mV steps. The 2-bit SLEW[1:0] parameter in the control register is used to choose one of the four slew rate values of 1, 2, 2.5 and 10V/ms.

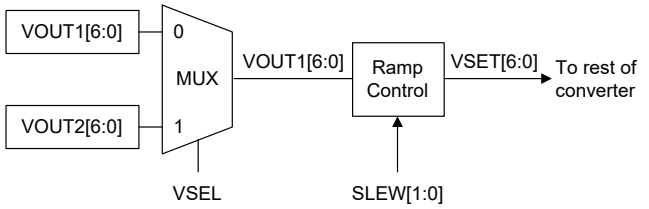


Figure 10. Block Diagram of the Dynamic Voltage Scaling

A DVS ramp is started when the VSEL logic level is changed or a new value is written in the active VOUTx register. Note that if these changes occur during the startup (before the end of the soft-start and achieving the first power-good), the new value will take effect immediately, and the V_{OUT} will change to the final value without gradual ramp.

DVS timing initiated by a VSEL logic change is shown in Figure 11. Figure 12 shows the same timing when an I^2C write is used to change the output voltage in the active VOUTx registers (VOUT1 in this example).

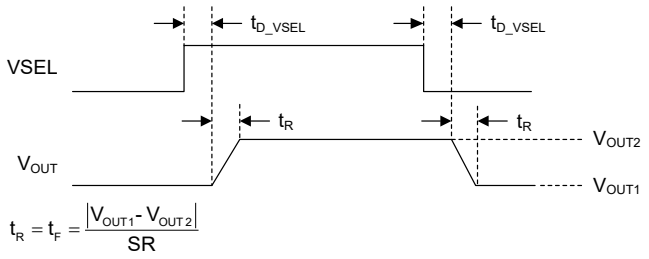


Figure 11. DVS Timing Diagram Initiated by a VSEL Change

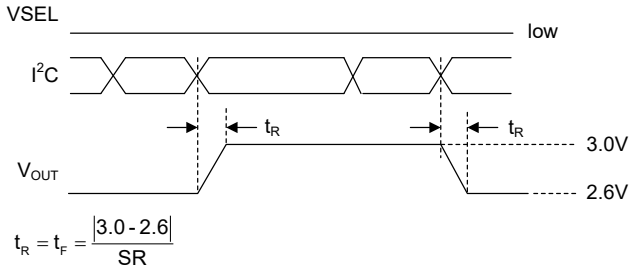


Figure 12. DVS Timing Initiated by a Write to the VOUT1 Register by I^2C

Input Voltage Protection (IVP)

When the output ramps down to a lower voltage by DVS, the current can flow from the device output back to the input, especially in light load condition. While the load does not sink enough current to discharge the output capacitors, the only path for the current released by the output capacitors will flow back to the input. This behavior can charge the input capacitor's voltage and cause the V_{IN} to rise in an uncontrolled manner. If the converter is operating in Buck mode, a rapid VOUT change to a lower voltage in forced PWM mode, the reverses current flow causes the converter to act as a Boost from output to the input temporarily.

The SGM62110 and SGM62111 provide IVP feature to ensure the voltage present on VIN pin never exceed higher than 5.7V during any conditions. Switching is immediately terminated when IVP is triggered and resumes automatically when the condition is removed. The PG bit is also set to 1 when the IVP is triggered, and the bit is cleared when the IVP condition is ended.

Current Limiting Protection

The device implements peak inductor current limit to protect the device in an overload condition. Overload usually results in higher power dissipation and increases junction temperature (T_J) in the device which will cause device shutdown triggered by the over-temperature protection.

DETAILED DESCRIPTION (continued)

Thermal Shutdown

If the junction temperature exceeds the +150℃ threshold, the converter will turn off (OTP) to protect the device. The device will automatically resume operation when T_J falls below +130℃. Note that the automatic recovery can result in a cyclic turn on and turn off if a permanent overload condition causes the OTP. Because after each shutdown, the device cools down and restarts operating. The I^2C interface is functional even when the device is shut down due to OTP. If an over-temperature is detected, the TSD bit in the status register will be set to 1. This bit will be cleared if it is read by I^2C when T_J is less than +130℃.

Power-Good

The SGM62110 and SGM62111 offer power-good function via the status register (02h) with active low logic. When the output voltage reaches above 95% of the programmed output voltage, the power-good bit toggles to logic low. When the output voltage falls below 90% of the programmed voltage, the power-good bit toggles to logic high, indicating that a power-not-good event has occurred.

Load Disconnect in Shutdown

When the device is shutdown, the Input and output are disconnected, blocking any current flow between the input and output of the device.

Output Discharge

When a logic low is applied to the EN pin or ENABLE bit is set to 0, the VOUT will be pulled to ground actively to discharge the output. This feature is beneficial for systems requiring strict power-down sequence.

Device Functional Modes

On and off functional modes are defined for the device. If V_{IN} is above the UVLO threshold and EN pin is pulled high, the device mode is on. It will enter into the off mode if a UVLO occurs or if EN is pulled low.

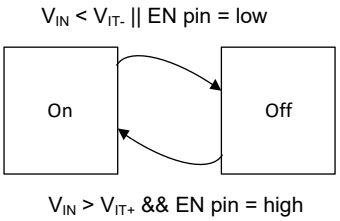


Figure 13. On and Off Functional Modes

I^2C Serial Interface and Programming

I^2C is a widely used 2-wire, bi-directional serial communication interface. It is used for the SGM62110 and SGM62111 to support I^2C communication for parameter programming, receiving and reporting device status. The use of I^2C significantly improves the design flexibility because most of the device functions can be programmed and adapted to the application requirements.

The I^2C bus uses two open-drain lines called serial data (SDA) and serial clock (SCL) for communication. The SDA and SCL pins must be pulled up to the bus high voltage by a current source or pull-up resistors. All devices connected to the bus have their own addresses (7-bit) and each may act as a master or slave during a data transfer. The master is usually a processor or another host device that initiates a data transfer and generates the clock signals to allow transmission of the data bit. Any device that is addressed in a transfer sequence is considered as a slave. For more details about I^2C refer to the “UM10204: I^2C-bus specification and user manual, revision 6”.

The SGM62110 and SGM62111 are slave devices with 75h (1110101b) address and only support 7-bit addressing and not 10-bit address or the general call address. The device supports standard-mode (100kbps), fast-mode (400kbps) and fast-mode plus (1Mbps) data transfer speeds. Each device has five 8-bit registers with individual internal addresses that can be read or written (except the read-only bits) by a host. See the Register Map section for details. The register contents remain intact if V_{IN} remains higher than 2.1V. The data transfer protocol for the standard and fast speed modes are the same.

DETAILED DESCRIPTION (continued)

START and STOP Conditions (For All Modes)

In the idle state condition, both SDA and SCL line are high. A transaction is initiated by a master who takes the control of the bus when it is free (idle) by sending a START or S condition to initiate the exchange of data as shown in Figure 14. When the data transfer job is done, the master sends one (or more) STOP or P conditions to terminate the transaction and releases the bus. To ensure that the bus is properly reset after bus power up, it is recommended to initiate the bus by sending a STOP condition after power up.

A START condition is generated by pulling SDA from high to low when SCL is high. START is detected by all devices on the bus. Similarly, a STOP is applied on the bus by pulling SDA from low to high when SCL is high. The START and STOP conditions are always generated by a master. After a START and before a STOP the bus is considered busy. The master may not release the bus after a complete transaction with the slave and send a repeated START to initiate a new data exchange with the slave.

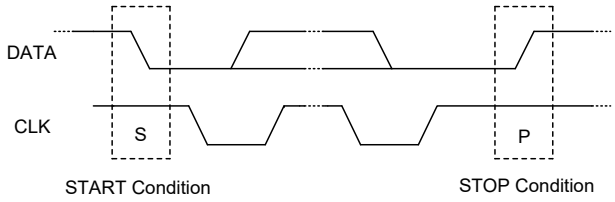


Figure 14. START and STOP Conditions

Data Bit Transmission and Validity

During a transaction all data bit (high or low) must remain stable on the SDA line during SCL = H period. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by the master. Bit transferring procedure is shown in Figure 15.

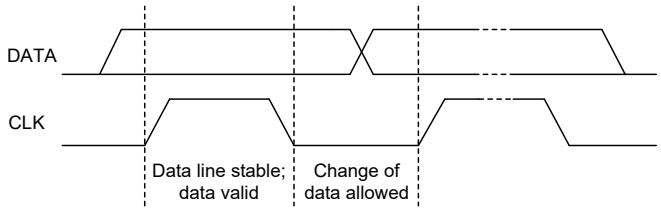


Figure 15. Bit Transfer on the Serial Interface

I²C Data Format

The data is transmitted one byte at a time. After detecting the START condition, the transmitter will send one byte (8-bit) of data, bit by bit, starting from the most significant bit (MSB), with each SCL pulse placing a new bit on the SDA line. After sending the 8th bit, the transmitter releases the SDA line during the 9th SCL pulse in order to receive an acknowledgement bit from the receiver. Therefore, a total of 9 bits is exchanged for each byte. The number of bytes in one transaction is not limited. After sending the ACK bit, if the receiver is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the sender in wait state (clock stretching). When it is ready for another byte of data, it releases the clock line and the data transfer can continue with clocks generated by the master.

The 9th bit is the receiver response (slave or master) to show that the byte is received. Sending a low signal during the 9th clock cycle is interpreted as ACK. If the receiver responds a high or does not respond at all, the sender will receive a high for the 9th bit that is considered as not ACK, called NCK. An NCK means that the receiver does not expect more data. Therefore, the response of the receiver to the last byte in a transaction is an NCK. It also shows that there is a problem in the communication link (rare). After the 9th bit, a STOP or a repeated START should be sent by master. Figure 16 and Figure 17 show the byte transfer and acknowledgment procedures of the I²C interface.

I²C Data Communication Protocol

After power up, it is recommended to send a STOP condition by the host to assure all I²C slaves are reset and ready. All connected I²C devices recognize the STOP condition and know when the bus is idle to monitor the bus for START condition followed by an address. To communicate with a specific device, after the host or master sends a START condition, it generates the SCL (clock) pulses and transmits the 7-bit address of the destination device along with an 8th (R/W) data-direction bit as one byte. All devices compare the address to their own fixed address. The SDA line is released after the 8th bit for the target receiver to reply with an ACK (by pulling the SDA line low during the high period of the 9th clock). By receiving the ACK, the master realizes that the slave is ready and the link is OK.

DETAILED DESCRIPTION (continued)

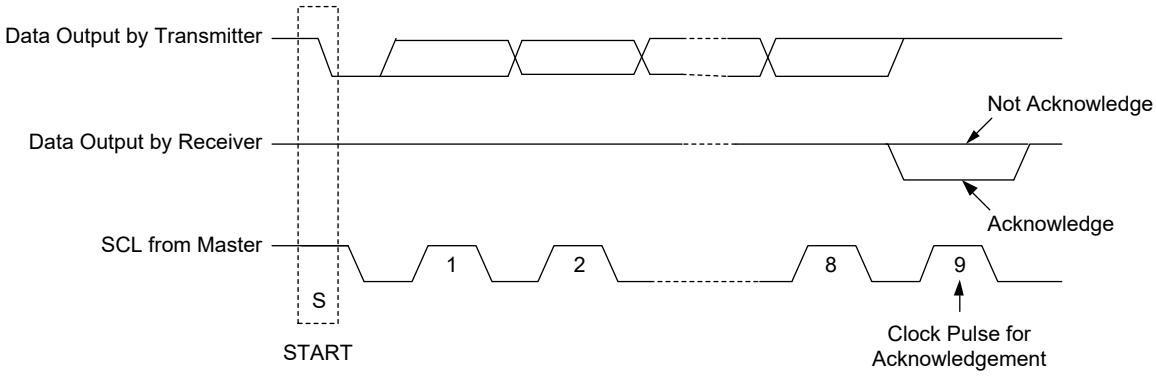


Figure 16. Acknowledgement on the I²C Bus

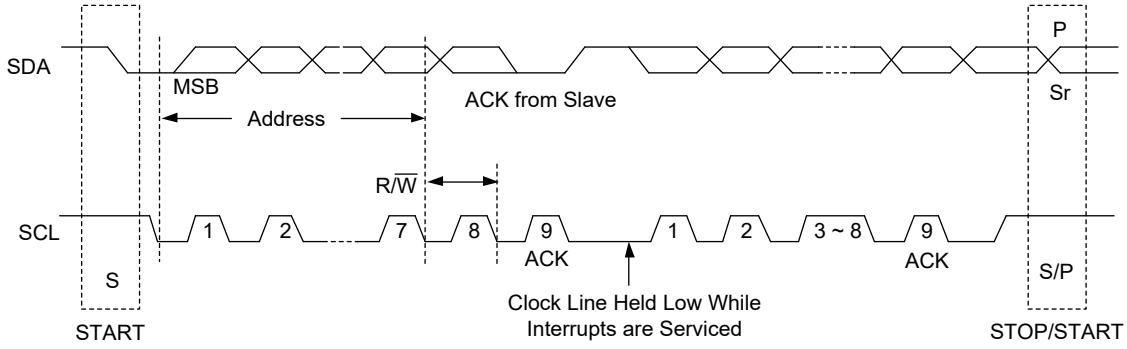


Figure 17. I²C Data Communication Protocol

Register Read and Write

After sending a START condition, the master sends the slave address (7 bits) with an 8th data-direction bit (R/$\overline{W}$) to inform the slave if the following byte of data is supposed to be a received by slave (WRITE) or the slave should send a byte of data back to master (READ). After receiving the ACK from the addressed slave, the master continues to send more clock pulses for future read or write. Usually, the second byte is also a WRITE containing the register address that the master wants to access in the slave.

WRITE: If the sequence is a single write and the master wants to write in the addressed register in the slave, the third byte will be the content of the addressed register as shown in Figure 18 for a single write data transfer. Ignoring the slaves reply (ACK or NCK), the master issues a STOP and the transaction is ended.

READ: If the sequence is a single read and the master wants to read the content of the addressed register in the slave, the master first sends a new START (repeated START) before the third byte because the direction of read/write needs to be changed from write to read. Therefore, the third byte is still the slave address (7 bits) and an 8th data-direction bit will be R/$\overline{W}$ = 1. The slave will send an ACK bit followed by the content of the register as the fourth byte. Master may reply with an ACK or NCK and then issues a STOP condition. The format of a single read from a device register is shown in the Figure 19. Reading data from a register address that is not listed will be 00h.

The device register contents are updated on the falling edge of the acknowledge signal after the last byte.

DETAILED DESCRIPTION (continued)

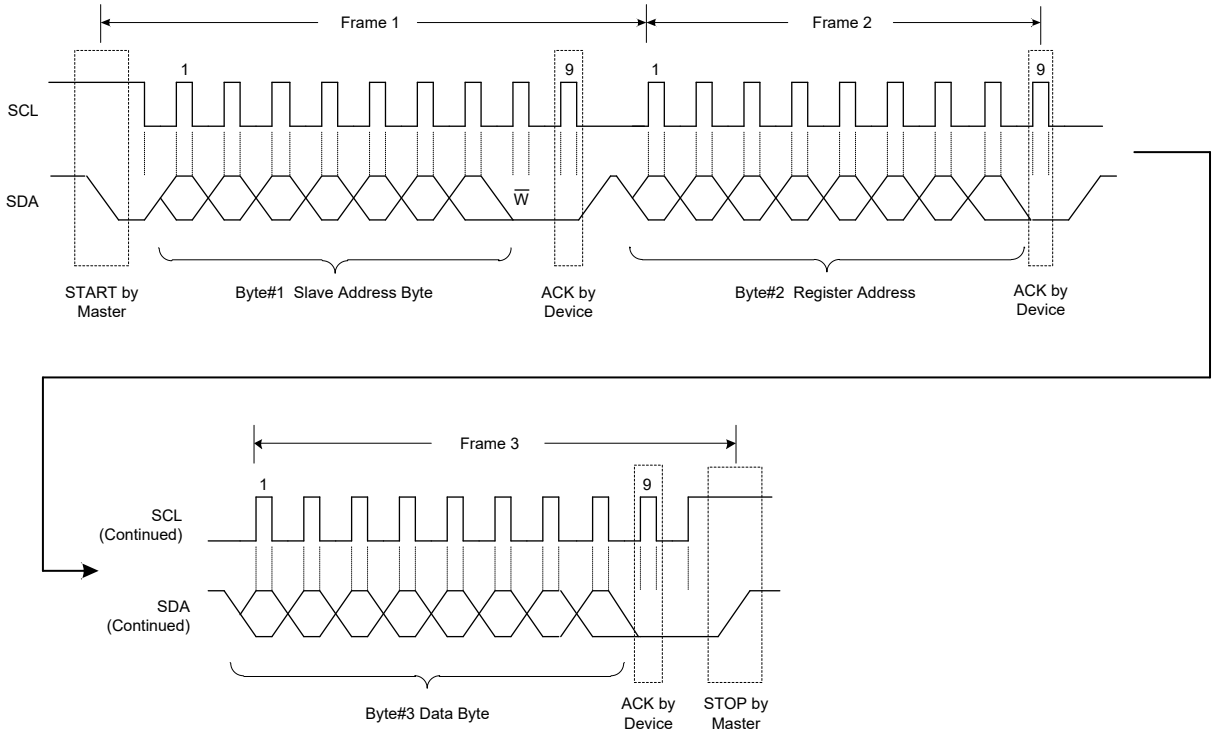


Figure 18. The Format of a WRITE into a Device Register in the Standard, Fast and Fast-Plus Modes

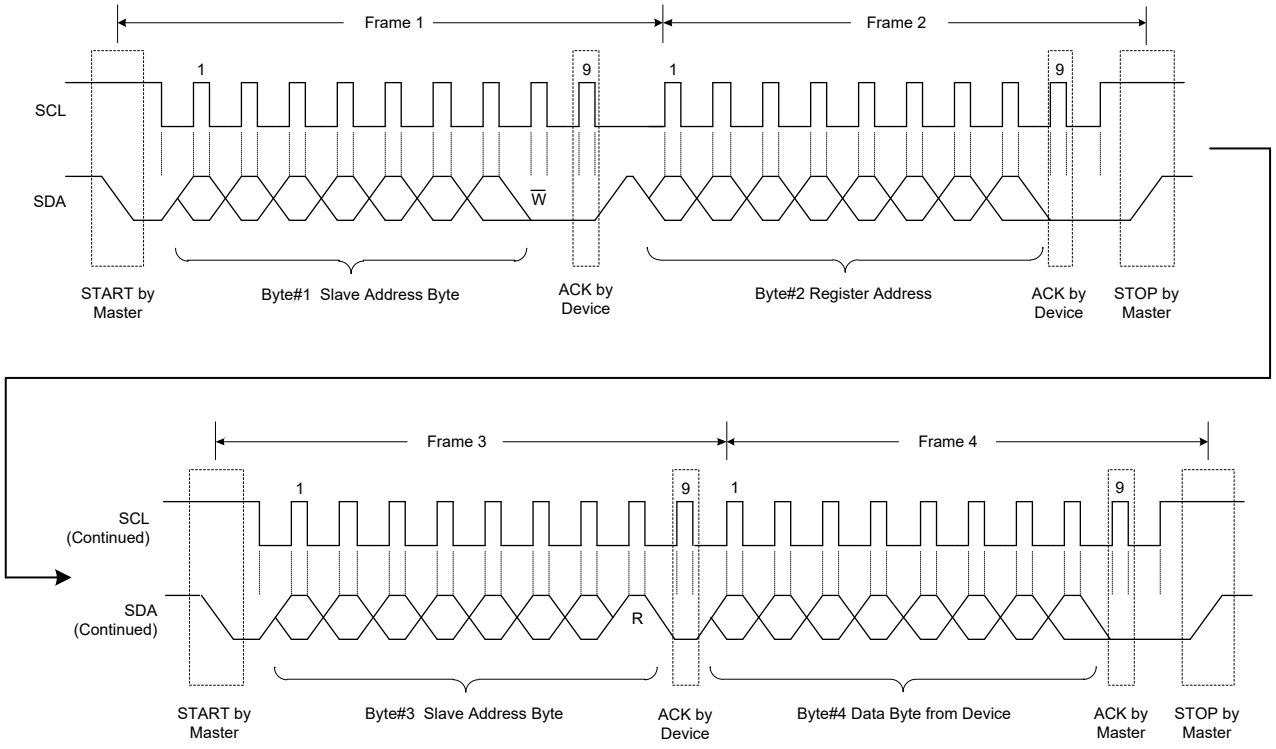


Figure 19. The Format of a READ from a Device Register in the Standard, Fast and Fast-Plus Modes

REGISTER MAP

Table 3 lists the map of the SGM62110 and SGM62111 registers. Any register address not listed in Table 3 should be considered as a reserved location and no write should be tried to modify them (they may be used in future revisions).

Table 3. Device Registers

ADDRESS	ACRONYM	REGISTER NAME
01h	CONTROL	Control Register
02h	STATUS	Status Register
03h	DEVID	Device Identity Register
04h	VOUT1	VOUT1 Register
05h	VOUT2	VOUT2 Register

R/W: Read/Write bit(s)
R: Read only bit(s)
PORV: Power-On Reset Value

Control Register (Address = 01h) [reset value = 20h for SGM62110 and 00h for SGM62111]

The control register is a volatile register. The contents are lost when the input voltage drops below the UVLO threshold or a logic low is applied on EN pin. Control register is a read/write register which programs the operation mode of the device as shown in Figure 4. Write to the reserved bit is not allowed.

Table 4. Control Register Details

BITS	BIT NAME	TYPE	PORV	DESCRIPTION
D[7]	RESERVED	R	0	Reserved
D[6]	RANGE	R/W	0	Select the Output Voltage Range 0 = Low range (1.800V to 4.975V) (default) 1 = High range (2.025V to 5.200V)
D[5]	ENABLE	R/W	x	Control Operation of the Converter 0 = Converter operation disabled (Startup value for SGM62111) 1 = Converter operation enabled (Startup value for SGM62110)
D[4]	RESERVED	R/W	0	Reserved. This bit allows read and write, however no function will be programmed, it is recommended to program this bit to 0.
D[3]	FPWM	R/W	0	Set Forced PWM Operation 0 = Disable (default) 1 = Enable
D[2]	RPWM	R/W	0	Set Ramp PWM Operation 0 = Disable (default) 1 = Enable
D[1:0]	SLEW[1:0]	R/W	00	Set the Slew Rate. Set the slew rate of the output voltage change to a new value. 00 = 1V/ms (default) 01 = 2.5V/ms 10 = 5V/ms 11 = 10V/ms

REGISTER MAP (continued)

Status Register (Address = 02h) [reset value = 00h]

Status register bit details are shown in Table 5. This is a read only register containing the device status information. A read operation clears all bits of this register (unless a status is still valid during the read and sets the bit again). It is a volatile register and loses its contents if the V_{IN} falls below UVLO threshold or the device is disabled by applying a low to the EN pin.

Table 5. Status Register Details

BITS	BIT NAME	TYPE	PORV	DESCRIPTION
D[7:4]	RESERVED	R	000	Reserved
D[3]	HD	R	0	The Status of the Hot-die Function 0 = Normal operation (default) 1 = A hot-die event was detected
D[2]	OC	R	0	The Status of the Over-Current Function 0 = Normal operation (default) 1 = An over-current event was detected
D[1]	TSD	R	0	Thermal Shutdown. It is cleared if this register is read and if the over-temperature condition no longer exists. 0 = Temperature good (default) 1 = An OTP event occurred
D[0]	PGn	R	0	Output Power-Good PG is cleared with a read if the power-not-good condition no longer exists. 0 = Power-good (default) 1 = A power-not-good event was detected

Device Identity Register (Address = 03h) [reset value = 40h]

Device identity register bit details are shown in Table 6. This is a read only register that holds the die revision of the device.

Table 6. Device Identity Register Details

BITS	BIT NAME	TYPE	PORV	DESCRIPTION
D[7:4]	DEVICE[3:0]	R	0100	Device ID (0100 = SGMICRO).
D[3:2]	MAJOR[1:0]	R	00	Major Die Revision 00 = A, initial silicon 01 = B, first major revision 10 = C, second major revision 11 = D, third major revision
D[1:0]	MINOR[1:0]	R	00	Minor Die Revision 00 = 0, initial silicon 01 = 1, first minor revision 10 = 2, second minor revision 11 = 3, third minor revision

REGISTER MAP (continued)

VOUT1 Register (Address = 04h) [reset value = 3Ch]

VOUT1 register bit details are shown in Table 7. VOUT1 register determines the device output voltage if the VSEL pin is logic low. It is a volatile register and loses its contents if the V_{IN} voltage falls below UVLO threshold or the device is disabled by applying a low to the EN pin.

Table 7. VOUT1 Register Details

BITS	BIT NAME	TYPE	PORV	DESCRIPTION
D[7]	RESERVED	R	0	Reserved
D[6:0]	VOUT1[6:0]	R/W	0111100	Set VOUT1 Output Voltage V_{OUT} = 1.8 + (VOUT1[6:0] × 0.025)V (RANGE = 0, default 3.3V) V_{OUT} = 2.025 + (VOUT1[6:0] × 0.025)V (RANGE = 1, default 3.525V)

VOUT2 Register (Address = 05h) [reset value = 42h]

VOUT2 register bit details are shown in Table 8. VOUT2 register determines the device output voltage if the VSEL pin is logic high. It is a volatile register and loses its contents if the V_{IN} voltage falls below UVLO threshold or the device is disabled by applying a low to the EN pin.

Table 8. VOUT2 Register Details

BITS	BIT NAME	TYPE	PORV	DESCRIPTION
D[7]	RESERVED	R	0	Reserved
D[6:0]	VOUT2[6:0]	R/W	1000010	Set VOUT2 Output Voltage V_{OUT} = 1.8 + (VOUT2[6:0] × 0.025)V (RANGE = 0, default 3.45V) V_{OUT} = 2.025 + (VOUT2[6:0] × 0.025)V (RANGE = 1, default 3.675V)

APPLICATION INFORMATION

The SGM62110 and SGM62111 are perfect choices for applications that demand for a power supply with high efficiency over a wide load range and their input voltage can vary from below, near and above the desired output voltage. The peak current in the internal switch of the device is typically limited to a maximum of around 6A. Input and output voltage ranges are 2.2V to 5.5V and 1.8V to 5.2V respectively.

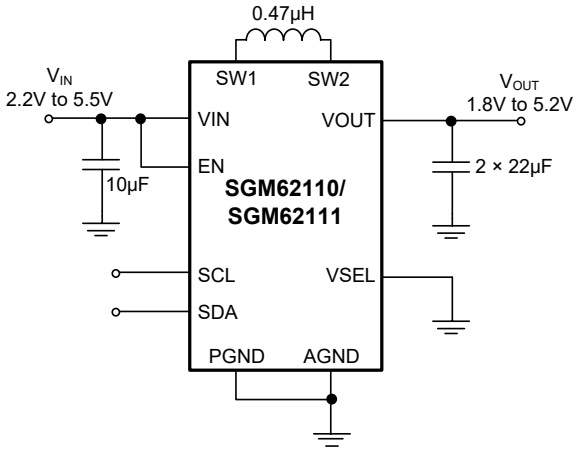


Figure 20. Application Example of Smartphone 2A Power Supply with 1.8V to 5.2V Output

Design Requirements

This example of the design parameters is shown in Table 9.

Table 9. Design Parameters

Parameter	Symbol	Recommended Value
Input Voltage	V_{IN}	2.5V to 4.8V
Output Voltage	V_{OUT}	1.8V to 5.2V
Output Current	I_{OUT}	2A
I²C Bus Capacitance	C_B	100pF
I²C Bus Voltage	V_{BUS}	3.3V
I²C Bus Speed		Fast-mode (400kHz)

Design Procedure

Input Capacitor

The total input capacitance after considering the DC bias de-rating is recommended to be above 5μF. It is recommended to use a 10μF, 6.3V ceramic capacitor in most applications. If the source is far away from the device, it is recommended to use additional bulk capacitance (such as a 47μF electrolytic or tantalum capacitor) for better stability.

Inductor

A 0.47μH inductor is recommended for use with SGM62110 and SGM62111. Lower DCR inductors are recommended for better efficiency. The rated saturation current (I_{SAT}) must be at least 20% above the maximum peak current in the worst cases including transients. Usually the worst cases occur in the Boost mode when operating at the lowest input voltage, highest output voltage and with the maximum load. Use Equation 1 to calculate the maximum duty cycle in Boost mode (corresponds to the maximum inductor current).

$$D_{MAX} = \frac{V_{OUT\_MAX} - V_{IN\_MIN}}{V_{OUT\_MAX}} \quad (1)$$

where:

D_{MAX} is the maximum duty cycle in Boost mode.

V_{IN_MIN} is the minimum input voltage.

V_{OUT_MAX} is the maximum output voltage.

In this application:

$$D_{MAX} = \frac{5.2V - 2.5V}{5.2V} \times 100\% = 52\%$$

The maximum inductor current can be calculated by:

$$I_{LM} = \frac{I_{OUT\_MAX}}{\eta(1 - D_{MAX})} + \frac{D_{MAX} \times V_{IN\_MIN}}{2fL} \quad (2)$$

where:

I_{LM} is the peak inductor current.

I_{OUT_MAX} is the maximum output current.

η is the converter efficiency (use application curves or choose 90%).

f is the switching frequency (3MHz).

L is the inductance (0.47μH).

$$I_{LM} = \frac{2A}{0.9 \times (1 - 0.52)} + \frac{0.52 \times 2.5V}{2 \times 3MHz \times 0.47\mu H} = 5.1A$$

Choose the I_{SAT} value at least 20% higher than the calculated I_{LM} value. In this example, I_{LM} ≈ 5.1A and the selected inductor saturation current is 6.1A.

APPLICATION INFORMATION (continued)

Output Capacitor

It is recommended to have at least 16μF effective output capacitance (after de-rating) for the SGM62110 and SGM62111. Using two 22μF, 6.3V ceramic capacitors should be sufficient for most applications. To reduce high frequency noise, a 100nF ceramic capacitor in 0201 or 0402 package is recommended to place as close to the VOUT and GND pins as possible in parallel to the other output capacitors.

There is no upper limit for the SGM62110 and SGM62111 output capacitance. However, using large output capacitance results in slower response to the transients and can cause other issues when the output is discharged.

I²C Pull-up Resistors

The standard I²C specifications and user manual can be used to set up the I²C bus. The maximum pull-up resistor value for the required bus speed can be calculated from Equation 3:

$$R_{P\_MAX} = \frac{t_R}{0.8473 \times C_B} \quad (3)$$

where:

t_R = maximum allowed rise time (300ns for fast-mode).
C_B = total capacitive load on each bus line.

$$R_{P\_MAX} = \frac{300ns}{0.8473 \times 100pF} = 3.541k\Omega$$

If the bus capacitance is not known for the application, measure the rise time with an oscilloscope starting with a 1kΩ pull-up and then calculate the C_B from Equation 3 to find the maximum allowed pull-up resistor.

To find the minimum permitted pull-up resistor value for a specific bus speed, use Equation 4.

$$R_{P\_MIN} = \frac{V_{BUS} - V_{OL}}{I_{OL}} \quad (4)$$

where:

V_{BUS} is the I²C bus pull-up voltage.
V_{OL} is the low-level output voltage (0.4V).
I_{OL} is the low-level output current (3mA for the fast mode).

$$R_{P\_MIN} = \frac{3.3V - 0.4V}{3mA} = 967\Omega \quad (5)$$

The pull-up resistor of R_P = 3.3kΩ meets both requirements.

Application Curves

Table 10 lists the component values and part numbers used for the tests and measurements outlined in the characteristic curves.

Table 10. Components used for Characteristic Curves

Reference	Description	Part Number	Manufacturer
C_1	Capacitor, 10μF, 6.3V, 0603, ceramic	GRM155R60J106ME15	Murata
C_2, C_3	Capacitor, 22μF, 6.3V, 0603, ceramic	GRM188R61A226ME15	Murata
L_1	Inductor, 0.47μH	744383560047HT	Wurth
U_1	Integrated circuit	SGM62110	SGMICRO

LAYOUT

Layout Guidelines

Layout plays a significant role for all switch modes in DC/DC power supplies. Improper layout could result in poor EMI performance, device unstable, and potential device damage. The input capacitor, output capacitor and the inductor should be placed as close as possible to the IC. The SGM62110 and SGM62111 implement a power ground and control ground pins to minimize the ground noise effect on sensitive analog circuits. Use a separate ground trace to connect the feedback, and connect this ground trace to the main power ground at a single point.

Figure 21 is an example layout which is also the PCB layout used to collect the data in the Application Curves section.

Layout Example

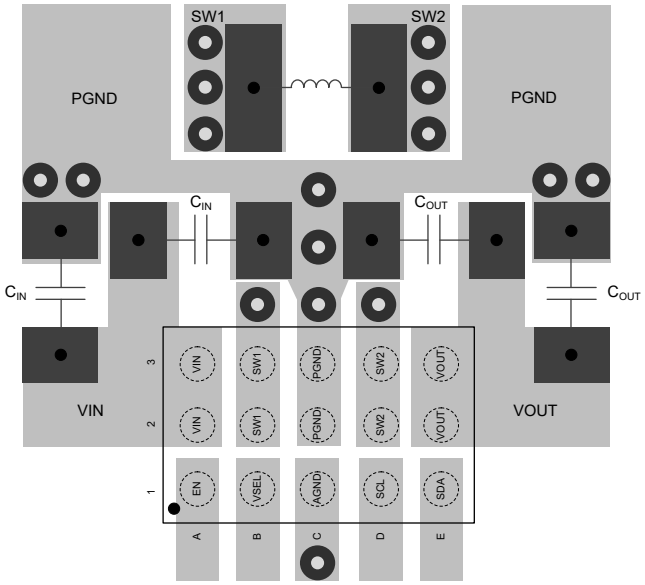


Figure 21. Recommended PCB Layout

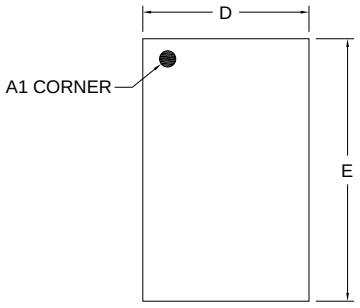
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

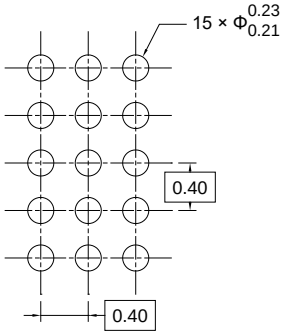
Changes from Original (MAY 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

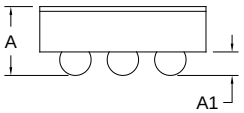
WLCSP-2.21×1.40-15B



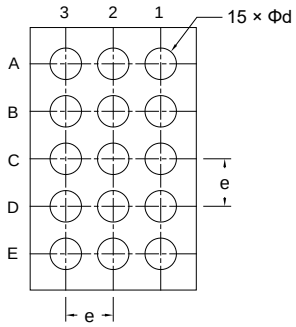
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



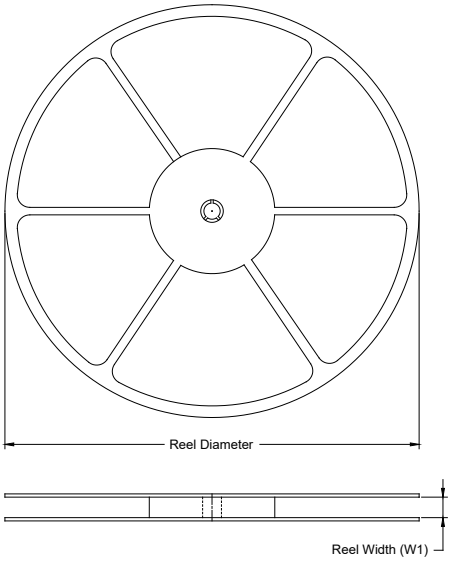
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.542	0.580	0.618
A1	0.178	0.198	0.218
D	1.380	1.405	1.430
E	2.190	2.215	2.240
d	0.245	0.265	0.285
e	0.400 BSC		

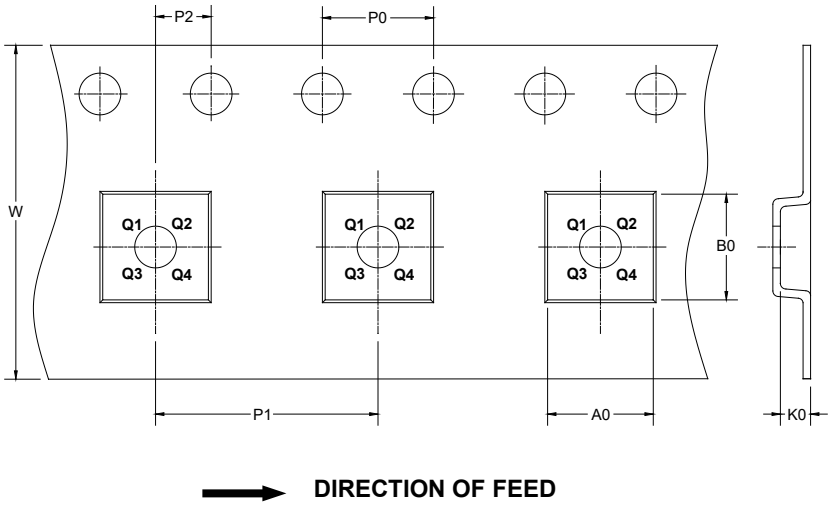
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



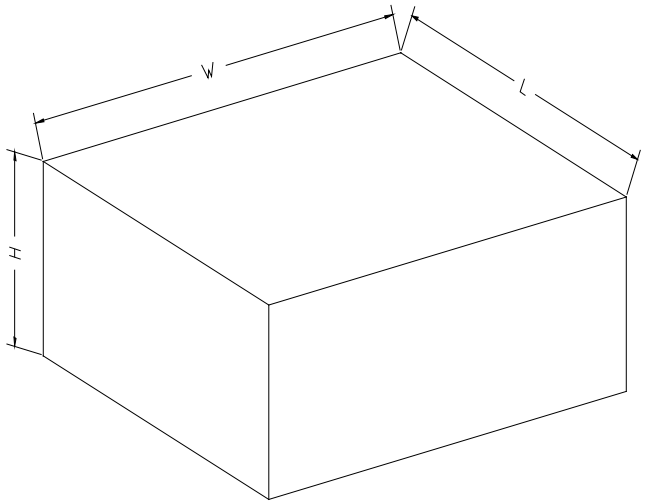
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.21×1.40-15B	7″	9.5	1.53	2.38	0.73	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002