SGM5200
12-Bit, 1MSPS, 16 Channels, Single-Ended, Serial Interface ADC

GENERAL DESCRIPTION

The SGM5200 is a 12-bit multichannel inputs analog-to-digital converter (ADC). The device includes a capacitor based SAR ADC with inherent sample and hold circuit.

The SGM5200 accepts a wide power supply range from 2.7V to 5.25V. Very low power consumption makes the device suitable for battery-powered or isolated power supply applications.

A wide 1.7V to 5.25V digital I/O power supply range facilitates a glueless interface with the most commonly used digital hosts. The serial interface is controlled by nCS and SCLK for easy connection with microprocessors and DSP.

The input signal is sampled with the falling edge of nCS. It uses SCLK for conversion, serial data output and reading serial data in. The device allows auto sequencing of preselected channels or manual selection of a channel for the next conversion cycle.

There are two software selectable input ranges (0V to V_{REF} and 0V to 2 × V_{REF}), individually configurable GPIOs (four in case of the TSSOP package and one in TQFN package) and two programmable alarm thresholds per channel. These features make the device suitable for most data acquisition applications.

The SGM5200 offers an attractive power-down feature. This is extremely useful for power saving when the device is operated at lower conversion speeds.

The SGM5200 is available in Green TSSOP-38 and TQFN-5×5-32L packages. It operates over an ambient temperature range -40℃ to +125℃.

FEATURES

- **1MHz Sample Rate**
- **12-Bit Resolution**
- **16 Channels**
- **Zero Latency**
- **20MHz Serial Interface**
- **Analog Power Supply Range: 2.7V to 5.25V**
- **Digital I/O Power Supply Range: 1.7V to 5.25V**
- **Two Software Selectable Unipolar, Input Ranges**
  - **Range 1: 0V to V_{REF}**
  - **Range 2: 0V to 2 × V_{REF}**
- **Auto and Manual Modes for Channel Selection**
- **Two Programmable Alarm Thresholds per Channel**
- **Four Individually Configurable GPIOs in TSSOP Package and One GPIO in TQFN Package**
- **Typical Power Dissipation:**
  24mW (V_A = 5V, V_{BD} = 3V) at 1MSPS
- **Power-Down Current: 1.4μA (TYP)**
- **Input Bandwidth: 45MHz (TYP) at -3dB**
- **Available in Green TSSOP-38 and TQFN-5×5-32L Packages**

APPLICATIONS

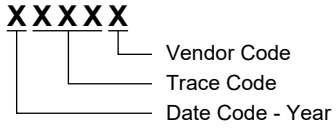
PLC/IPC
Optical Line Card Monitoring
Medical Instrumentation
Digital Power Supplies
Multichannel, General-Purpose Signal Monitoring
High-Speed Data Acquisition Systems
High-Speed Closed-Loop Systems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5200	TSSOP-38	-40℃ to +125℃	SGM5200XTS38G/TR	SGM5200 XTS38 XXXXX	Tape and Reel, 4000
	TQFN-5×5-32L	-40℃ to +125℃	SGM5200XTQL32G/TR	SGM5200 XTQL32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AINP or CHx to AGND ..... -0.3V to V_A + 0.3V
+VA to AGND, +VBD to BDGND ..... -0.3V to 6V
Digital Input Voltage to BDGND ..... -0.3V to 6V
Digital Output to BDGND ..... -0.3V to V_A + 0.3V
Input Current to Any Pin except Supply Pins ..... -10mA to 10mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Analog Power Supply Voltage Range ..... 2.7V to 5.25V
Digital I/O Power Supply Voltage Range ..... 1.7V to V_A
Reference Voltage Range ..... 2V to 3V
SCLK Frequency 20MHz
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

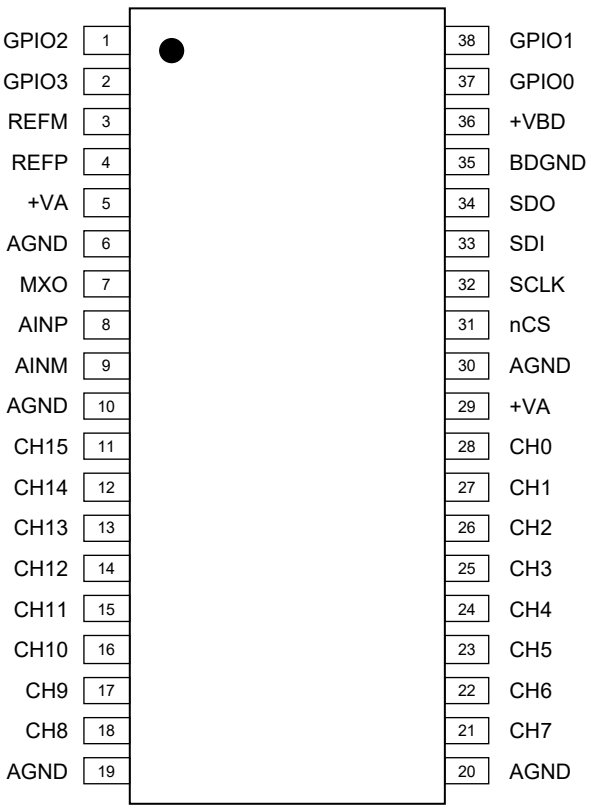
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

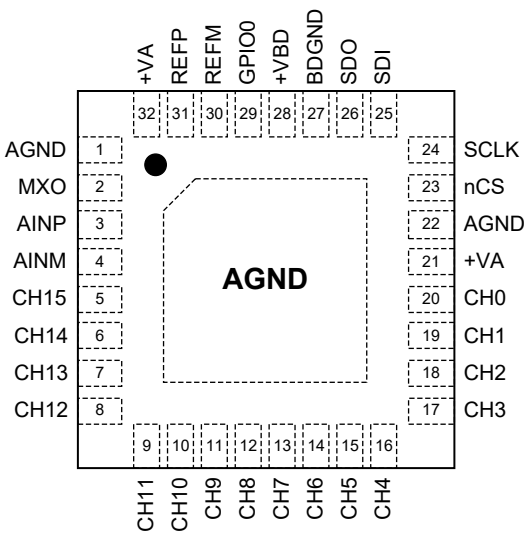
PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-38

(TOP VIEW)



TQFN-5×5-32L

PIN DESCRIPTION

PIN		NAME	TYPE (1)	FUNCTION
TSSOP-38	TQFN-5×5-32L			
1	–	GPIO2	DIO	General-Purpose Input or Output.
		Range	DI	Selects ADC Input Range High (1): select Range 2 (0V to 2 × V_{REF}), Low (0): select Range 1 (0V to V_{REF}).
2	–	GPIO3	DIO	General-Purpose Input or Output.
		nPD	DI	Active Low Power-Down Input.
3	30	REFM	AI	Reference Ground.
4	31	REFP	AI	Reference Input.
5, 29	21, 32	+VA	–	Analog Power Supply.
6, 10, 19, 20, 30	1, 22	AGND	–	Analog Ground.
7	2	MXO	AO	Multiplexer Output.
8	3	AINP	AI	ADC Input Signal.
9	4	AINM	AI	ADC Input Ground.
11	5	CH15	AI	Analog Channel for Multiplexer.
12	6	CH14	AI	
13	7	CH13	AI	
14	8	CH12	AI	
15	9	CH11	AI	
16	10	CH10	AI	
17	11	CH9	AI	
18	12	CH8	AI	
21	13	CH7	AI	
22	14	CH6	AI	
23	15	CH5	AI	
24	16	CH4	AI	
25	17	CH3	AI	
26	18	CH2	AI	
27	19	CH1	AI	
28	20	CH0	AI	
31	23	nCS	DI	Chip-Select Input Pin. Active low.
32	24	SCLK	DI	Serial Clock Input Pin.
33	25	SDI	DI	Serial Data Input Pin.
34	26	SDO	DI	Serial Data Output Pin.
35	27	BDGND	–	Digital Ground.
36	28	+VBD	–	Digital Power Supply.
37	29	GPIO0	DIO	General-Purpose Input or Output.
		Alarm	DO	Active High Alarm Output. For configuration, see the Programming section.
38	–	GPIO1	DIO	General-Purpose Input or Output.
		Low Alarm	DO	Active High Output Indicating Low Alarm.

NOTE:
1. AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input or Output.

ELECTRICAL CHARACTERISTICS

(V_A = 2.7V to 5.25V, V_{BD} = 1.7V to V_A, V_{REF} = 2.5V ± 0.1V, f_{SAMPLE} = 1MHz, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Input							
Full-Scale Input Span (1)		Range 1		0		V_{REF}	V
		Range 2 while 2 × V_{REF} ≤ V_A		0		2 × V_{REF}	
Absolute Input Range		Range 1		-0.2		V_{REF} + 0.2	V
		Range 2 while 2 × V_{REF} ≤ V_A		-0.2		2 × V_{REF} + 0.2	
Input Capacitance					31		pF
Input Leakage Current		T_A = +125℃			60		nA
System Performance							
Resolution					12		Bits
No Missing Codes		Range 1		11			Bits
		Range 2		12			
Integral Linearity		Range 1		-3.50	±1.6	2.60	LSB (2)
		Range 2		-1.32	±0.8	1.32	
Differential Linearity		Range 1		-1.00	-1/+1.3	2.20	LSB
		Range 2		-0.99	±0.5	1.00	
Offset Error (3)		Range 1		-4.00	±0.6	4.00	LSB
		Range 2		-5.60	±1.6	5.60	
Gain Error		Range 1		-5.20	±0.8	4.40	LSB
		Range 2		-4.10	±0.8	3.10	
Total Unadjusted Error	TUE	Range 1			±1.8		LSB
		Range 2			±1.9		
Sampling Dynamics							
Conversion Time		20MHz SCLK			800		ns
Acquisition Time					325		ns
Maximum Throughput Rate		20MHz SCLK				1	MHz
Aperture Delay					6		ns
Dynamic Characteristics							
Total Harmonic Distortion (4)	THD	100kHz	Range 1		-77		dB
			Range 2		-79		
Signal-to-Noise Ratio	SNR	100kHz	Range 1	66.4	70.4		dB
			Range 2	67.9	71.4		
Signal-to-Noise + Distortion		100kHz	Range 1	65.6	69.5		dB
			Range 2	66.7	70.7		
Spurious Free Dynamic Range		100kHz	Range 1		78		dB
			Range 2		81		
Small Signal Bandwidth		At -3dB			45		MHz
Channel-to-Channel Crosstalk		Any off-channel with 100kHz, full-scale input to channel being sampled with DC input (isolation crosstalk)			-100		dB
		From previously sampled to channel with 100kHz, full-scale input to channel being sampled with DC input (memory crosstalk)			-84		

ELECTRICAL CHARACTERISTICS (continued)

(V_A = 2.7V to 5.25V, V_{BD} = 1.7V to V_A, V_{REF} = 2.5V ± 0.1V, f_{SAMPLE} = 1MHz, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Reference Input						
Reference Voltage at REFP (5)	V_{REF}		2	2.5	3	V
Reference Input Resistance		At f_{SAMPLE} = 1MHz		31		kΩ
Alarm Setting						
High Threshold Range			0		4092	LSB
Low Threshold Range			0		4092	LSB
Digital Input/Output						
Logic Level	V_{IH}	V_{BD} = 5.25V	3.10			V
	V_{IL}				1.90	
	V_{IH}	V_{BD} = 1.7V	1.25			
	V_{IL}				0.45	
	V_{OH}	At I_{SOURCE} = 200μA	V_{BD} - 0.2			
	V_{OL}	At I_{SINK} = 200μA			0.4	
Data Format MSB First				MSB First		
Power Supply Requirements						
+VA Supply Voltage	V_A		2.7	3.3	5.25	V
+VBD Supply Voltage	V_{BD}		1.7	3.3	5.25	V
Supply Current (Normal Mode)		At V_A = 2.7V to 3.6V and 1MHz throughput		3		mA
		At V_A = 2.7V to 3.6V static state		1.1		
		At V_A = 4.7V to 5.25V and 1MHz throughput		4.1	5.4	
		At V_A = 4.7V to 5.25V static state		1.1	2.2	
Power-Down State Supply Current				1.4		μA
+VBD Supply Current		V_A = 5.25V, f_{SAMPLE} = 1MHz		1.3		mA
Power-Up Time				1		μs
Invalid Conversions after Power-Up or Reset				1		Conversion

NOTES:
1. Ideal input span; does not include gain or offset error.
2. LSB means least significant bit.
3. Measured relative to an ideal full-scale input.
4. Calculated on the first nine harmonics of the input frequency.
5. Device is designed to operate over V_{REF} = 2V to 3V. However, one can expect lower noise performance at V_{REF} < 2.4V. This is due to SNR degradation resulting from lowered signal range.

TIMING REQUIREMENTS

(Full = -40℃ to +125℃, V_A = 2.7V to 5.25V, unless otherwise noted.) [1] [2] (See Figure 1 and Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time	t_{CONV}	V_{BD} = 1.8V			16	SCLK
		V_{BD} = 3V			16	
		V_{BD} = 5V			16	
Minimum Quiet Sampling Time Needed from Bus 3-State to Start of Next Conversion	t_Q	V_{BD} = 1.8V	40			ns
		V_{BD} = 3V	40			
		V_{BD} = 5V	40			
Delay Time, nCS Low to First Data (DO-15) Out	t_{D1}	V_{BD} = 1.8V			38	ns
		V_{BD} = 3V			27	
		V_{BD} = 5V			17	
Setup Time, nCS Low to First Rising Edge of SCLK	t_{SU1}	V_{BD} = 1.8V	8			ns
		V_{BD} = 3V	6			
		V_{BD} = 5V	4			
Delay Time, SCLK Falling to SDO Next Data Bit Valid	t_{D2}	V_{BD} = 1.8V			35	ns
		V_{BD} = 3V			27	
		V_{BD} = 5V			17	
Hold Time, SCLK Falling to SDO Data Bit Valid	t_{H1}	V_{BD} = 1.8V	13			ns
		V_{BD} = 3V	12			
		V_{BD} = 5V	12			
Delay Time, 16th SCLK Falling Edge to SDO 3-State	t_{D3}	V_{BD} = 1.8V			26	ns
		V_{BD} = 3V			22	
		V_{BD} = 5V			13	
Setup Time, SDI Valid to Rising Edge of SCLK	t_{SU2}	V_{BD} = 1.8V	2			ns
		V_{BD} = 3V	3			
		V_{BD} = 5V	4			
Hold Time, Rising Edge of SCLK to SDI Valid	t_{H2}	V_{BD} = 1.8V	12			ns
		V_{BD} = 3V	10			
		V_{BD} = 5V	6			
Pulse Duration nCS High	t_{W1}	V_{BD} = 1.8V	20			ns
		V_{BD} = 3V	20			
		V_{BD} = 5V	20			
Delay Time nCS High to SDO 3-State	t_{D4}	V_{BD} = 1.8V			24	ns
		V_{BD} = 3V			21	
		V_{BD} = 5V			12	
Pulse Duration SCLK High	t_{WH}	V_{BD} = 1.8V	20			ns
		V_{BD} = 3V	20			
		V_{BD} = 5V	20			
Pulse Duration SCLK Low	t_{WL}	V_{BD} = 1.8V	20			ns
		V_{BD} = 3V	20			
		V_{BD} = 5V	20			
Frequency SCLK		V_{BD} = 1.8V			20	MHz
		V_{BD} = 3V			20	
		V_{BD} = 5V			20	

NOTES:

1. 1.8V specifications apply from 1.6V to 1.9V, 3V specifications apply from 2.7V to 3.6V, 5V specifications apply from 4.75V to 5.25V.
2. With 50pF load.

TIMING DIAGRAM

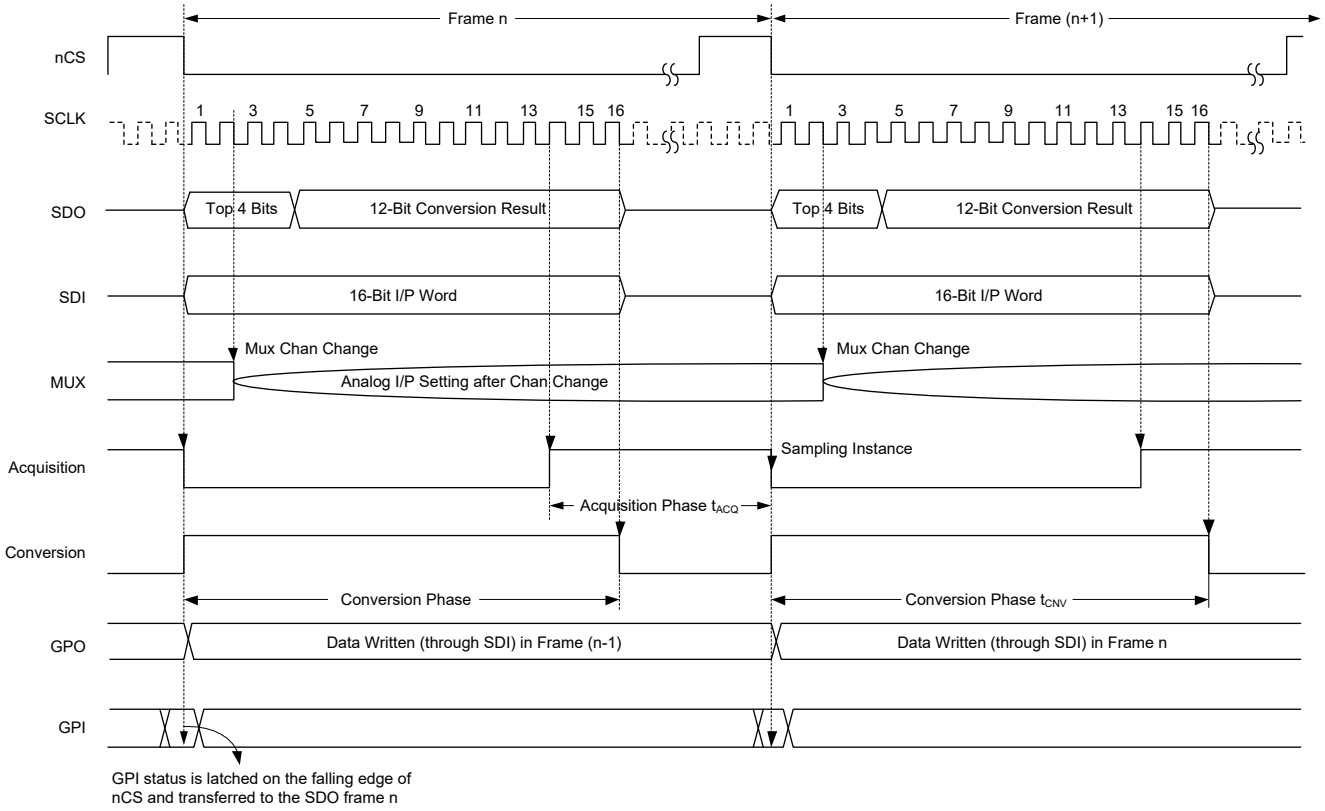


Figure 1. Device Operation Timing Diagram

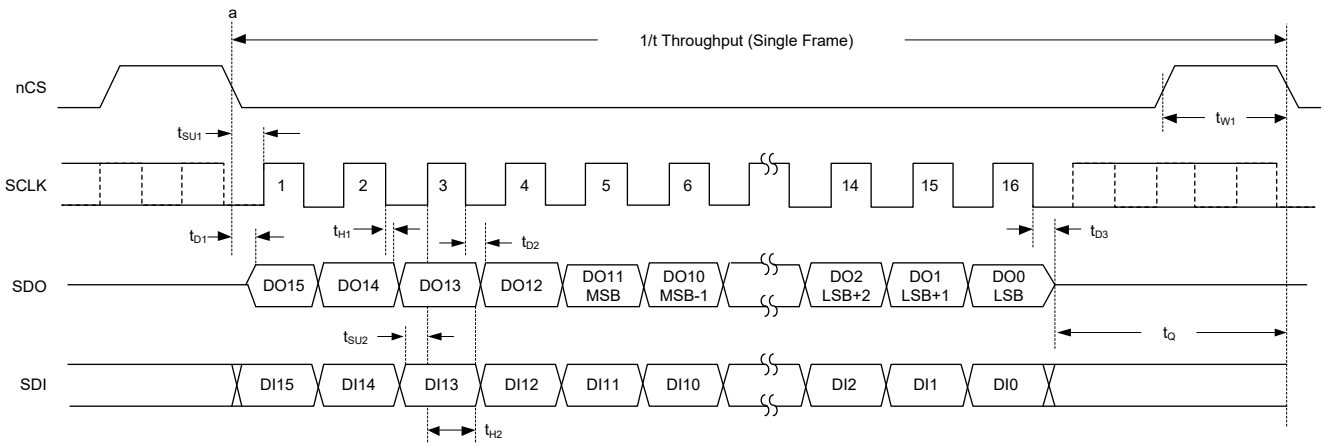
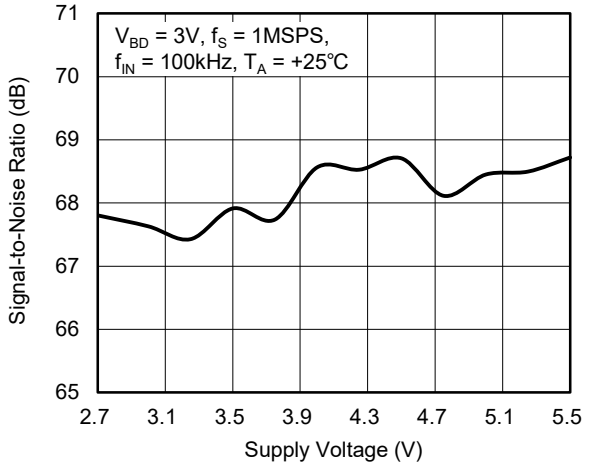


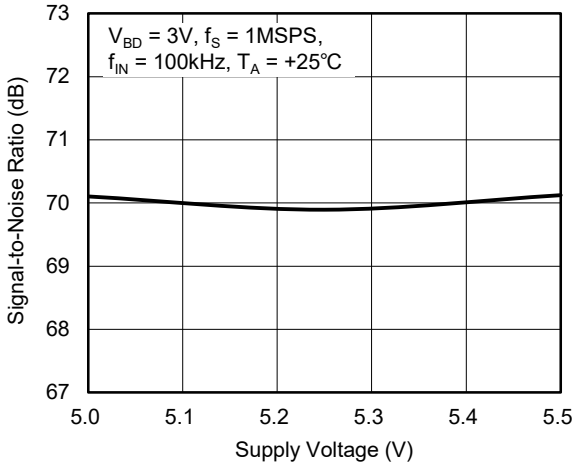
Figure 2. Serial Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

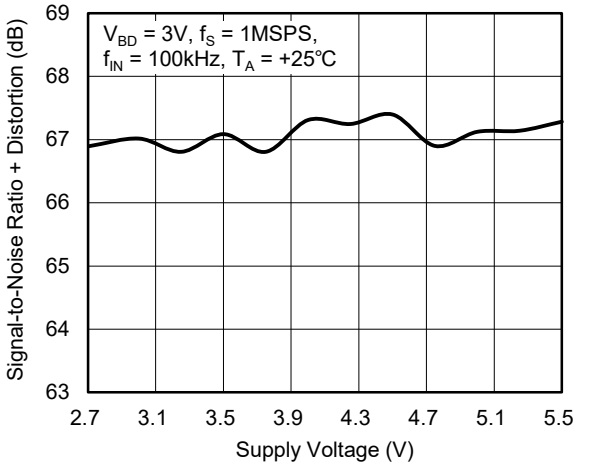
Signal-to-Noise Ratio vs. Supply Voltage (Range 1)



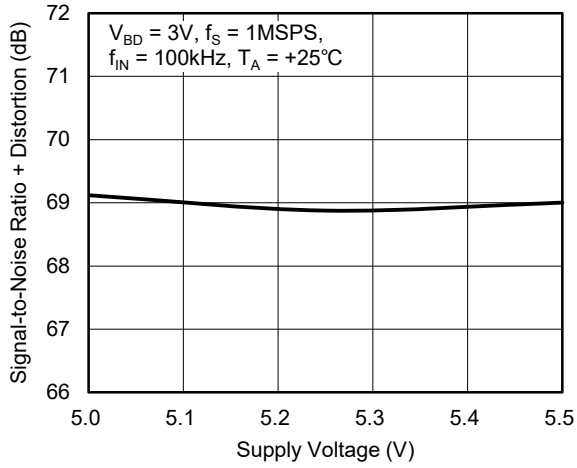
Signal-to-Noise Ratio vs. Supply Voltage (Range 2)



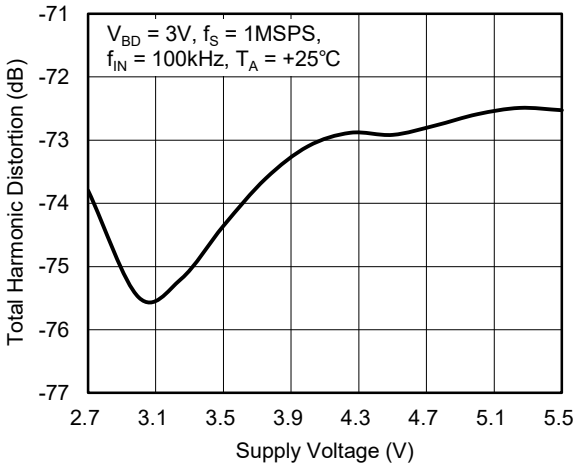
Signal-to-Noise + Distortion vs. Supply Voltage (Range 1)



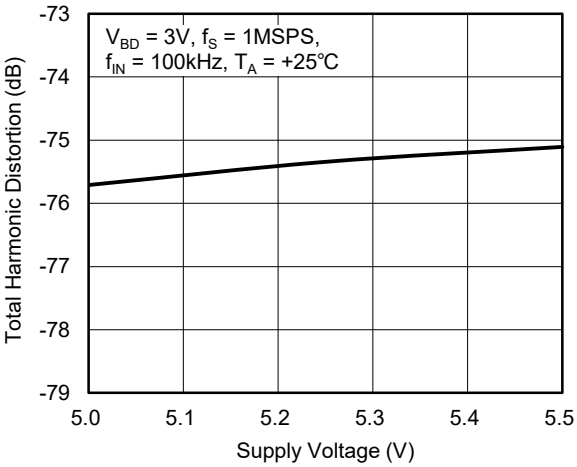
Signal-to-Noise + Distortion vs. Supply Voltage (Range 2)



Total Harmonic Distortion vs. Supply Voltage (Range 1)

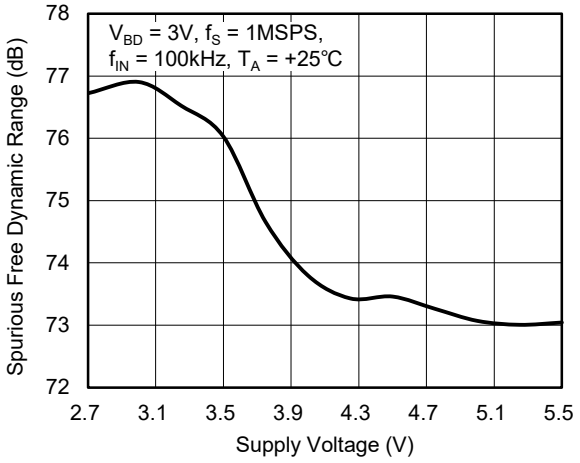


Total Harmonic Distortion vs. Supply Voltage (Range 2)

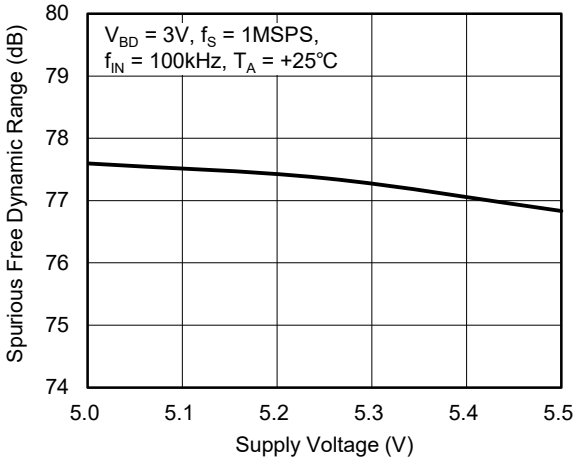


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

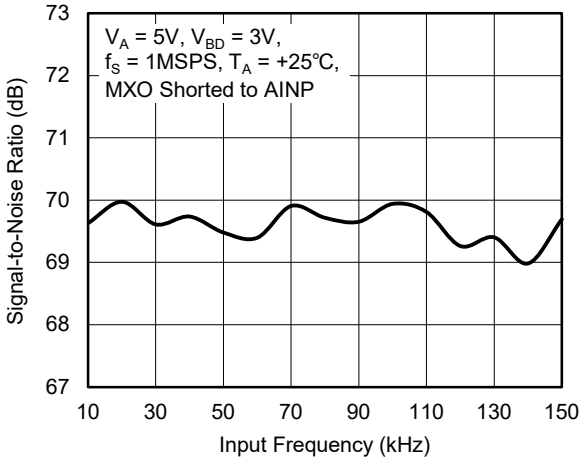
Spurious Free Dynamic Range vs. Supply Voltage (Range 1)



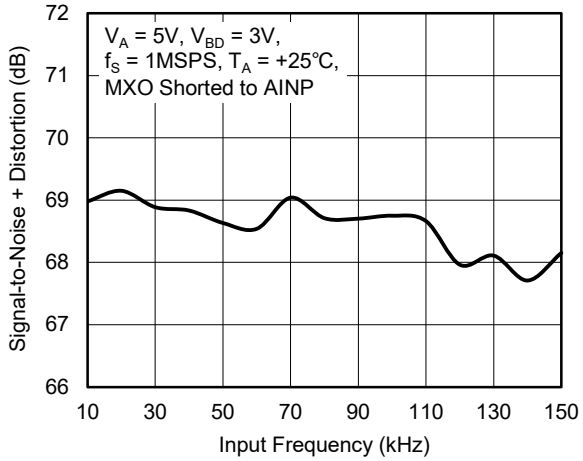
Spurious Free Dynamic Range vs. Supply Voltage (Range 2)



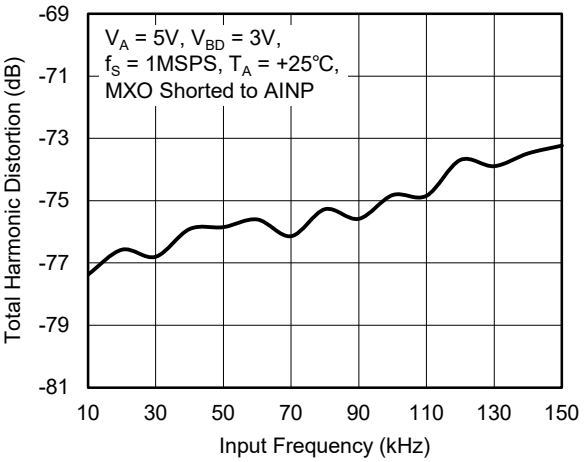
Signal-to-Noise Ratio vs. Input Frequency



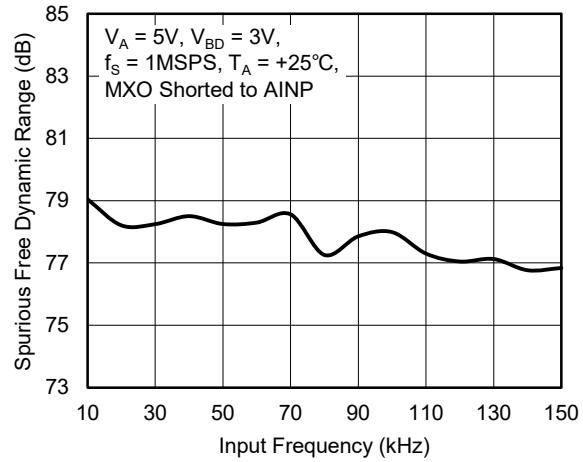
Signal-to-Noise + Distortion vs. Input Frequency



Total Harmonic Distortion vs. Input Frequency

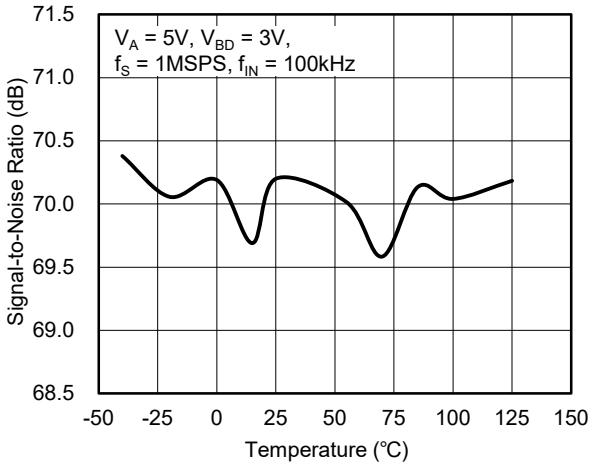


Spurious Free Dynamic Range vs. Input Frequency

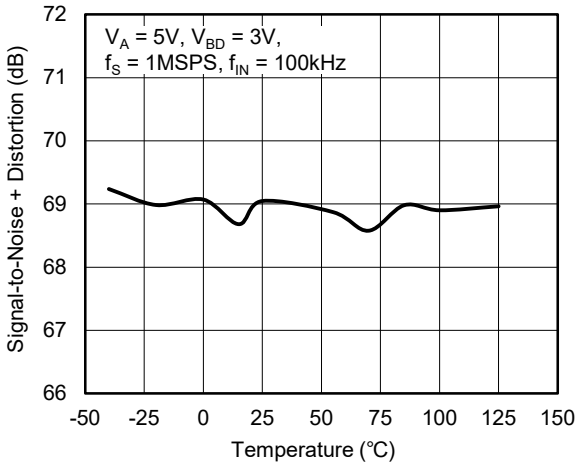


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

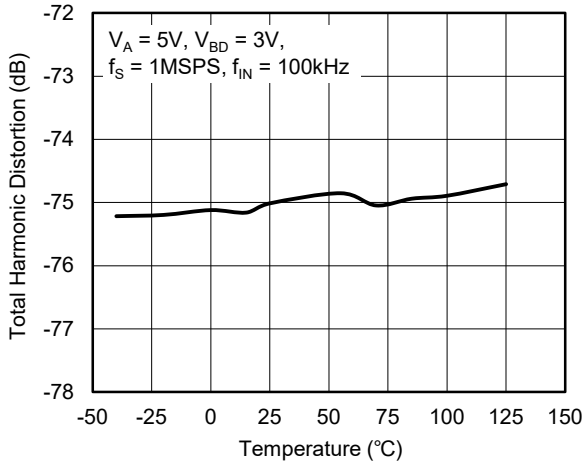
Signal-to-Noise Ratio vs. Temperature



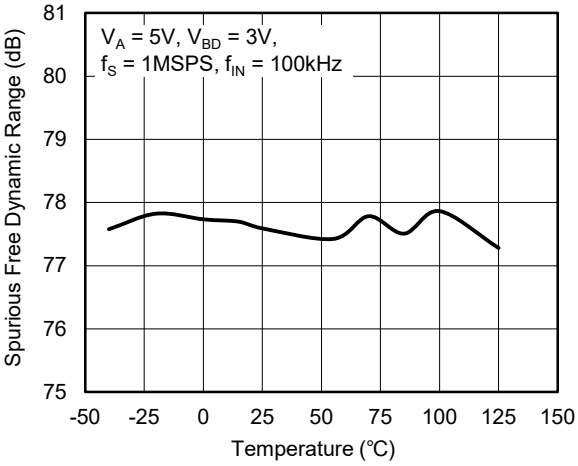
Signal-to-Noise + Distortion vs. Temperature



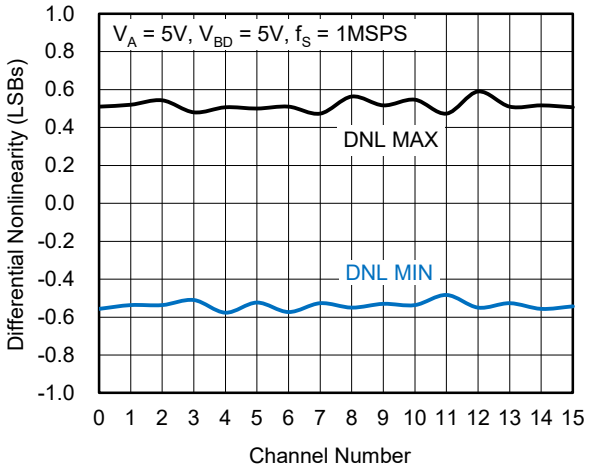
Total Harmonic Distortion vs. Temperature



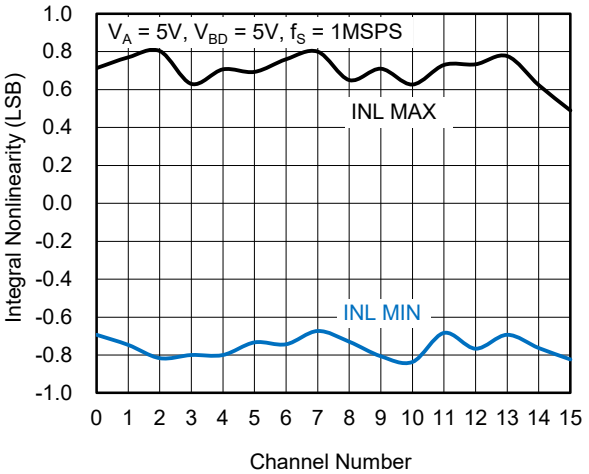
Spurious Free Dynamic Range vs. Temperature



Differential Nonlinearity Variation Across Channels

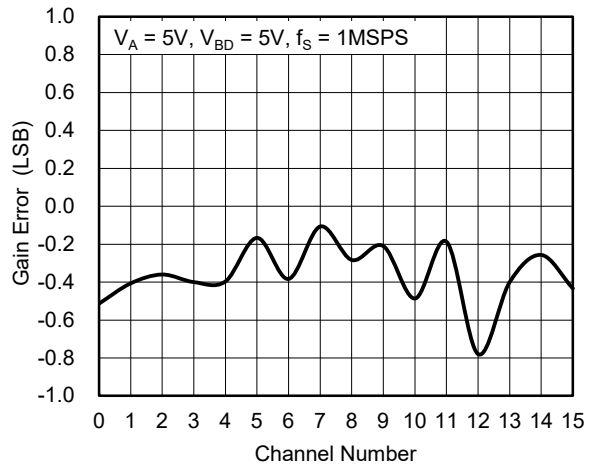


Integral Nonlinearity Variation Across Channels

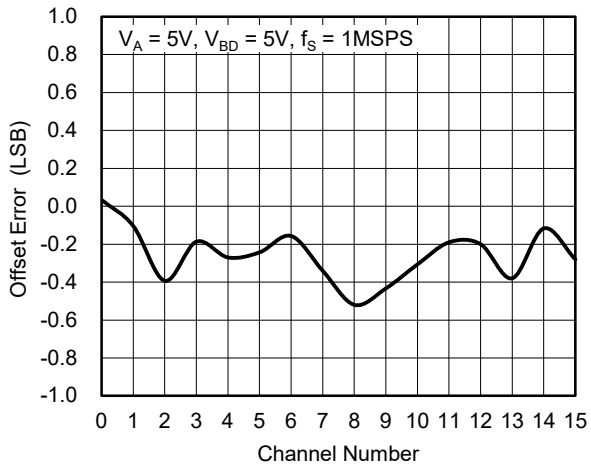


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

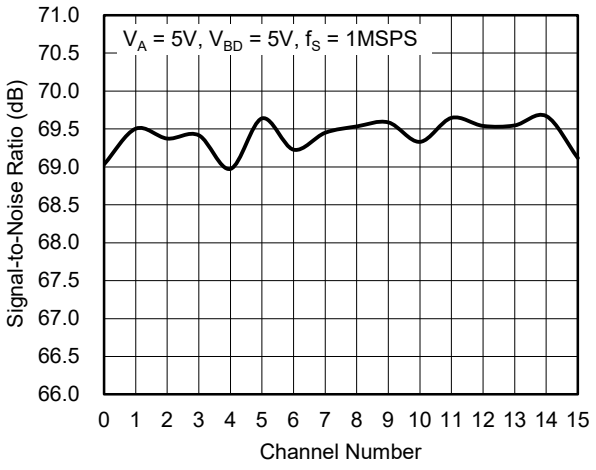
Gain Error Variation Across Channels



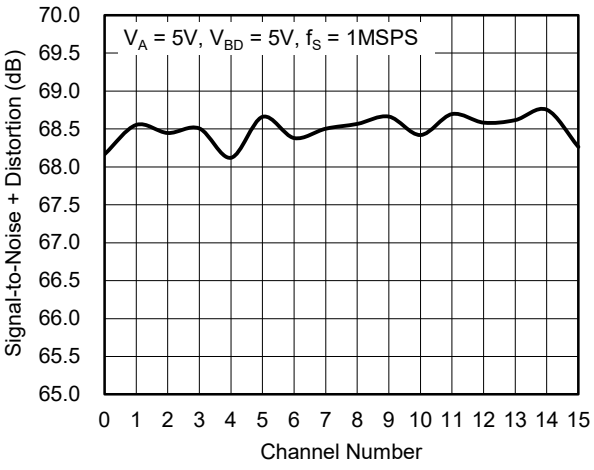
Offset Error Variation Across Channels



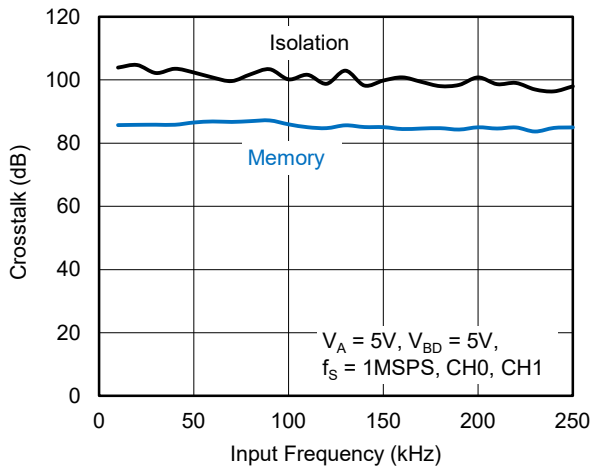
Signal-to-Noise Ratio Variation Across Channels



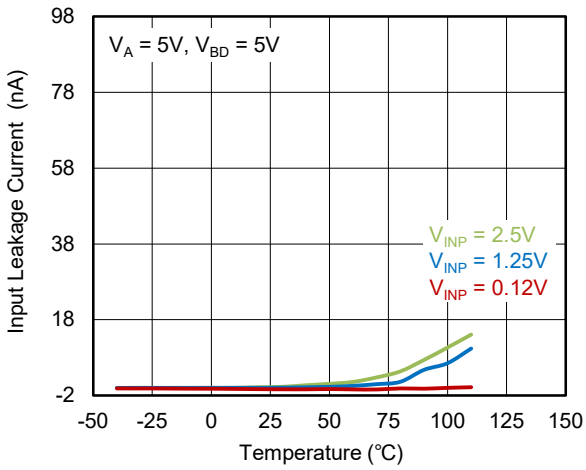
Signal-to-Noise + Distortion Variation Across Channels



Crosstalk vs. Input Frequency

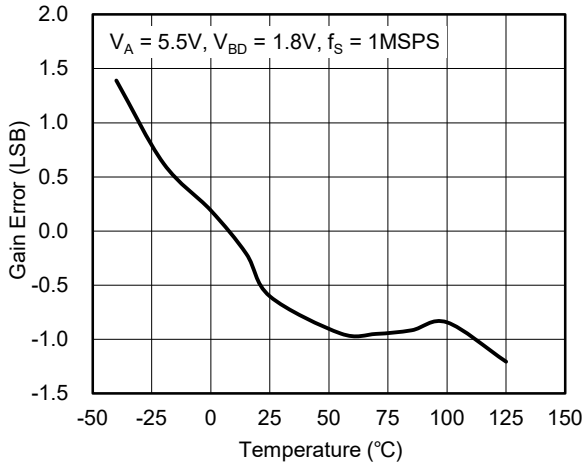


Input Leakage Current vs. Temperature

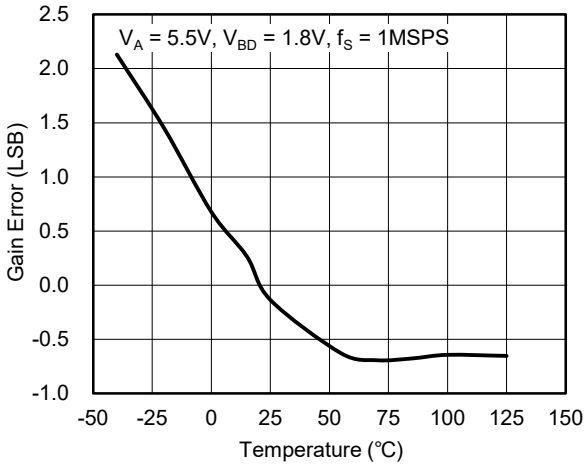


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

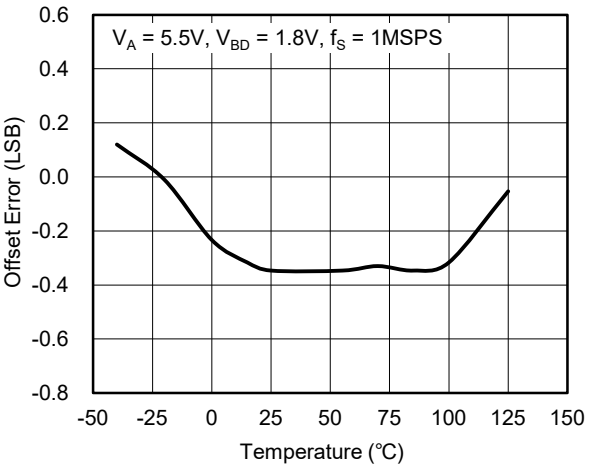
Gain Error vs. Temperature (Range 1)



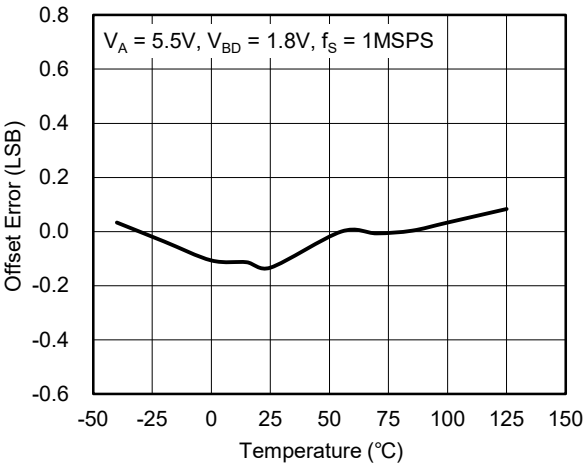
Gain Error vs. Temperature (Range 2)



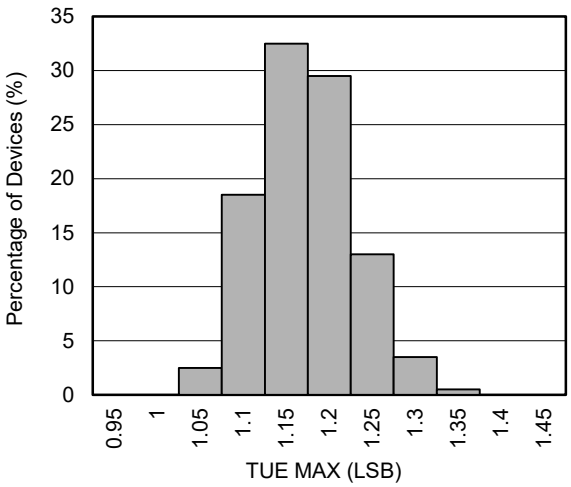
Offset Error vs. Temperature (Range 1)



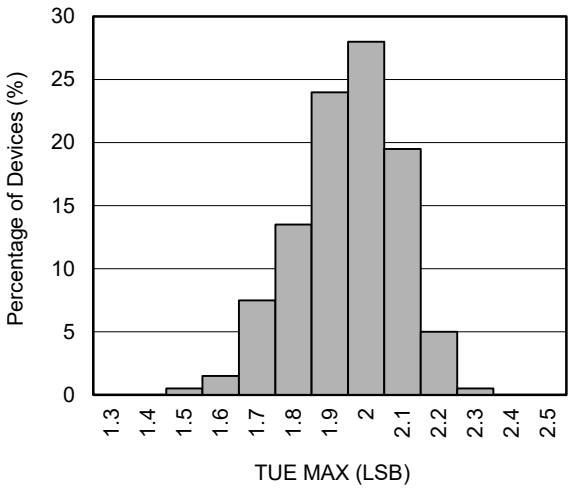
Offset Error vs. Temperature (Range 2)



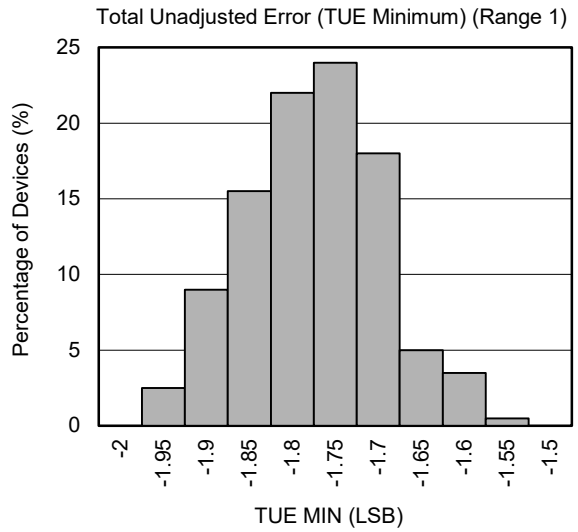
Total Unadjusted Error (TUE Maximum) (Range 1)

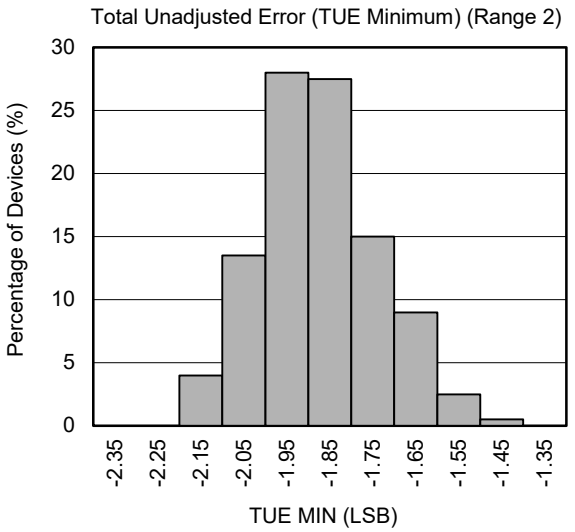


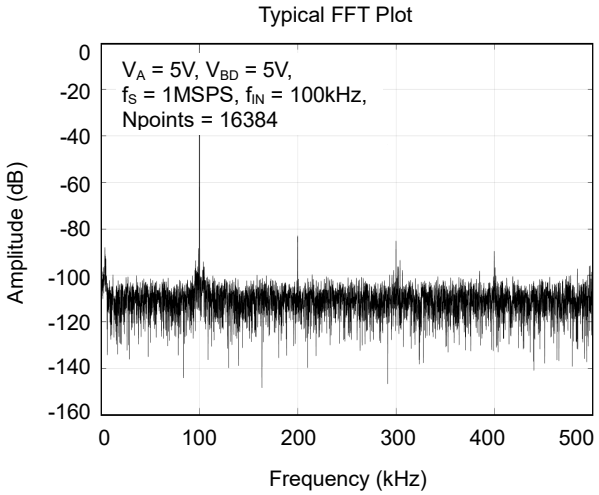
Total Unadjusted Error (TUE Maximum) (Range 2)



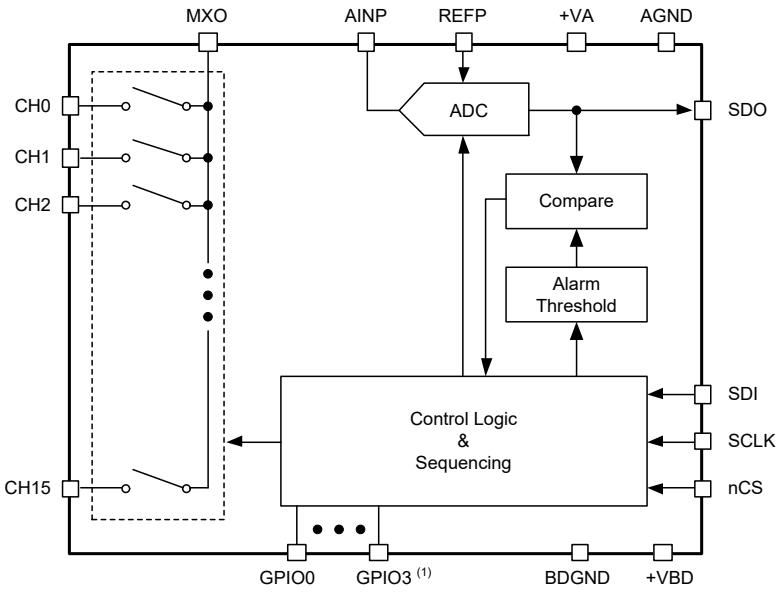
TYPICAL PERFORMANCE CHARACTERISTICS (continued)







FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. There are 4 GPIOs in TSSOP package and 1 GPIO in TQFN package.

Figure 3. Block Diagram

TYPICAL APPLICATION CIRCUITS

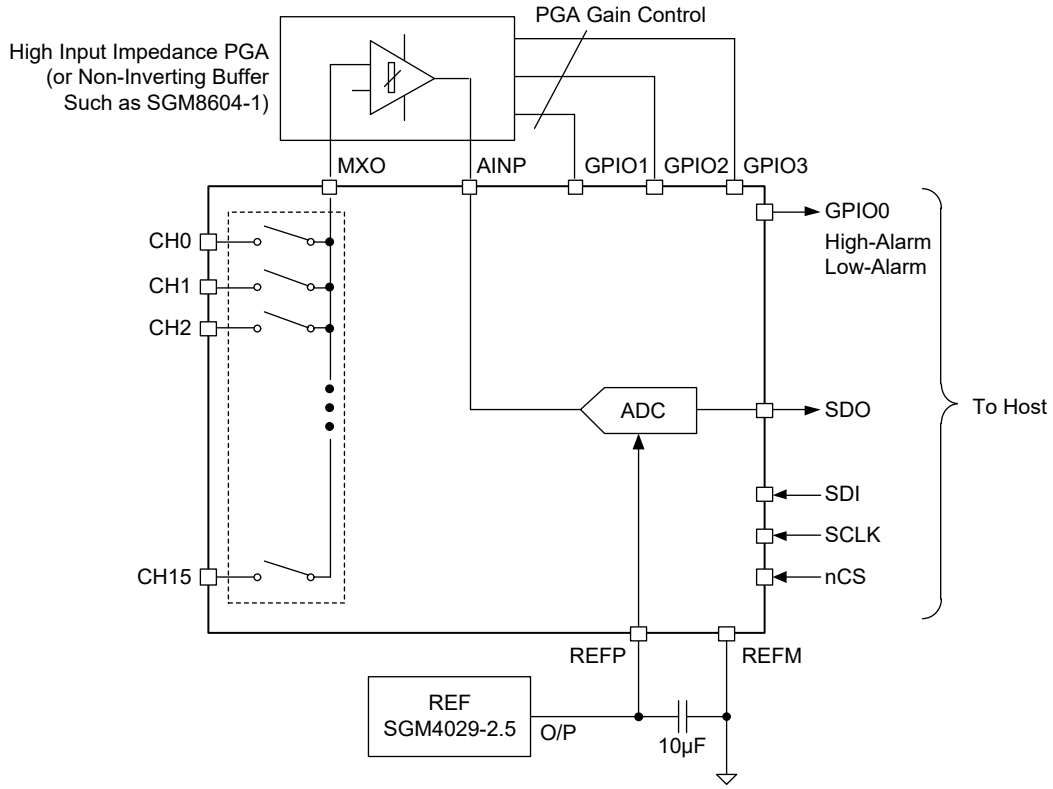


Figure 4. Typical Application Circuit

DETAILED DESCRIPTION

Overview

The SGM5200 is a 12-bit, high-speed, low-power and successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample/hold function. The analog inputs to the SGM5200 are provided to CHx input channels. All input channels share a common analog ground AGND. The SGM5200 has multiplexer breakout feature which allows user to connect the signal conditioning circuit between multiplexer output (MXO) and ADC input (AINP). This feature enables use of common signal conditioning block for the input signal which exhibit similar performance characteristics. SGM5200 can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep through the input channels automatically.

Figure 1 and Figure 2 show device operation timing. Device operation is controlled with nCS, SCLK and SDI. The device outputs its data on SDO.

Each frame begins with the falling edge of nCS. With the falling edge of nCS, the input signal from the selected channel is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The 16-bit data word contains a 4-bit channel address, followed by a 12-bit conversion result in MSB first format. There is an option to read the GPIO status instead of the channel address. (Refer to Table 1, Table 2 and Table 5 for more details.)

The device selects a new multiplexer channel on the 2nd SCLK falling edge. The acquisition phase starts on the 14th SCLK rising edge. On the next nCS falling edge, the acquisition phase will end and the device starts a new frame.

The TSSOP packaged device has four general purpose IO (GPIO0 - GPIO3) pins while TQFN version has only one GPIO0 pin. The four pins can be individually programmed as GPO or GPI. It is also possible to use them for pre-assigned functions, refer to Table 9. GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the nCS falling edge as per the SDI data written in previous frame.

Similarly the device latches GPI status on the nCS falling edge and outputs the GPI data on the SDO line (if GPI read is enabled by writing DI4 = 1 in the previous frame) in the same frame starting with the nCS falling edge.

The falling edge of nCS clocks out DO15 (the first bit of the 4-bit channel address) and remaining address bits are clocked out on every falling edge of SCLK until the third falling edge. The conversion result MSB is clocked out on the 4th SCLK falling edge and LSB on the 15th falling edge respectively for 12-bit. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK. The nCS can be asserted (pulled high) only after 16 clocks have elapsed.

The device reads a 16-bit word on the SDI pin while it outputs the data on the SDO pin. SDI data is latched on every rising edge of SCLK starting with the 1st clock as shown in Figure 2. nCS can be asserted (pulled high) only after 16 clocks have elapsed.

The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits, the device flags out an alarm on GPIO0/GPIO1 depending on the GPIO program register settings (refer to Table 9). The alarm is asserted (under the alarm conditions) on the 12th falling edge of SCLK in the same frame when a data conversion is in progress. The alarm output is reset on the 10th falling edge of SCLK in the next frame.

Reference

The SGM5200 can operate with an external 2.5V ± 10mV reference. A clean, low noise and well-decoupled reference voltage on the REFP pin is required to ensure good performance of the converter. A low noise bandgap reference can be used to drive this pin. A 10μF ceramic decoupling capacitor is required between the REFP and REFM pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

Power Saving

The SGM5200 offers a power-down feature to save power when not in use. There are two ways to power down the device. It can be powered down by writing DI5 = 1 in the mode control register (refer to Table 1, Table 2 and Table 5); in this case, the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to power down the device is through GPIO. GPIO3 can act as the nPD input (refer to Table 9, for assigning this functionality to GPIO3). This is an asynchronous and active low input. The device powers down instantaneously after GPIO3 (nPD) = 0. The device will power up again on the nCS falling edge while DI5 = 0 in the mode control register and GPIO3 (nPD) = 1.

DETAILED DESCRIPTION (continued)

Device Functional Modes

Channel Sequencing Modes

There are three modes for channel sequencing, namely manual mode, auto-1 mode and auto-2 mode. Mode selection is done by writing into the mode control register (refer to Table 1, Table 2 and Table 5). A new multiplexer channel is selected on the 2nd falling edge of SCLK (as shown in Figure 1) in all three modes.

Manual Mode

When configured to operate in manual mode, the next channel to be selected is programmed in each frame and the device selects the programmed channel in the next frame. On power-up or after reset the default channel is 'channel 0' and the device is in manual mode.

Auto-1 Mode

In this mode, the device scans pre-programmed channels in ascending order. A new multiplexer channel is selected every frame on the 2nd falling edge of SCLK. There is a separate program register for pre-programming the channel sequence. Table 3 and Table 4 show auto-1 program register settings.

Once programmed the device retains program register settings until the device is powered down, reset or reprogrammed. It is allowed to exit and re-enter the auto-1 mode any number of times without disturbing program register settings.

The auto-1 program register is reset to "FFFF" hex for SGM5200 upon device power-up or reset; implying the device scans all channels in ascending order.

Auto-2 Mode

In this mode, the user can configure the program register to select the last channel in the scan sequence. The device scans all channels from channel 0 up to and including the last channel in ascending order. The multiplexer channel is selected every frame on the 2nd falling edge of SCLK. There is a separate program register for preprogramming of the last channel in the sequence (multiplexer depth). Table 6 lists the auto-2 program register settings for selection of the last channel in the sequence.

Once programmed the device retains program register settings until the device is powered down, reset or reprogrammed. It is allowed to exit and re-enter the auto-2 mode any number of times without disturbing program register settings.

On power-up or reset the bits DI[9:6] of the auto-2 program register are reset to "F" hex for SGM5200; implying the device scans all channels in ascending order.

Device Programming and Mode Control

The following section describes device programming and mode control. The device features two types of registers to configure and operate the device in different modes. These registers are referred as configuration registers. There are two types of configuration registers namely mode control register and program registers.

Mode Control Register

A mode control register is configured to operate the device in one of three channel sequencing modes, namely manual mode, auto-1 mode and auto-2 mode. It is also used to control user programmable features like range selection, device power-down control. GPIO read control and writing output data into the GPIO.

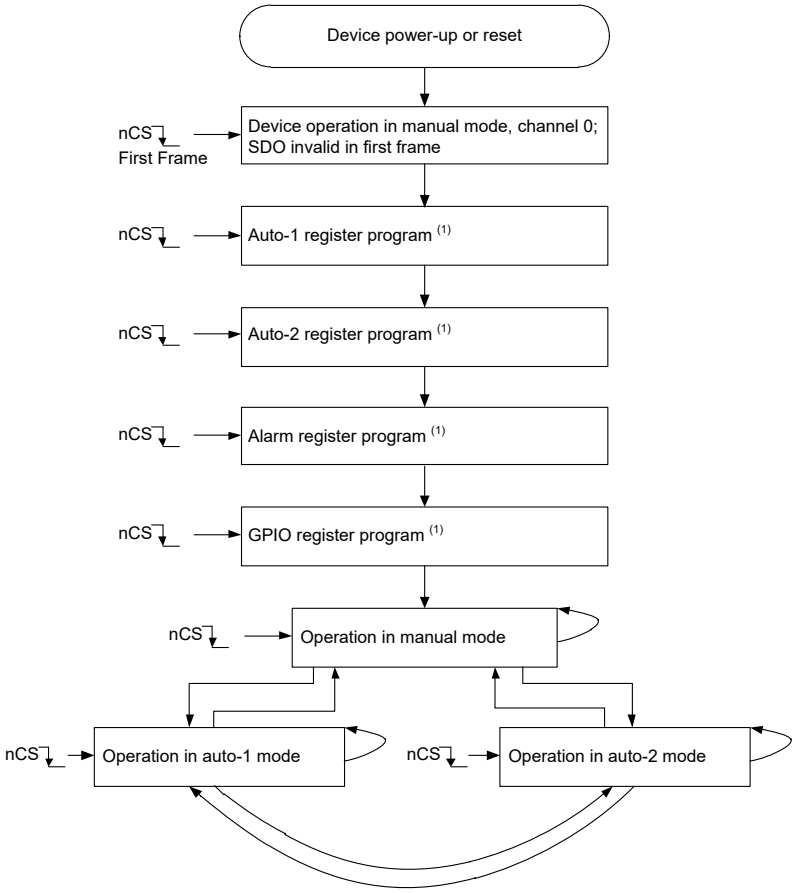
Program Registers

The program registers are used for device configuration settings and are typically programmed once on power-up or after device reset. There are different program registers such as auto-1 mode programming for preprogramming the channel sequence, auto-2 mode programming for selection of the last channel in the sequence, alarm programming for all 16 channels and GPIO for individual pin configuration as GPI or GPO or a pre-assigned function.

Device Power-Up Sequence

The device power-up sequence is shown in Figure 5. By default, the mode control register is configured for manual mode and the default channel is channel 0. As explained previously, the device offers program registers to configure user programmable features like GPIOs, Alarms and to preprogram the channel sequence for auto modes. At 'power-up or on reset', these registers are set to the default values listed in Table 1 to Table 9. On power-up or after reset, it is required to program mode control register and program registers to required mode of operation. Once configured, the device is ready to use in any of the three channel sequencing modes namely manual, auto-1 and auto-2.

DETAILED DESCRIPTION (continued)



NOTES:
1. The device continues its operation in manual mode channel 0 throughout the programming sequence and outputs valid conversion results. It is possible to change channel, range, GPIO by inserting extra frames in between two programming blocks. It is also possible to bypass any programming block if the user does not intend to use that feature.
2. It is possible to reprogram the device at any time during operation, regardless of what mode the device is in. During programming the device continues its operation in whatever mode it is in and outputs valid data.

Figure 5. Device Power-Up Sequence

DETAILED DESCRIPTION (continued)

Operating in Manual Mode

Figure 6 illustrates the steps involved in operating in manual channel sequencing mode. Table 1 lists the mode control register settings for manual mode. There are no program registers in manual mode.

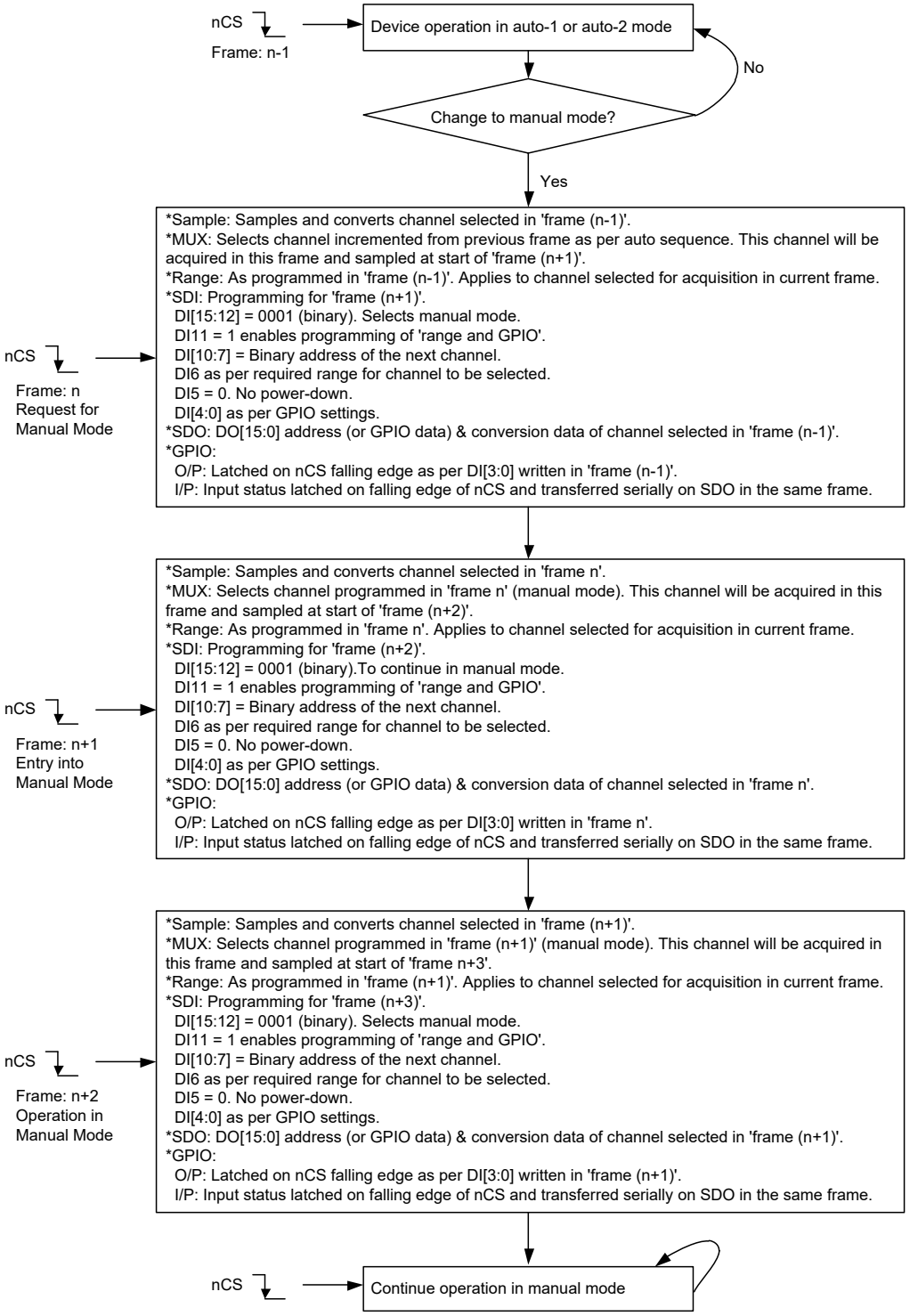


Figure 6. Entering and Running in Manual Channel Sequencing Mode

DETAILED DESCRIPTION (continued)

Table 1. Mode Control Register Settings for Manual Mode

Bits	Reset State	Logic State	Function			
DI[15:12]	0001	0001	Selects manual mode.			
DI11	0	1	Enables programming of bits DI[6:0].			
		0	Device retains values of DI[6:0] from the previous frame.			
DI[10:7]	0000		This 4-bit data represents the address of the next channel to be selected in the next frame. DI10: MSB and DI7: LSB. For example, 0000 represents channel 0, 0001 represents channel 1 and so forth.			
DI6	0	0	Selects 0V to V_{REF} input range (Range 1).			
		1	Selects 0V to 2 × V_{REF} input range (Range 2).			
DI5	0	0	Device normal operation (no power-down).			
		1	Device powers down on the 16th SCLK falling edge.			
DI4	0	0	SDO outputs current channel address of the channel on DO[15:12] followed by 12-bit conversion result on DO[11:0].			
		1	GPIO3 - GPIO0 data (both input and output) is mapped onto DO[15:12] in the order shown below. Lower data bits DO[11:0] represent 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3 (1)	GPIO2 (1)	GPIO1 (1)	GPIO0 (1)
DI[3:0]	0000		GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below.			
			DI3	DI2	DI1	DI0
			GPIO3 (1)	GPIO2 (1)	GPIO1 (1)	GPIO0 (1)

NOTE: 1. GPIO1 to GPIO3 are available only in TSSOP packaged device. TQFN device offers GPIO0 only.

Figure 7 shows an example in which manual mode is used to scan channels 4, 7 and 9. The command to select channel 4 (CH4) is issued in the n^{th} frame and the data corresponding to CH4 is available in the $(n+2)^{th}$ frame. Internally, the SDI command is parsed and on the rising edge of nCS of the $(n+1)^{th}$ frame and the MUX switches accordingly on the 2^{nd} falling edge of SCLK in this frame. On the rising edge of nCS of the $(n+2)^{th}$ frame, the input signal for CH4 is sampled and the ADC sends the conversion data in this third frame. The device follows the same steps and the ADC sends the conversion data for CH7 and CH9 in the subsequent two frames.

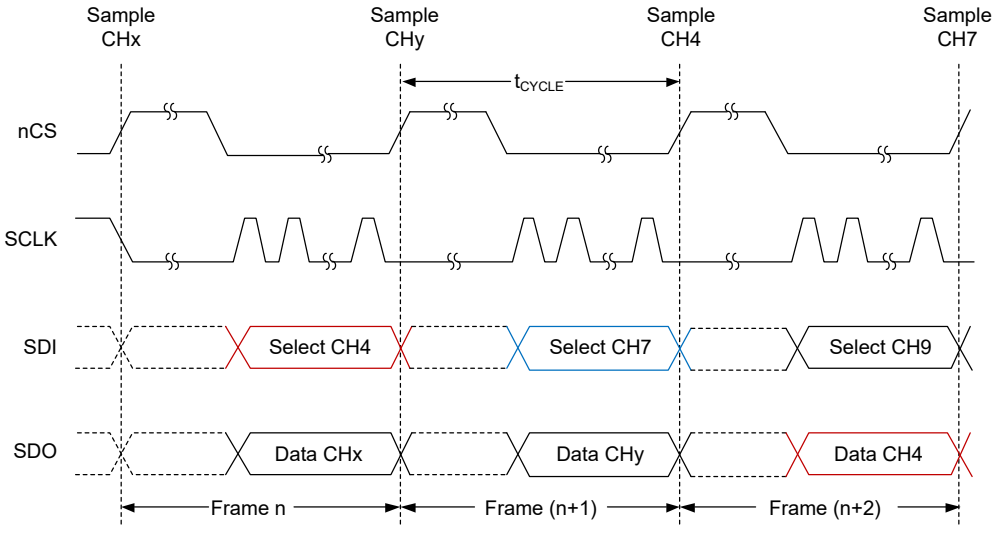


Figure 7. Example Manual Mode Timing Diagram

DETAILED DESCRIPTION (continued)

Operating in Auto-1 Mode

Figure 8 illustrates the steps involved in entering and operating in auto-1 channel sequencing mode. Table 2 lists the mode control register settings for auto-1 mode.

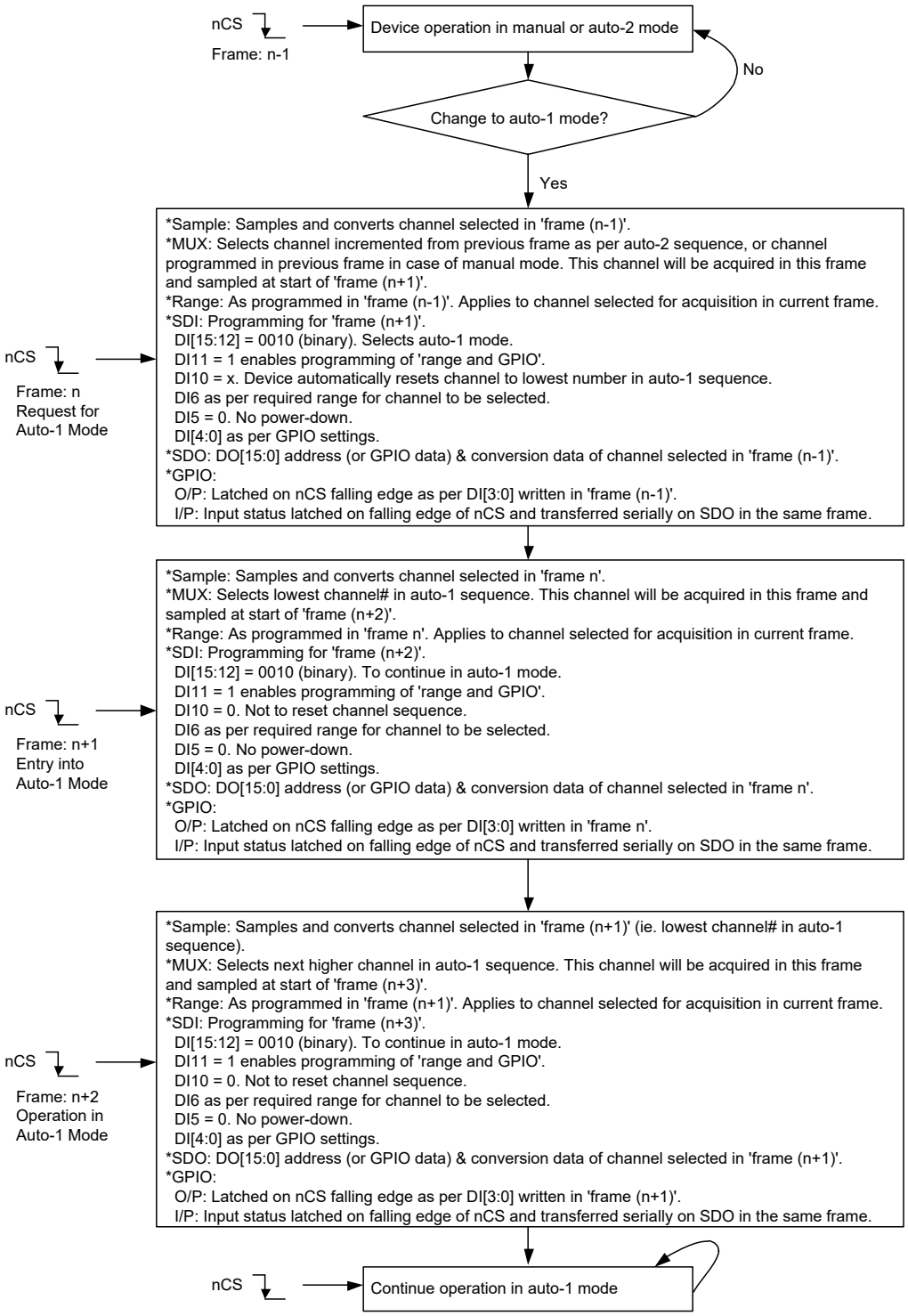


Figure 8. Entering and Running in Auto-1 Channel Sequencing Mode

DETAILED DESCRIPTION (continued)

Table 2. Mode Control Register Settings for Auto-1 Mode

Bits	Reset State	Logic State	Function			
DI[15:12]	0001	0010	Selects auto-1 mode.			
DI11	0	1	Enables programming of bits DI[10:0].			
		0	Device retains values of DI[10:0] from previous frame.			
DI10	0	1	The channel counter is reset to the lowest programmed channel in the auto-1 program register.			
		0	The channel counter increments every conversion (no reset).			
DI[9:7]	000	xxx	Do not care.			
DI6	0	0	Selects 0V to V_{REF} input range (Range 1).			
		1	Selects 0V to 2 × V_{REF} input range (Range 2).			
DI5	0	0	Device normal operation (no power-down).			
		1	Device powers down on the 16th SCLK falling edge.			
DI4	0	0	SDO outputs current channel address of the channel on DO[15:12] followed by 12-bit conversion result on DO[11:0].			
		1	GPIO3 - GPIO0 data (both input and output) is mapped onto DO[15:12] in the order shown below. Lower data bits DO[11:0] represent 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3 (1)	GPIO2 (1)	GPIO1 (1)	GPIO0 (1)
DI[3:0]	0000		GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below.			
			DI3	DI2	DI1	DI0
			GPIO3 (1)	GPIO2 (1)	GPIO1 (1)	GPIO0 (1)

NOTE:1. GPIO1 to GPIO3 are available only in TSSOP packaged device. TQFN device offers GPIO0 only.

Consider a case where auto-1 mode is selected to scan channels 2 (CH2), 5 (CH5) and 6 (CH6) as represented in Figure 9. The program register for auto-1 mode must be programmed as described in Figure 9 before entering into this auto sequencing mode. The device enters into auto-1 mode on receiving the auto-1 mode command in the nth frame. This step causes the device to find the first enabled channel in ascending order and switch the MUX for CH2 in the $(n+1)^{th}$ frame. In the $(n+2)^{th}$ frame, the ADC samples the signal on CH2, shifts out the conversion results and the MUX also internally switches to CH5. In the $(n+3)^{th}$ frame, the ADC samples and shifts out the conversion result for CH5 and the MUX also internally switches to CH6. This process repeats until the last enabled channel is reached, in which case the process loops back to the first enabled channel. Entering auto-1 mode from any other mode also causes the device to restart from the first enabled channel. However, modifying the contents of the auto-1 mode program register while operating in auto-1 mode causes the device to scan for the next enabled channel.

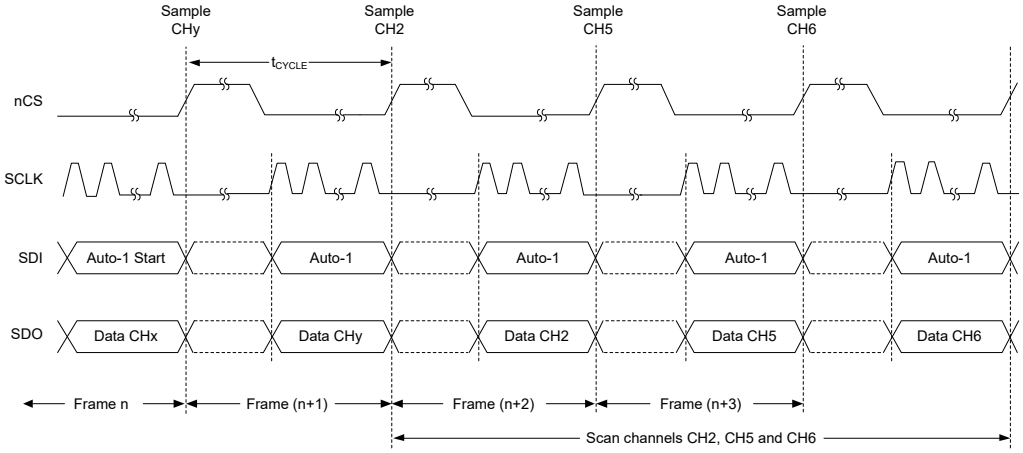
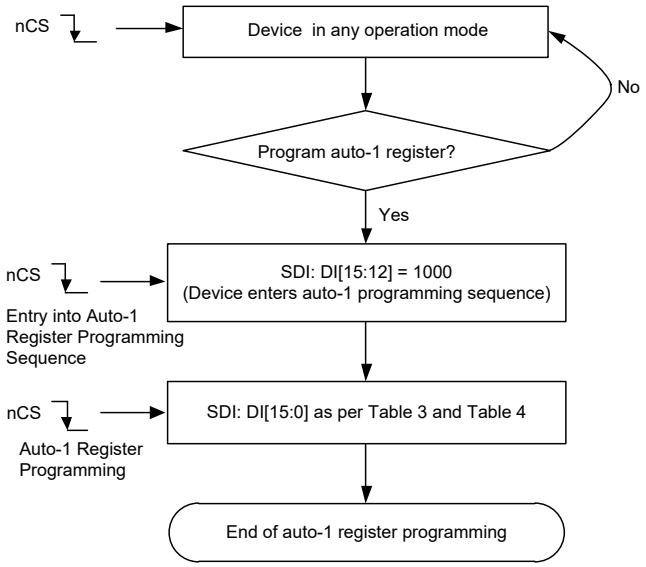


Figure 9. Example Auto-1 Mode Timing Diagram

DETAILED DESCRIPTION (continued)

The auto-1 program register is programmed (once on power-up or reset) to pre-select the channels for the auto-1 sequence. Auto-1 program register programming requires two nCS frames for complete programming. In the first nCS frame the device enters the auto-1 register programming sequence and in the second frame it programs the auto-1 program register. Refer to Table 2, Table 3 and Table 4 for complete details.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 10. Auto-1 Register Programming Flowchart

Table 3. Program Register Settings for Auto-1 Mode

Bits	Reset State	Logic State	Function
Frame 1			
DI[15:12]	NA	1000	Device enters auto-1 program sequence. Device programming is done in the next frame.
DI[11:0]	NA	Do not care.	
Frame 2			
DI[15:0]	All '1'	1 (Individual Bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example, DI15 → CH15, DI14 → CH14 … DI0 → CH0.
		0 (Individual Bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example, DI15 → CH15, DI14 → CH14 … DI0 → CH0.

Table 4. Mapping of Channels to SDI Bits for the SGM5200

Device (1)	SDI Bits															
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI0	DI4	DI3	DI2	DI1	DI0
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

NOTE:
1. When operating in auto-1 mode, the device only scans the channels programmed to be selected.

DETAILED DESCRIPTION (continued)

Operating in Auto-2 Mode

Figure 11 illustrates the steps involved in entering and operating in auto-2 channel sequencing mode. Table 5 lists the mode control register settings for auto-2 mode.

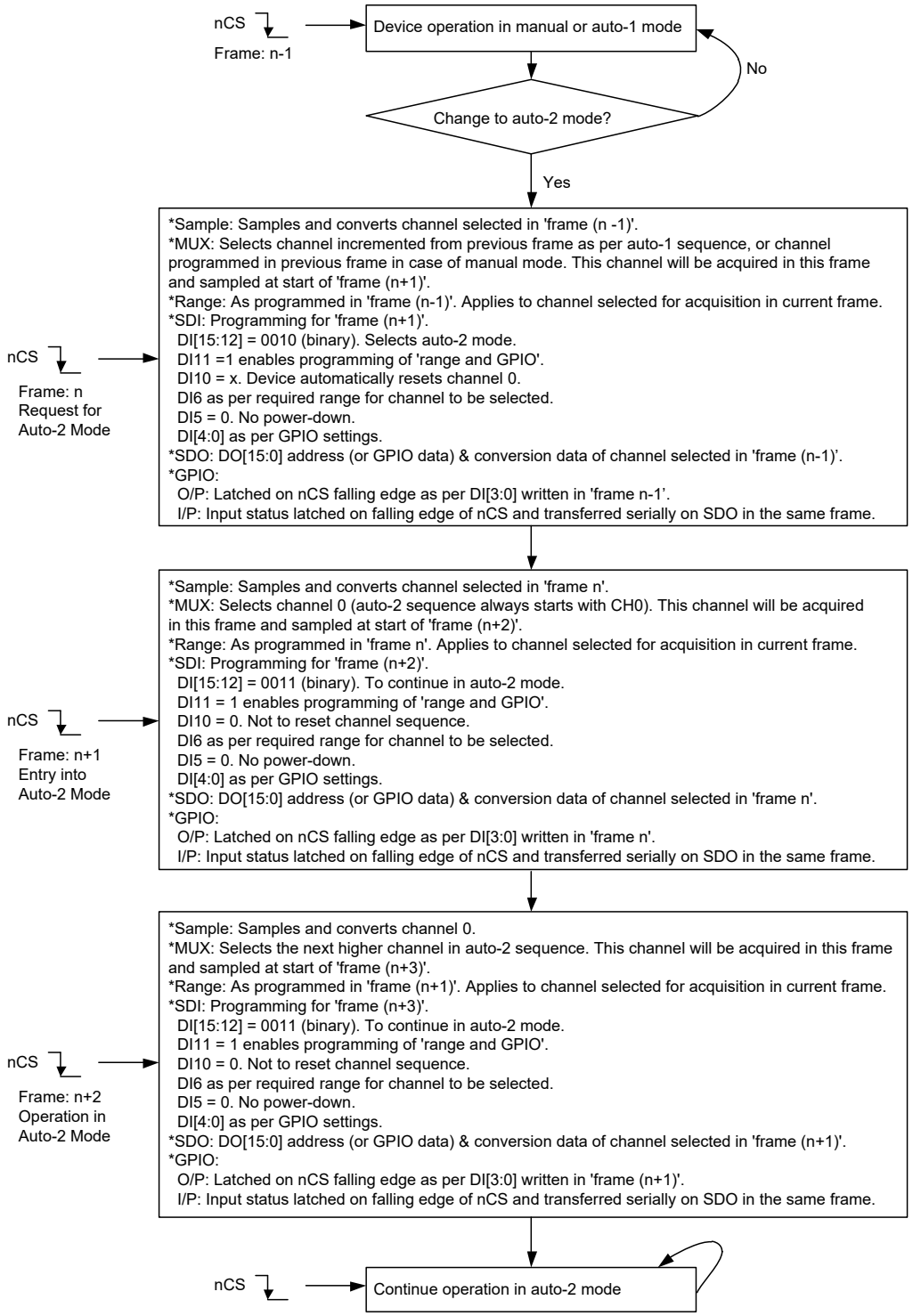


Figure 11. Entering and Running in Auto-2 Channel Sequencing Mode

DETAILED DESCRIPTION (continued)

Table 5. Mode Control Register Settings for Auto-2 Mode

Bits	Reset State	Logic State	Function			
DI[15:12]	0001	0011	Selects auto-2 mode.			
DI11	0	1	Enables programming of bits DI[10:0].			
		0	Device retains values of DI[10:0] from the previous frame.			
DI10	0	1	Channel number is reset to CH0.			
		0	Channel counter increments every conversion (no reset).			
DI[9:7]	000	xxx	Do not care.			
DI6	0	0	Selects V_{REF} input range (Range 1).			
		1	Selects 2 × V_{REF} input range (Range 2).			
DI5	0	0	Device normal operation (no power-down).			
		1	Device powers down on the 16th SCLK falling edge.			
DI4	0	0	SDO outputs the current channel address of the channel on DO[15:12] followed by the 12-bit conversion result on DO[11:0].			
		1	GPIO3 - GPIO0 data (both input and output) is mapped onto DO[15:12] in the order shown below. Lower data bits DO[11:0] represent the 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3 (1)	GPIO2 (1)	GPIO1 (1)	GPIO0 (1)
DI[3:0]	0000		GPIO data for the channels configured as output. Device ignores data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below.			
			DI3	DI2	DI1	DI0
			GPIO3 (1)	GPIO2 (1)	GPIO1 (1)	GPIO0 (1)

NOTE: 1. GPIO1 to GPIO3 are available only in TSSOP packaged device. TQFN device offers GPIO0 only.

Figure 12 shows an example in which auto-2 mode is used to scan channels 0, 1 and 2. Auto-2 mode is selected to scan all channels until channel 2 (CH2) in ascending order by programming the auto-2 register as described in Figure 12. The device enters auto-2 mode on receiving the auto-2 mode command in the n^{th} frame. This step causes the MUX to switch to CH0 in the $(n+1)^{th}$ frame. In the $(n+2)^{th}$ frame, the ADC samples and shifts out the conversion results for CH0 because the MUX internally switches to CH1. In the $(n+3)^{th}$ frame, the ADC samples and the shifts out the conversion result for CH1 and the MUX also switches to CH2 and so on. When this process reaches the maximum selected channel, CH2 in this case, the device returns to CH0 and repeats the cycle as long as the device remains in auto-2 mode. Entering auto-2 mode from any other mode also causes the device to restart from CH0. Additionally, modifying the contents of the for auto-2 program register while operating in auto-2 also causes the device to scan for restart from CH0.

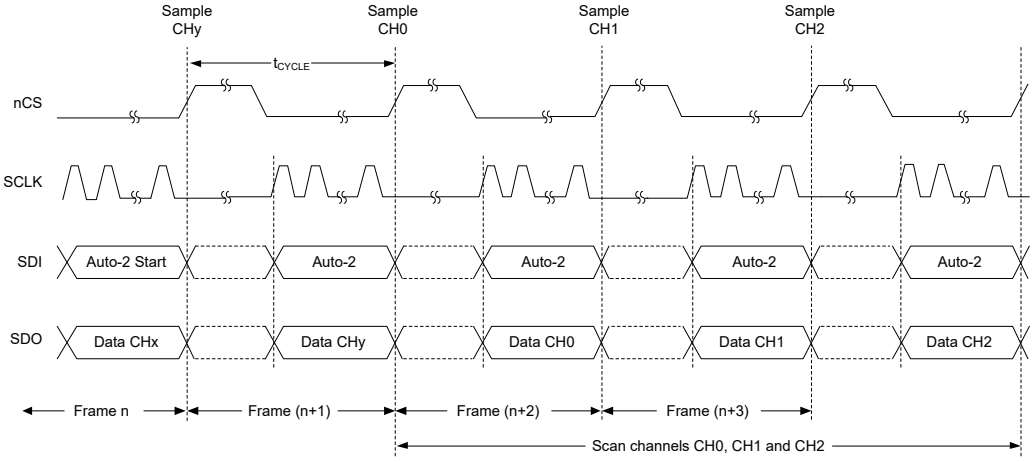


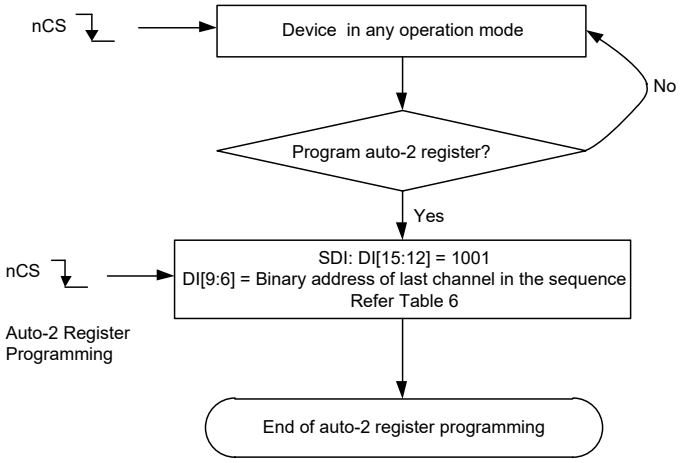
Figure 12. Example Auto-2 Mode Timing Diagram

DETAILED DESCRIPTION (continued)

The auto-2 program register is programmed (once on power-up or reset) to pre-select the last channel (or sequence depth) in the auto-2 sequence. Unlike auto-1 program register programming, auto-2 program register programming requires only 1 nCS frame for complete programming. See Figure 13 and Table 6 for complete details.

Continued Operation in a Selected Mode

Once a device is programmed to operate in one of the modes, the user may want to continue operating in the same mode. Mode control register settings to continue operating in a selected mode are detailed in Table 7.



NOTE: The device continues its operation in the selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 13. Auto-2 Register Programming Flowchart

Table 6. Program Register Settings for Auto-2 Mode

Bits	Reset State	Logic State	Function
DI[15:12]	NA	1001	Auto-2 program register is selected for programming.
DI[11:10]	NA	Do not care.	
DI[9:6]	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in auto-2 mode, the channel counter starts at CH0 and increments every frame until it equals "aaaa". The channel counter roles over to CH0 in the next frame.
DI[5:0]	NA	Do not care.	

Table 7. Continued Operation in a Selected Mode

Bits	Reset State	Logic State	Function
DI[15:12]	0001	0000	The device continues to operate in the selected mode. In auto-1 and auto-2 modes the channel counter increments normally, whereas in the Manual mode it continues with the last selected channel. The device ignores data on DI[11:0] and continues operating as per the previous settings. This feature is provided so that SDI can be held low when no changes are required in the mode control register settings.
DI[11:0]	All '0'	Device ignores these bits when DI[15:12] is set to 0000 logic state.	

DETAILED DESCRIPTION (continued)

Programming

Digital Output

As discussed previously in overview, the digital output of the SGM5200 device is SPI compatible. The Table 8 lists the output codes corresponding to various analog input voltages.

GPIO Registers

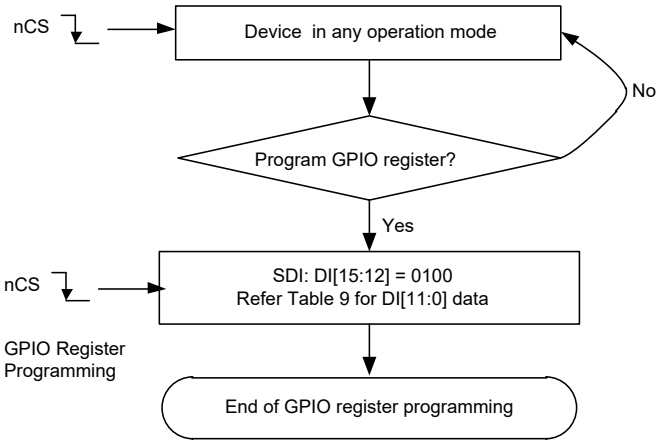
Note that GPIO0, GPIO1, GPIO2 and GPIO3 are available in the TSSOP package. Only GPIO0 is available in the TQFN package.

The device has four general purpose input and output (GPIO) pins. Each of the four pins can be independently programmed as general purpose output (GPO) or general purpose input (GPI). It is also possible to use the GPIOs for some pre-assigned functions (refer to Table 9 for details). GPO data can be written into the device through the SDI line. The device refreshes the GPO data on every nCS falling edge as per the SDI data written in the previous frame. Similarly, the device latches GPI status on the nCS falling edge and outputs it on SDO (if GPI is read enabled by writing DI4 = 1 during the previous frame) in the same frame starting on the nCS falling edge.

The details regarding programming the GPIO registers are illustrated in the flowchart in Figure 14. Table 9 lists the details regarding GPIO Register programming settings.

Table 8. Ideal Input Voltages and Output Codes

Description	Analog Value		Digital Output Straight Binary	
Full Scale Range	Range 1 → V_{REF}	Range 2 → 2 × V_{REF}		
Least Significant Bit (LSB)	V_{REF}/4096	2 × V_{REF}/4096	**Binary Code**	**Hex Code**
Full Scale	V_{REF} - 1LSB	2 × V_{REF} - 1LSB	1111 1111 1111	FFF
Midscale	V_{REF}/2	V_{REF}	1000 0000 0000	800
Midscale - 1LSB	V_{REF}/2 - 1LSB	V_{REF} - 1LSB	0111 1111 1111	7FF
Zero	0V	0V	0000 0000 0000	000



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 14. GPIO Program Register Programming Flowchart

DETAILED DESCRIPTION (continued)

Table 9. GPIO Program Register Settings

Bits	Reset State	Logic State	Function
DI[15:12]	NA	0100	Device selects GPIO program registers for programming.
DI[11:10]	00	00	Do not program these bits to any logic state other than '00'.
DI9	0	1	Device resets all registers in the next nCS frame to the reset state shown in the corresponding tables (it also resets itself).
		0	Device normal operation.
DI8	0	1	Device configures GPIO3 as the device power-down input.
		0	GPIO3 remains general purpose I or O. Program 0 for TQFN packaged device.
DI7	0	1	Device configures GPIO2 as device range input.
		0	GPIO2 remains general purpose I or O. Program 0 for TQFN packaged device.
DI[6:4]	000	000	GPIO1 and GPIO0 remain general purpose I or O. Valid setting for TQFN packaged device.
		xx1	Device configures GPIO0 as 'high or low' alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for TQFN packaged device.
		010	Device configures GPIO0 as high alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for TQFN packaged device.
		100	Device configures GPIO1 as low alarm output. This is an active high output. GPIO0 remains general purpose I or O. Setting not allowed for TQFN packaged device.
		110	Device configures GPIO1 as low alarm output and GPIO0 as a high alarm output. These are active high outputs. Setting not allowed for TQFN packaged device.
Note: The following settings are valid for GPIO which are not assigned a specific function through bits DI[8:4].			
DI3	0	1	GPIO3 pin is configured as general purpose output. Program 1 for TQFN packaged device.
		0	GPIO3 pin is configured as general purpose input. Setting not allowed for TQFN packaged device.
DI2	0	1	GPIO2 pin is configured as general purpose output. Program 1 for TQFN packaged device.
		0	GPIO2 pin is configured as general purpose input. Setting not allowed for TQFN packaged device.
DI1	0	1	GPIO1 pin is configured as general purpose output. Program 1 for TQFN packaged device.
		0	GPIO1 pin is configured as general purpose input. Setting not allowed for TQFN packaged device.
DI0	0	1	GPIO0 pin is configured as general purpose output. Valid setting for TQFN packaged device.
		0	GPIO0 pin is configured as general purpose input. Valid setting for TQFN packaged device.

Alarm Thresholds for GPIO Pins

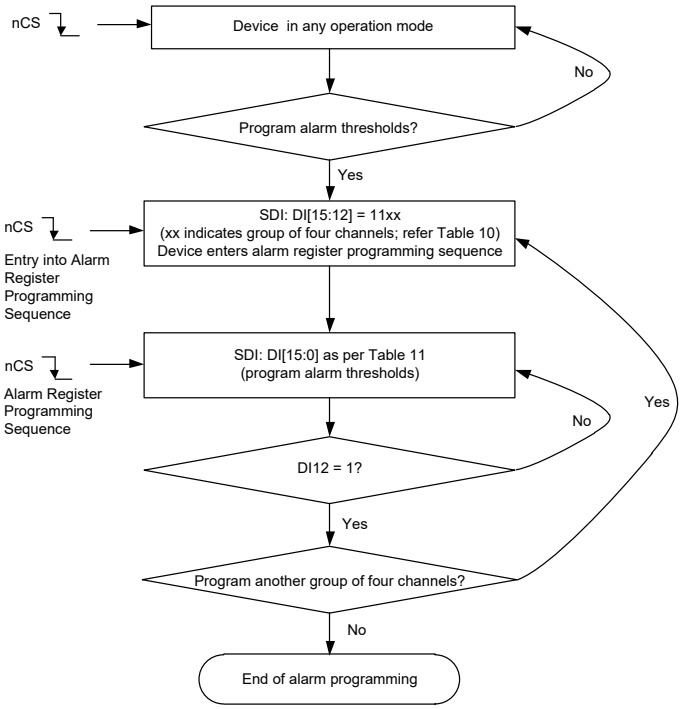
Each channel has two alarm program registers, one for setting the high alarm threshold and the other for setting the low alarm threshold. For ease of programming, two alarm programming registers per channel, corresponding to four consecutive channels, are assembled into one group (a total eight registers). There are four such groups for the 16-channel device respectively. The grouping of the various channels for each SGM5200 device is listed in Table 10. The details regarding programming the alarm thresholds are illustrated in the flowchart in Figure 15. Table 11 lists the details regarding the alarm program register settings.

Each alarm group requires 9 nCS frames for programming their respective alarm thresholds. In the first frame the device enters the programming sequence and in each subsequent frame it programs one of the registers from the group. The device offers a feature to program less than eight registers in one programming sequence. The device exits the alarm threshold programming sequence in the next frame after it encounters the first exit alarm program bit high.

Table 10. Grouping of Alarm Program Registers

Group NO.	Registers
0	High and low alarm for channel 0, 1, 2 and 3.
1	High and low alarm for channel 4, 5, 6 and 7.
2	High and low alarm for channel 8, 9, 10 and 11.
3	High and low alarm for channel 12, 13, 14 and 15.

DETAILED DESCRIPTION (continued)



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 15. Alarm Program Register Programming Flowchart

Table 11. Alarm Program Register Settings

Bits	Reset State	Logic State	Function
Frame 1			
DI[15:12]	NA	1100	Device enters 'alarm programming sequence' for group 0.
		1101	Device enters 'alarm programming sequence' for group 1.
		1110	Device enters 'alarm programming sequence' for group 2.
		1111	Device enters 'alarm programming sequence' for group 3.
Note: DI[15:12] = 11bb is the alarm programming request for group bb. Here 'bb' represents the alarm programming group number in binary format.			
DI[11:0]	NA	Do not care.	
Frame 2 and Onwards			
DI[15:14]	NA	cc	Where "cc" represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number "bbcc". "bb" is programmed in the first frame.
DI13	NA	1	High alarm register selection.
		0	Low alarm register selection.
DI12	NA	0	Continue alarm programming sequence in the next frame.
		1	Exit alarm programming in the next frame. Note: If the alarm programming sequence is not terminated using this feature then the device will remain in the alarm programming sequence state and all SDI data will be treated as alarm thresholds.
DI[11:10]	NA	xx	Do not care.
DI[9:0]	All ones for high alarm register and all zeros for low alarm register	This 10-bit data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit word of the 12-bit conversion result. The device sets off an alarm when the conversion result is higher (high alarm) or lower (low alarm) than this number. For 10-bit devices, all 10 bits of the conversion result are compared with the set threshold. For 8-bit devices, all 8 bits of the conversion result are compared with DI9 to DI2 and DI1, DI0 are 'do not care'.	

APPLICATION INFORMATION

In general applications, when the internal multiplexer is updated, the previously converted channel charge is stored in the 31pF internal input capacitance that disturbs the voltage at the newly selected channel. This disturbance is expected to settle to less than 1/2LSB during sampling (acquisition) time to avoid degrading converter performance. The initial absolute disturbance error at the channel input must be less than 0.5V to prevent source current saturation or slewing that causes significantly long settling times. Fortunately, significantly reducing disturbance error is easy to accomplish by simply placing a large enough capacitor at the input of each channel. Specifically, with a 300pF capacitor, instantaneous charge distribution keeps disturbance error less than 0.47V because the internal input capacitance can only hold up to 155pC (or 5V × 31pF). The remaining error must be corrected by the voltage source at each input, with impedance low enough to settle within 1/2LSB. Figure 16 shows the equivalent circuit model for the MUX and ADC.

Analog Input

The SGM5200 offers 12-bit ADC with the 16-channel multiplexer for analog inputs. The multiplexer output is available on the MXO pin. The AINP pin is the ADC input pin. The device offers flexibility for a system designer as both signals are accessible externally.

Typically it is convenient to short MXO to the AINP pin so that signal input to each multiplexer channel can be processed independently. In this condition, the source impedance of each channel is limited to 50Ω or less. Higher source impedance may affect the signal settling time after a multiplexer channel change. This condition can affect linearity and total harmonic distortion. Refer to Figure 17.

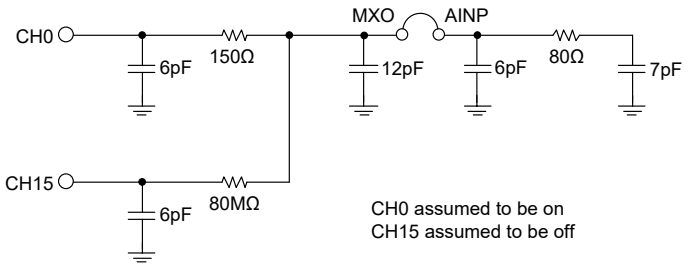
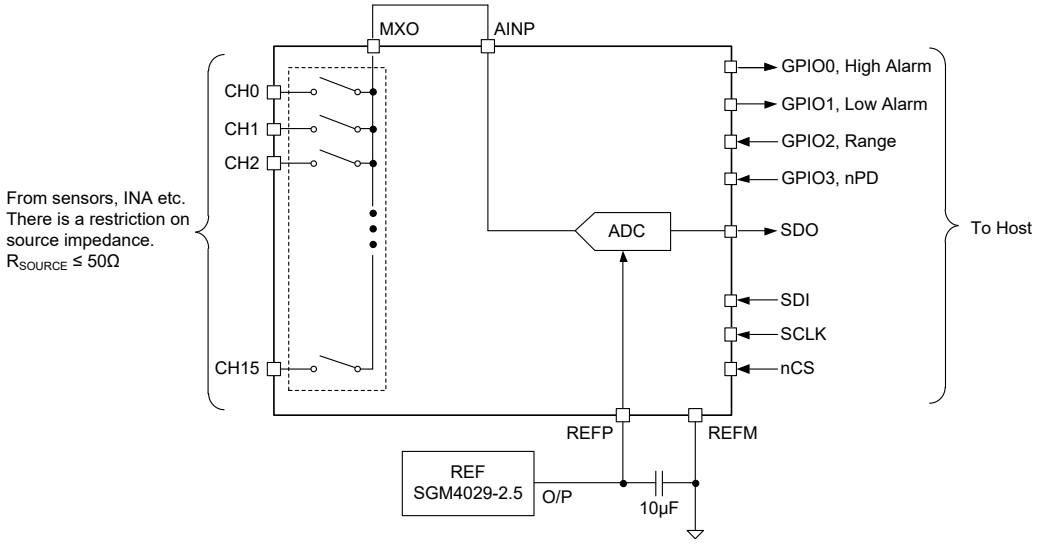


Figure 16. ADC and MUX Equivalent Circuit



NOTE: GPIO0, GPIO1, GPIO2 and GPIO3 are available only in TSSOP packaged device. TQFN device offers GPIO0 only. As a result, all references related to GPIO0 only are valid in case of TQFN packaged device.

Figure 17. Typical Application Diagram Showing MXO Shorted to AINP

APPLICATION INFORMATION (continued)

Another option is to add a common ADC driver buffer between the MXO and AINP pins, see Figure 18. This relaxes the restriction on source impedance to a large extent. Refer to Typical Characteristics section for the effect of source impedance on device performance. The typical characteristics show that the device has respectable performance with up to 1kΩ source impedance. This topology (including a common ADC driver) is useful when all channel signals are within the acceptable range of the ADC. In this case the user can save on signal conditioning circuit for each channel.

When the converter samples an input, the voltage difference between AINP and AGND is captured on the internal capacitor array. The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage and source impedance. The current into the SGM5200 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. When the converter goes into hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the CH0 - CH15 and AINP inputs should be within the limits specified. Outside of these ranges, converter linearity may not meet specifications.

Power Supply Recommendations

The SGM5200 is designed to operate from an analog supply voltage (V_A) range from 2.7V to 5.25V and a digital supply voltage (V_{BD}) range from 1.7V to 5.25V. Both supplies must be well regulated. The analog supply is always greater than or equal to the digital supply. A 1μF ceramic decoupling capacitor is required at each supply pin and must be placed as close as possible to the device.

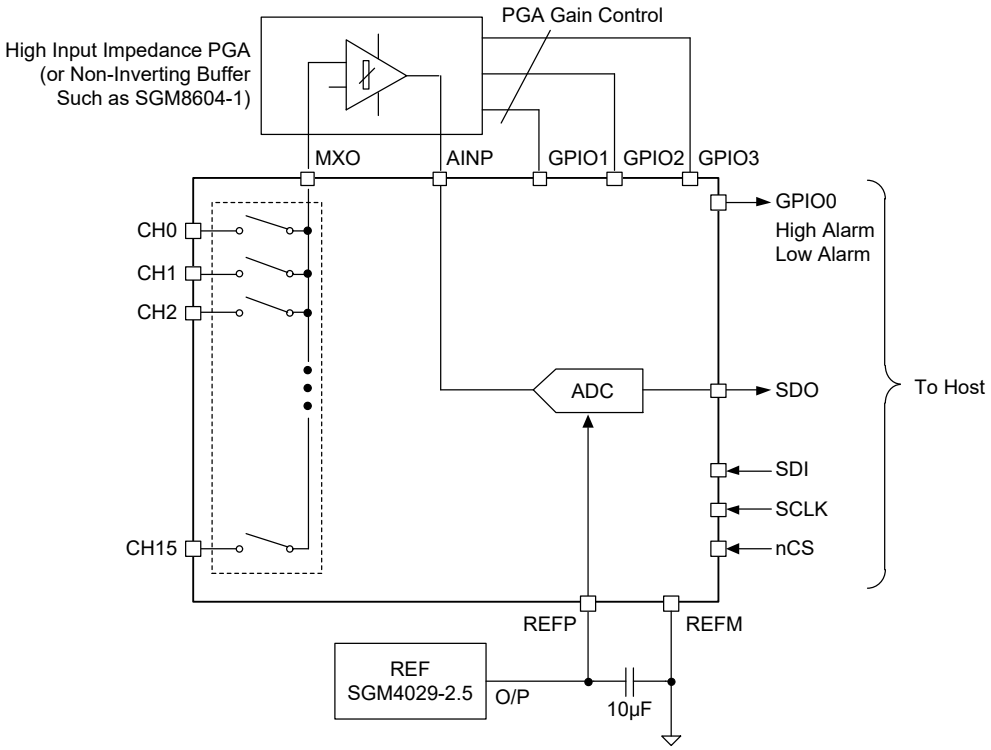


Figure 18. Typical Application Diagram Showing Common Buffer/PGA for All Channels

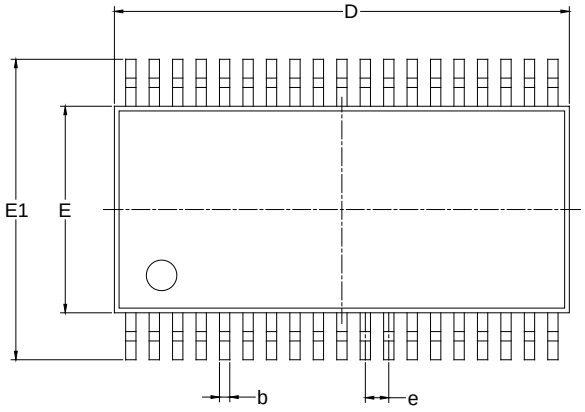
REVISION HISTORY

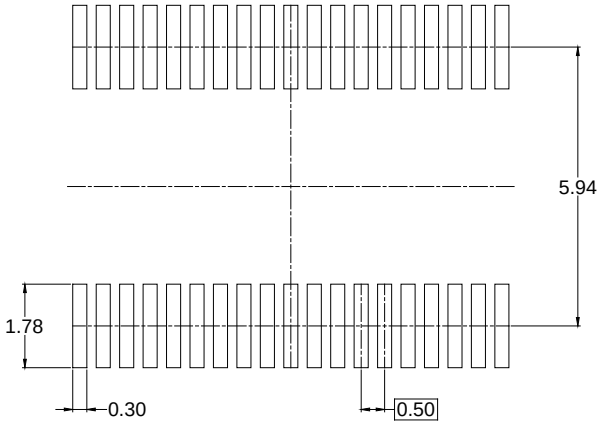
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (SEPTEMBER 2021) to REV.A	Page
Changed from product preview to production data	All

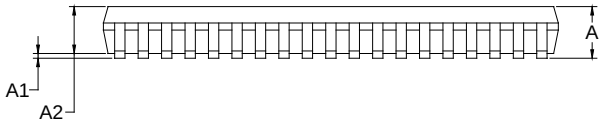
PACKAGE OUTLINE DIMENSIONS

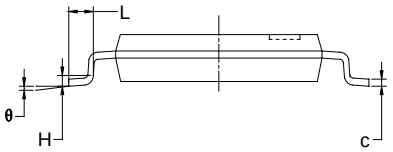
TSSOP-38





RECOMMENDED LAND PATTERN (Unit: mm)





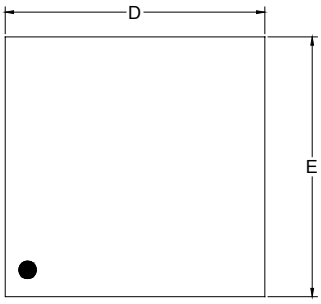
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.500 BSC		0.020 BSC	
H	0.250 TYP		0.010 TYP	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°

NOTES:

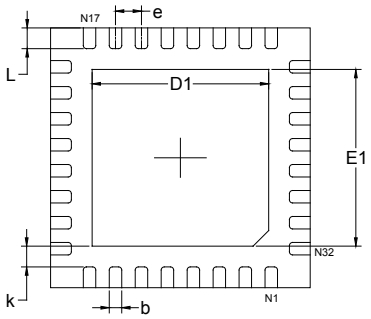
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

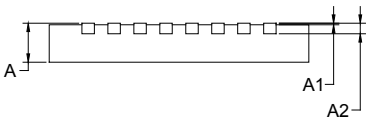
TQFN-5×5-32L



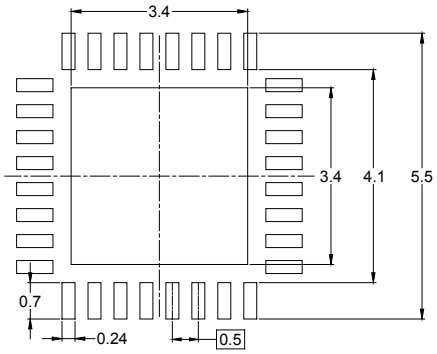
TOP VIEW



BOTTOM VIEW



SIDE VIEW

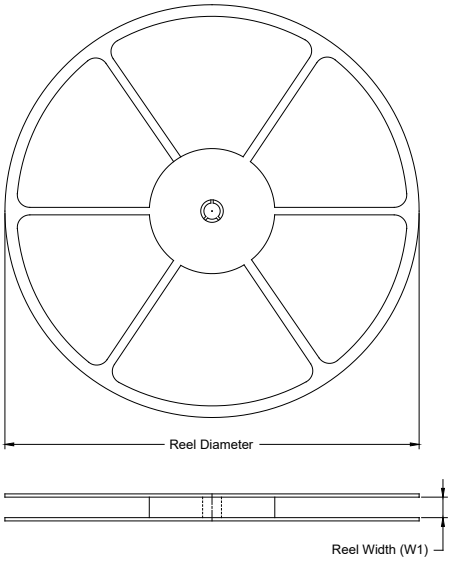


RECOMMENDED LAND PATTERN (Unit: mm)

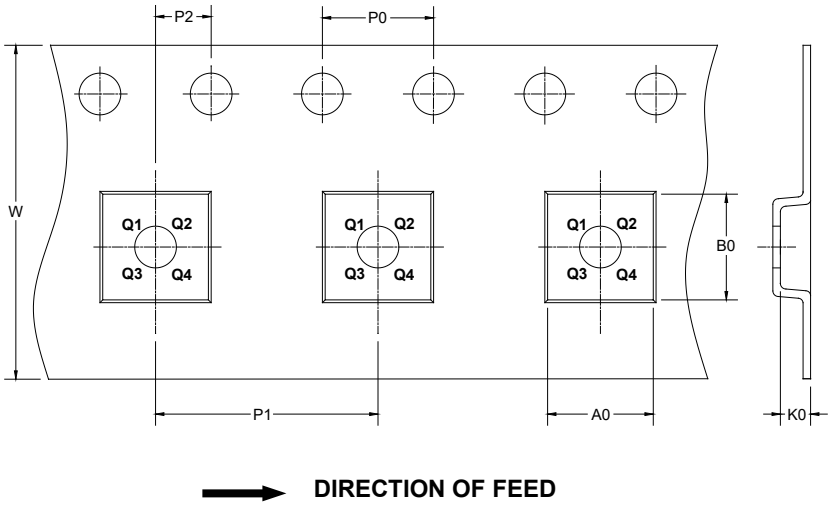
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E	4.924	5.076	0.194	0.200
E1	3.300	3.500	0.130	0.138
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.324	0.476	0.013	0.019

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



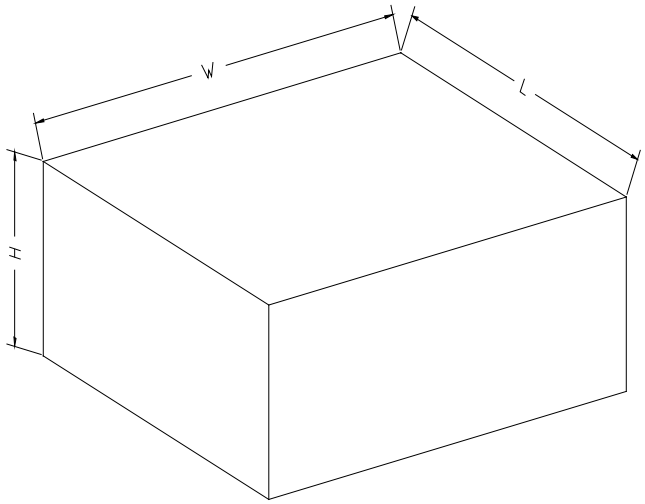
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-38	13″	16.4	6.80	10.20	1.60	4.0	8.0	2.0	16.0	Q1
TQFN-5×5-32L	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002