# SGM62110/SGM62111
# 2.5A Buck-Boost Converters with I²C Interface

## GENERAL DESCRIPTION

The SGM62110 and SGM62111 are 4-switch buck-boost converters with programmable I²C interface for simple configuration of integrated rich features. Synchronous rectification improves system efficiency which is friendly for battery operated applications. In addition, the programmable light load PFM (pulse frequency modulation) mode and low quiescent current (15μA, TYP) offer above 90% efficiency in the 10mA to 2A output current range.

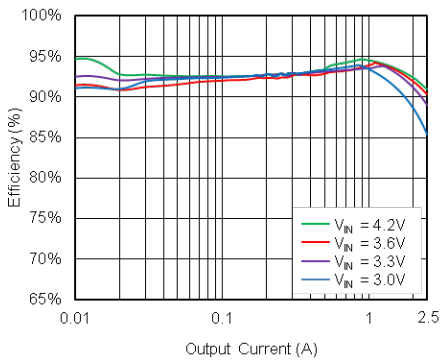
The devices are capable to operate in buck, boost or a novel 4-cycle buck-boost mode when the input voltage is close to or equal to the output voltage. The devices implement pre-defined mode transition thresholds to avoid undesired toggling between modes to reduce output voltage ripple.

Dynamic voltage scaling is enabled via VSEL pin and I²C controlled output voltage registers which allows the device to toggle output voltages based on application needs.

The SGM62110 and SGM62111 implement robust protection features such as over-temperature, input over-voltage, output over-current protections to protect device against unexpected system failure.

The SGM62110 and SGM62111 are available in a small WLCSP-2.21×1.40-15B package. High integration provides a compact solution with only four external components, allowing implementation in a PCB area as small as 39mm².

**Efficiency vs. Output Current**




## FEATURES

- **2.2V to 5.5V Input Voltage Range**
- **1.8V to 5.2V Output Voltage Range**
  - **2.5A Output Current for $V_{IN}$ ≥ 2.5V, $V_{OUT}$ = 3.3V**
  - **2.5A Output Current for $V_{IN}$ ≥ 2.8V, $V_{OUT}$ = 3.5V**
  - **2A Output Current for $V_{IN}$ ≥ 2.5V, $V_{OUT}$ = 3.5V**
- **3.3V or 3.45V Pre-Programmed Output Voltage (SGM62110)**
- **Programmed Output Voltage Prior to Start-up (SGM62111)**
- **Above 90% Efficiency for $I_{OUT}$ from 10mA to 2A**
- **15μA Quiescent Current**
- **User-Selectable Power-Save Mode**
- **Real Buck, Boost and Buck-Boost Modes**
- **Automatic Mode Transition**
- **I²C Interface (Up to 1MHz Clock Speed)**
- **Internal Soft-Start**
- **OTP, Input OVP and Output OCP Protections**
- **True Shutdown Function with Load Disconnect and Active Output Discharge**
- **Available in a Green WLCSP-2.21×1.40-15B Package**

## APPLICATIONS

Smartphones and Tablets
Pre-regulators and USB VCONN Supplies
TWS Earbud Chargers
General-Purpose Point-of-Load Regulators

## TYPICAL APPLICATION

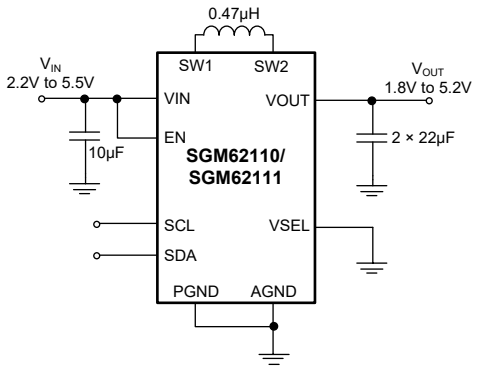


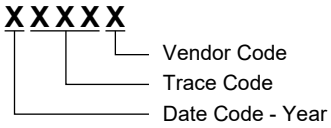

**Figure 1. Typical Application Circuit**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM62110 | WLCSP-2.21×1.40-15B | -40℃ to +85℃ | SGM62110YG/TR | 62110<br>XXXXX | Tape and Reel, 3000 |
| SGM62111 | WLCSP-2.21×1.40-15B | -40℃ to +85℃ | SGM62111YG/TR | 62111<br>XXXXX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Input Voltage (VIN, SW1, SW2, VOUT, SCL, SDA, EN, VSEL) ..... -0.3V to 6V
Input Voltage for Less than 10ns (SW1, SW2) ..... -3V to 9V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.2V to 5.5V
Low Range Output Voltage ..... 1.8V to 4.975V
High Range Output Voltage ..... 2.025V to 5.2V
High-Level Input Voltage ..... 1.3V to $V_{IN}$
Low-Level Input Voltage ..... 0V to 0.3V
EN Voltage ..... 0V to $V_{IN}$
Output Current (1)
$V_{OUT}$ = 3.3V, $V_{IN}$ ≥ 2.5V ..... 2.5A
$V_{OUT}$ = 3.5V, $V_{IN}$ ≥ 2.5V ..... 2A
$V_{OUT}$ = 3.5V, $V_{IN}$ ≥ 2.8V ..... 2.5A
Capacitance at $V_{IN}$ = 2.5V to 5V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 2.5A
Input Capacitance (2) ..... 5μF (MIN)
Output Capacitance (2) ..... 16μF (13μF, MIN)
Inductance ..... 390nH to 560nH (470nH TYP)
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:
(1) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.

(2) Effective capacitance after DC bias effects have been considered.

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

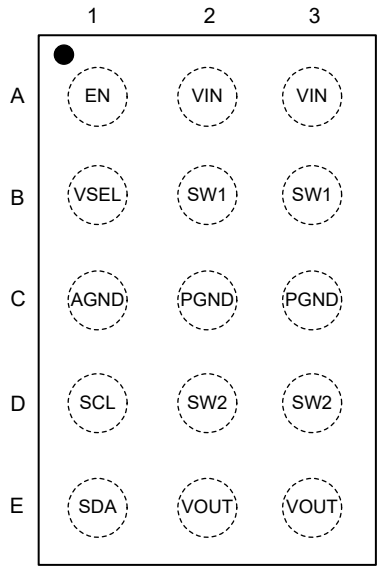
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




WLCSP-2.21×1.40-15B

## PIN DESCRIPTION

| PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| A1 | EN | I | Active High Logic, Device Enable Input. |
| A2, A3 | VIN | P | Input Power Supply. |
| B1 | VSEL | I | VOUT Register Select Pin. VOUT1 register is selected by VSEL = low and VOUT2 register is selected by VSEL = high to set the output voltage. |
| B2, B3 | SW1 | P | Buck Leg Connection for Inductor. |
| C1 | AGND | G | Analog Ground. Connect it to the GND pins under the chip. |
| C2, C3 | PGND | G | Power Ground. |
| D1 | SCL | I/O | $I^2C$ Bus Clock Signal. Pull up with a resistor or current source to the $I^2C$ bus voltage. |
| D2, D3 | SW2 | P | Boost Leg Connection for Inductor. |
| E1 | SDA | I/O | $I^2C$ Bus Data Signal. Pull up with a resistor or current source to the $I^2C$ bus voltage. |
| E2, E3 | VOUT | O | Converter Output. |

NOTE: I: input, I/O: input or output.

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V and $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| Supply Current into VIN | $I_Q$ | $V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V, $V_{EN}$ = 3.6V, not switching, $T_J$ = +25℃ | | 15 | | μA |
| Shutdown Current into VIN | $I_{SD}$ | $V_{IN}$ = 3.6V, $V_{OUT}$ = 0V, $V_{EN}$ = 0V, $T_J$ = +25℃ | | 0.35 | | μA |
| UVLO Rising Threshold Voltage | $V_{IT+}$ | | | 2.10 | | V |
| UVLO Falling Threshold Voltage | $V_{IT-}$ | | | 1.90 | | V |
| UVLO Hysteresis Voltage | $V_{HYS}$ | | | 200 | | mV |
| **I/O Signals** | | | | | | |
| Logic Voltage Rising Threshold | $V_{IH}$ | | 1.2 | | | V |
| Logic Voltage Falling Threshold | $V_{IL}$ | | | | 0.4 | V |
| High-Level Input Current | $I_{IH}$ | For SCL, SDA, VSEL, $V_{SCL}$ = $V_{SDA}$ = $V_{VSEL}$ = 1.8V, no pull-up resistor | | ±0.01 | | μA |
| Low-Level Input Current | $I_{IL}$ | For SCL, SDA, VSEL, $V_{SCL}$ = $V_{SDA}$ = $V_{VSEL}$ = 0V, no pull-up resistor | | ±0.01 | | μA |
| Input Bias Current | $I_{IB}$ | For EN, $V_{EN}$ = 0V to 5.5V | | ±0.01 | | μA |
| **Power Stage** | | | | | | |
| Output Voltage Range | $V_{OUT}$ | RANGE = 0 | 1.8 | | 4.975 | V |
| | | RANGE = 1 | 2.025 | | 5.2 | |
| Output Voltage Accuracy | | PWM operation | -1.5 | | 1.5 | % |
| | | PSM operation | -1.5 | | 3.5 | % |
| Default Output Voltage | $V_{OUT}$ | VSEL = low (RANGE = 0) | | 3.30 | | V |
| | | VSEL = high (RANGE = 0) | | 3.45 | | |
| Switch Current Limit | $I_{LIM}$ | $V_{IN}$ = 2.5V, $V_{OUT}$ = 3.3V, boost operation, output sourcing current | | 6 | | A |
| | | $V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V, buck operation, output sourcing current | | 6 | | |
| | | $V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V, reverse-boost operation, output sinking current | | 1 | | |
| PSM Entry Threshold (Peak) Current | $I_{T-\_PSM}$ | $V_{IN}$ = 4.2V, $V_{OUT}$ = 3.3V | | 0.85 | | A |
| Output Discharge Current | $I_{DIS}$ | $V_{OUT}$ = 3.5V | 50 | | | mA |
| Output Voltage Rising Power-Good Threshold | $V_{T+}$ | | | 95 | | % |
| Output Voltage Falling Power-Good Threshold | $V_{T-}$ | | | 90 | | % |
| VIN Rising Over-Voltage Threshold | | | | 5.7 | | V |
| **I²C Interface** | | | | | | |
| 7-Bit Slave Address | | | | 75 | | h |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold | $T_{SD}$ | $T_J$ rising | | 150 | | ℃ |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 20 | | ℃ |

## TIMING REQUIREMENTS

(Over operating junction temperature range and recommended supply voltage range, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCL Clock Frequency | $f_{SCL}$ | Standard mode | 0 | | 100 | kHz |
| | | Fast mode | 0 | | 400 | |
| | | Fast mode plus | 0 | | 1000 | |
| SCL Clock LOW Period | $t_{LOW}$ | Standard mode | 4.7 | | | μs |
| | | Fast mode | 1.3 | | | |
| | | Fast mode plus | 0.5 | | | |
| SCL Clock HIGH Period | $t_{HIGH}$ | Standard mode | 4.0 | | | μs |
| | | Fast mode | 0.6 | | | |
| | | Fast mode plus | 0.26 | | | |
| Bus Free Time between a STOP and a START Condition | $t_{BUF}$ | Standard mode | 4.7 | | | μs |
| | | Fast mode | 1.3 | | | |
| | | Fast mode plus | 0.5 | | | |
| Set-up Time for a Repeated START Condition | $t_{SU,STA}$ | Standard mode | 4.7 | | | μs |
| | | Fast mode | 0.6 | | | |
| | | Fast mode plus | 0.26 | | | |
| Hold Time (Repeated) START Condition | $t_{HD,STA}$ | Standard mode | 4.0 | | | μs |
| | | Fast mode | 0.6 | | | |
| | | Fast mode plus | 0.26 | | | |
| Data Set-Up Time | $t_{SU,DAT}$ | Standard mode | 250 | | | ns |
| | | Fast mode | 100 | | | |
| | | Fast mode plus | 50 | | | |
| Data Hold Time | $t_{HD,DAT}$ | Standard mode | 0 | | | μs |
| | | Fast mode | 0 | | | |
| | | Fast mode plus | 0 | | | |
| Rise Time of SDA and SCL Signals | $t_R$ | Standard mode | | | 1000 | ns |
| | | Fast mode | 20 | | 300 | |
| | | Fast mode plus | | | 120 | |
| Fall Time of SDA and SCL Signals | $t_F$ | Standard mode | | | 300 | ns |
| | | Fast mode | $20 \times V_{DD}/5.5$ | | 300 | |
| | | Fast mode plus | $20 \times V_{DD}/5.5$ | | 120 | |
| Set-up Time for STOP Condition | $t_{SU,STO}$ | Standard mode | 4.0 | | | μs |
| | | Fast mode | 0.6 | | | |
| | | Fast mode plus | 0.26 | | | |
| Data Valid Time | $t_{VD,DAT}$ | Standard mode | | | 3.45 | μs |
| | | Fast mode | | | 0.9 | |
| | | Fast mode plus | | | 0.45 | |
| Data Valid Acknowledge Time | $t_{VD,ACK}$ | Standard mode | | | 3.45 | μs |
| | | Fast mode | | | 0.9 | |
| | | Fast mode plus | | | 0.45 | |
| Capacitive Load on Each Bus Line | $C_B$ | Standard mode | | | 400 | pF |
| | | Fast mode | | | 400 | |
| | | Fast mode plus | | | 550 | |
| VSEL Pulse Duration | $t_{w\_VSEL}$ | VSEL = high or low | 5 | | | μs |

## SWITCHING CHARACTERISTICS

($V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V and $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| EN Rising Edge to Output Ramp Start Delay | $t_{D\_EN}$ | $T_J$ = +25℃, $V_{IN}$ = 3.6V | | 229 | | μs |
| Power-Good Delay | $t_{D\_PG}$ | $V_{OUT}$ falling | | 50 | | μs |
| Slew Rate of Internal Ramp during Dynamic Voltage Scaling | SR | SLEW[1:0] = 00, forced-PWM operation | | ±1 | | V/ms |
| | | SLEW[1:0] = 01, forced-PWM operation | | ±2.5 | | |
| | | SLEW[1:0] = 10, forced-PWM operation | | ±5 | | |
| | | SLEW[1:0] = 11, forced-PWM operation | | ±10 | | |
| Switching Frequency | $f_{SW}$ | PWM operation, $I_{OUT}$ = 100mA | | 3 | | MHz |
| VSEL Rising Edge to DVS Ramp Start Delay | $t_{D\_VSEL}$ | Measured from rising edge of VSEL to the start of the ramp in Dynamic Voltage Scaling | | | 5 | μs |

## FUNCTIONAL BLOCK DIAGRAM

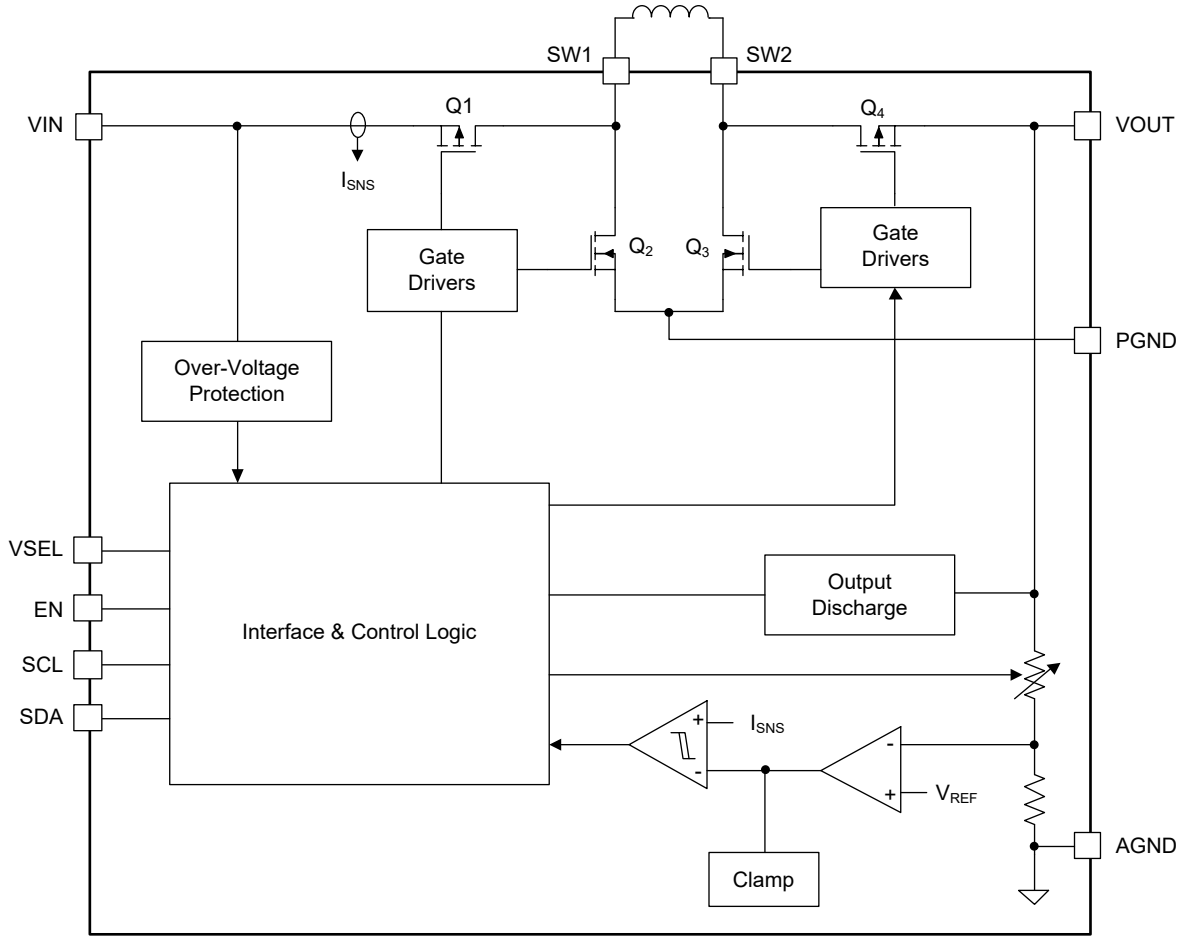



**Figure 2. Block Diagram**

# DETAILED DESCRIPTION

## Overview

The SGM62110 and SGM62111 are synchronous buck-boost converters with integrated switches that can operate over a wide input voltage and output current range with high efficiency. It is capable to change its mode automatically among buck, boost and buck-boost depending on the input condition. Buck mode when $V_{IN}$ > $V_{OUT}$, boost mode when $V_{IN}$ < $V_{OUT}$, and 4-cycle buck-boost mode when $V_{IN}$ ≈ $V_{OUT}$. In the buck-boost mode, the 4-cycle operation controls the 4-switches to turn on/off alternately to reduce the RMS current in the inductor and output capacitors to maintain low output voltage ripple and achieving high efficiency across entire input voltage range.

## Mode Toggle

The SGM62110 and SGM62111 automatically select the operation mode based on the input and output voltages as shown in Figure 3. Hysteresis is added in the $V_{IN}$ ≈ $V_{OUT}$ region to ensure stable operation.

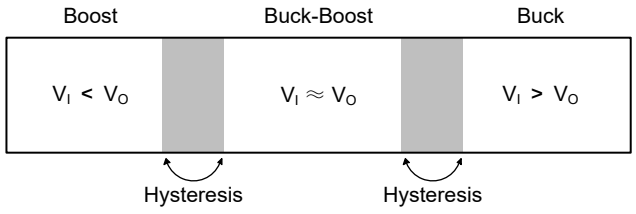



**Figure 3. Switching Scheme Selection**

### Buck Mode

When $V_{IN}$ > $V_{OUT}$, the device operates as a buck converter as shown in Figure 4. $Q_1$ is the control switch, $Q_2$ is the synchronous rectifier, $Q_3$ is off and $Q_4$ is always on. In buck mode, each switching cycle has two phases (switch on and off). Note that $Q_1$ and $Q_4$ are P-channel MOSFETs, which eliminates the need for external boot-strap capacitors.

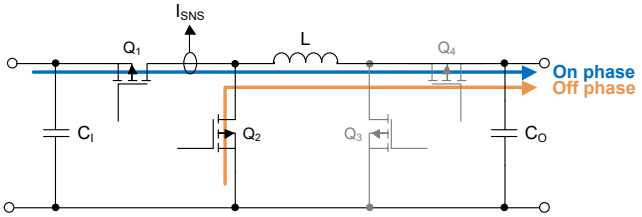



**Figure 4. Buck Mode Switching**

### Boost Mode

If $V_{IN}$ < $V_{OUT}$, the device operates as a boost converter (see Figure 5). In the boost mode, $Q_1$ is always on, $Q_2$ is off, $Q_3$ is the control switch, and $Q_4$ acts as the synchronous rectifier. Each cycle has two phases (Switch on and off).

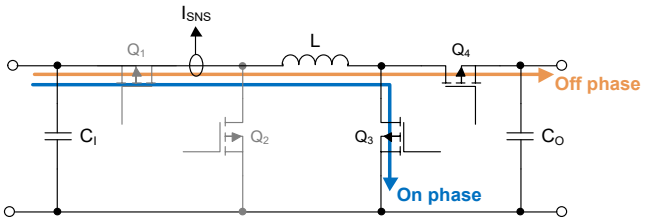



**Figure 5. Boost Mode Switching**

### Buck-Boost Mode

When $V_{IN}$ is close to or equal to $V_{OUT}$, all four switches are controlled in a continuously on manner (Figure 6). Each switching cycle has four phases: on phase ($Q_1$, $Q_3$ on), commutate phase ($Q_1$, $Q_4$ on), off phase ($Q_2$, $Q_4$ on) and commutate phase ($Q_1$, $Q_4$ on).

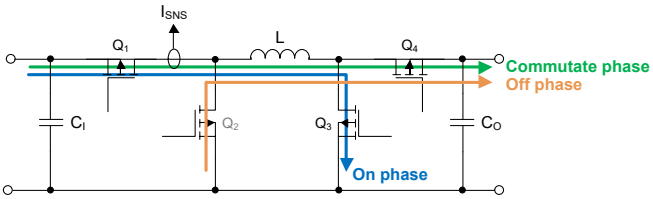



**Figure 6. Buck-Boost Switch Configuration**

## Control Scheme

The SGM62110 and SGM62111 employ peak current mode. The output voltage loop's error amplifier output sets the desired current loop threshold for PWM duty cycle control. When the sensed peak inductor current ($I_{LM}$) reaches the reference, the on-phase is terminated and the next phase(s) of the switching cycle will start.

The off time is a function of $V_{IN}$ and $V_{OUT}$ and converter operating mode (buck, boost or buck-boost).

## DETAILED DESCRIPTION (continued)

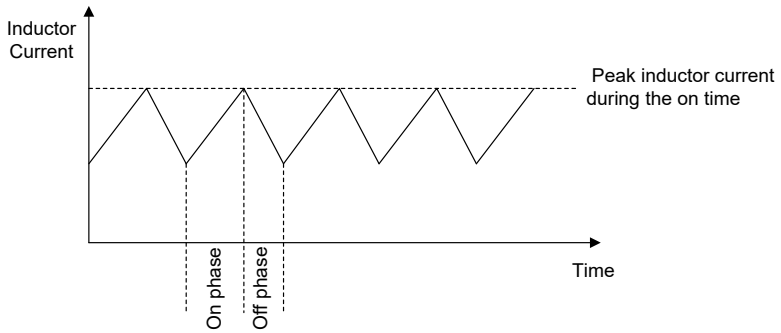



**Figure 7. Buck or Boost Modes Peak Current Control**

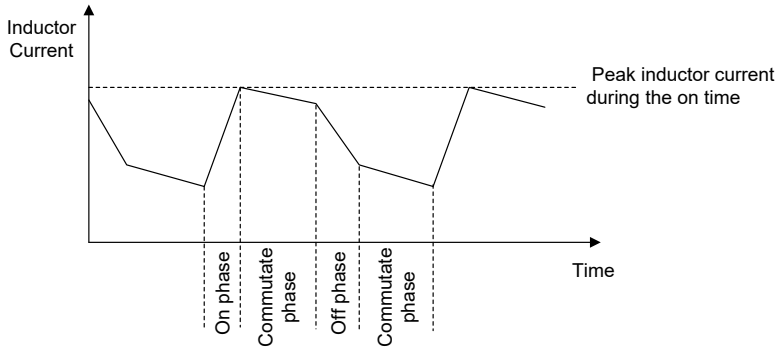



**Figure 8. Buck-Boost Mode Peak Current Control ($V_{IN}$ < $V_{OUT}$)**

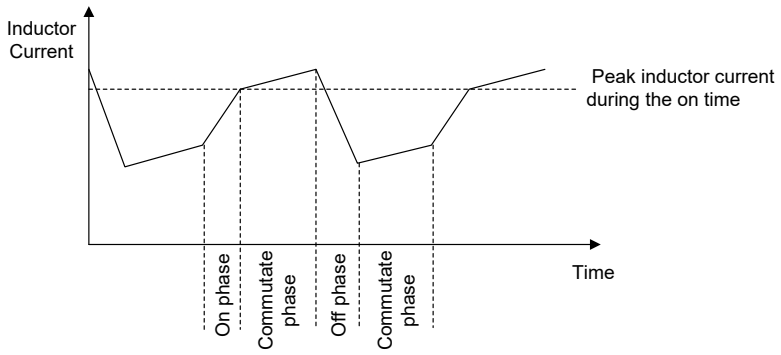



**Figure 9. Buck-Boost Mode Peak Current Control ($V_{IN}$ > $V_{OUT}$)**

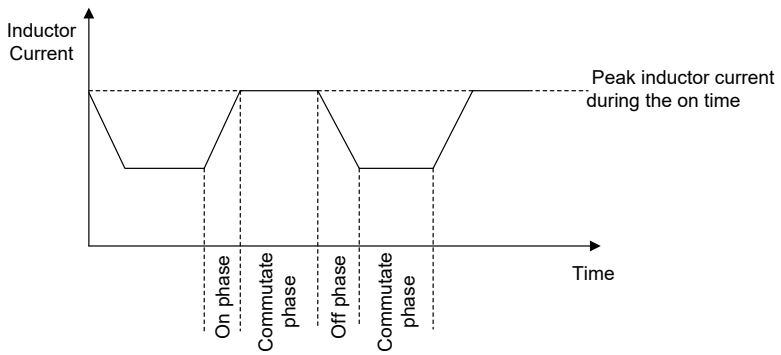



**Figure 10. Buck-Boost Mode Peak Current Control ($V_{IN}$ = $V_{OUT}$)**

## DETAILED DESCRIPTION (continued)

When the Forced PWM (FPWM) mode is configured in the Control register, the SGM62110 and SGM62111 remain in continuous conduction mode even if the inductor current is negative, which causes current to flow in the reversed direction. During the negative current phase, the voltage loop's error amplifier will provide a negative peak current threshold for the inner current loop which causes the inductor's average current in reversed direction to become more negative. Thus, smaller current limit levels must be used for the reverse current (Figure 11 and Figure 12).

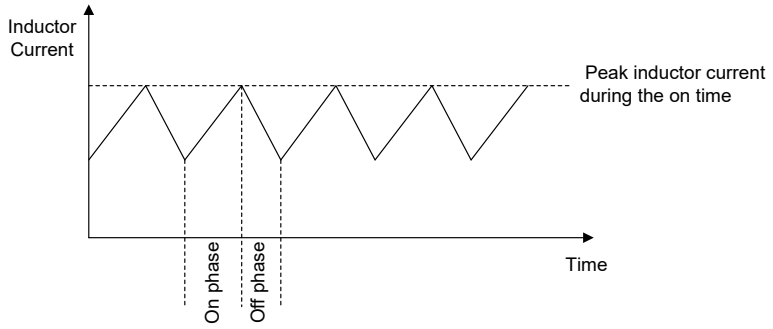



**Figure 11. Buck or Boost Mode Reverse Peak Current Control**

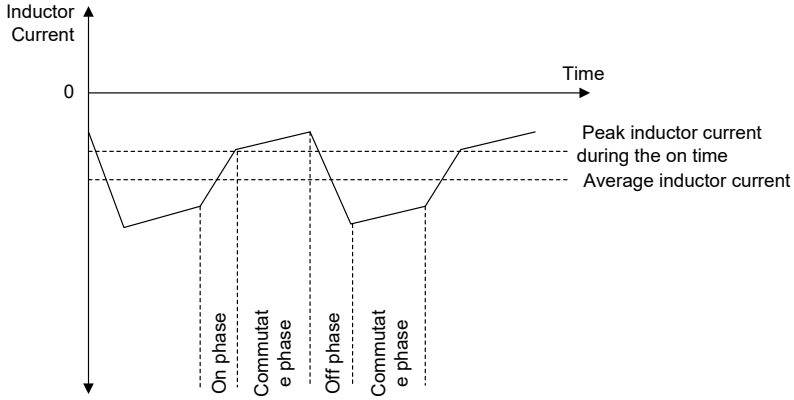



**Figure 12. Buck-Boost Mode Reverse Peak Current Control (with $V_{IN}$ > $V_{OUT}$)**

### Power-Save Mode (PSM)

To enable power-save mode, clear the FPWM bit in the control register (reset to 0).

In PFM mode, in medium to heavy load, SGM62110 and SGM62111 operate in FPWM mode. To improve the efficiency at light load, the device switches to the pulse-frequency modulation (PFM) mode. In the PFM mode, a sequence of burst switching cycles occurs to maintain the output voltage followed by an off period (Figure 13). A built-in comparator looks at the error amplifier's (EA) output voltage and pre-defined PFM threshold voltage. When the EA output is higher than the burst threshold voltage, the device starts burst sequence, and vice versa. The device automatically adjusts the switching frequency and burst sequence duration to ensure the output voltage is in regulation.

In PFM mode, switching loss is reduced due to the reduced switching cycles. Some of the internal blocks are turned off in PFM mode to further improve the light load efficiency, however, output voltage ripple, DC output voltage accuracy and load transient performance are reduced in PFM mode (see Table 1).

## DETAILED DESCRIPTION (continued)

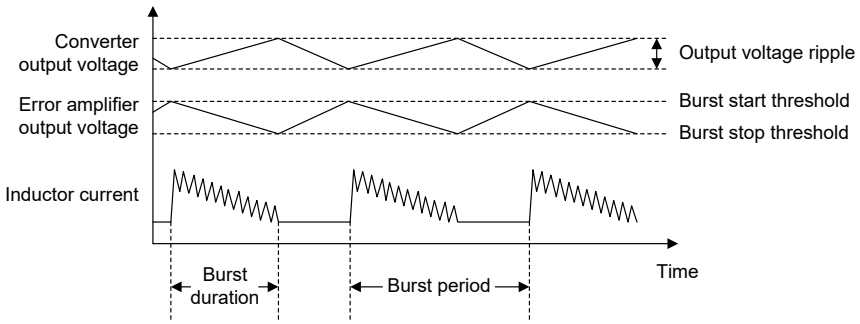



**Figure 13. Pulse-Frequency Modulation (PFM)**

**Table 1. Comparison of the Forced-PWM and Power-Save Mode Performances**

| Performance Parameter | Best Operating Mode |
|---|---|
| Low-Power Efficiency | Power-Save Mode |
| DC Output Voltage Accuracy | Forced-PWM |
| Transient Response | Forced-PWM |
| Output Voltage Ripple | Forced-PWM |

### Forced-PWM (FPWM)

In the forced PWM mode, at light load condition, the synchronous switches are not turned off when the inductor current goes negative to maintain a constant switching frequency. FPWM operation has lower output voltage ripple and better transient response compared to PFM. However, in the lower output currents, FPWM results in higher switching and conduction loss thus lower efficiency.

The FPWM bit in the control register should be set to 1 to enable the forced-PWM operation. During start-up, the device will force to operate in FPWM until power-good status is reached for the first time.

### Ramp-PWM

RPWM bit sets the Ramp-PWM operation, which also configures the device in FPWM operation when ramping from one output voltage to another during dynamic voltage scaling. In light load condition and PFM mode is configured, when ramping from a higher voltage to a lower voltage, load cannot sink enough current to discharge the output capacitor. It is recommended to enable RPWM bit to control the output voltage ramp down in a controlled manner (see Figure 14).

Set the RAMP bit in the Control register to enable ramp-PWM operation.

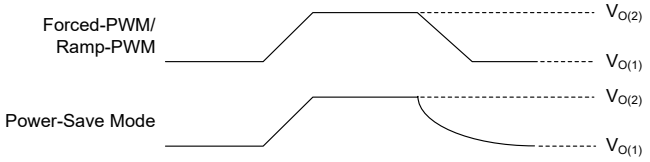



**Figure 14. Ramp-PWM Operation**

### Device Enable (EN)

Use the EN pin to enable or disable the device (EN = high to enable).

### Under-Voltage Lockout (UVLO)

The under-voltage lockout feature disables the device when the input supply voltage is too low to prevent device malfunction.

### Soft-Start

A built-in internal soft-start function will minimize the inrush current and limit the output voltage overshoot during start-up. When the device is turned on or enabled, the switch current limit is increased gradually to the maximum to prevent large input currents at start-up. With the gradual increase of the current limit, the inrush current for no-load conditions is minimized while it is still possible to start heavy loads (as long as the load does not exceed the device current limit).

The output voltage rise time depends on the application and operating conditions. $V_{OUT}$ rise time will increase if the output capacitance and load are large or if the device operates in boost mode. More information can be found in the Application Information section.

## DETAILED DESCRIPTION (continued)

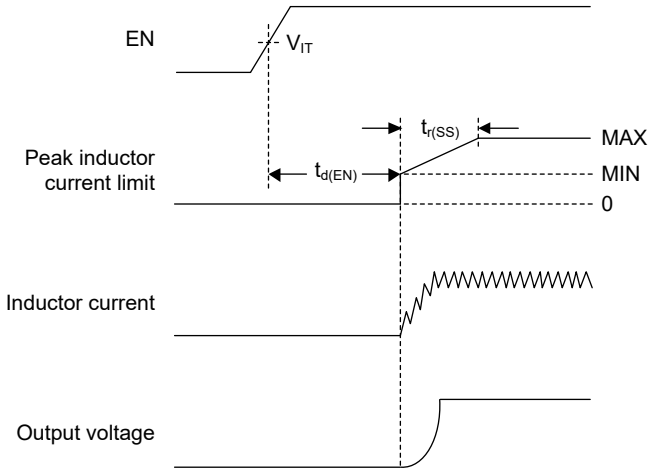



**Figure 15. Start-up Performance**

### Output Voltage Control

The SGM62110 and SGM62111 output voltages can be programmed between 1.8V to 5.2V with a resolution of 25mV.

The RANGE bit in the Control register is used to select the output voltage range.

When RANGE = 0, the output voltage is programmed from 1.8V to 4.975V. When RANGE = 1, the output voltage is programmed from 2.025V to 5.2V.

The VSEL pin selects which VOUT register is used to set the output voltage. The 7-bit value of the selected VOUT[6:0] register determines the output value as follows:

When RANGE = 0, $V_{OUT}$ = (VOUT[6:0] × 0.025) + 1.8V. When RANGE = 1, $V_{OUT}$ = (VOUT[6:0] × 0.025) + 2.025V

If VSEL = low, the VOUT1 registers sets the output voltage. If VSEL = high, the VOUT2 register sets the output voltage.

#### Dynamic Voltage Scaling

Dynamic voltage scaling (DVS) allows changing of the output voltage with a controlled rate. Figure 16 explains the DVS function. The ramp control block changes the output voltage toward the target value in 25mV steps. The 2-bit SLEW parameter in the Control register is used to choose one of the four slew rates values of 1, 2, 5 and 10V/ms.

A DVS ramp is started when the VSEL logic level is changed or a new value is written in the active VOUT register. Note that if these changes occur during the start-up (before the end the soft-start and achieving the first power-good), the new value will take effect immediately and $V_{OUT}$ will change to the final value without gradual ramp.

DVS timing initiated by a VSEL logic change is shown in Figure 17. Figure 18 shows the same timing when an I²C write is used to change the output voltage in the active VOUT register (VOUT1 in this example).

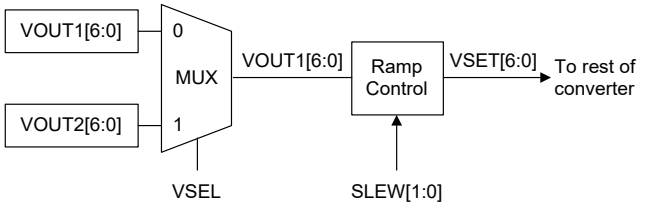
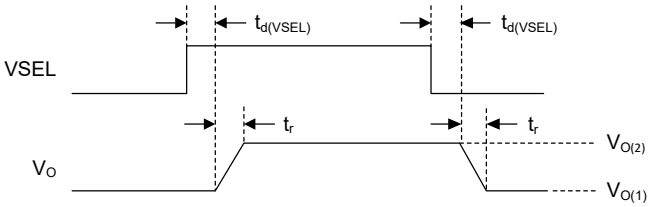


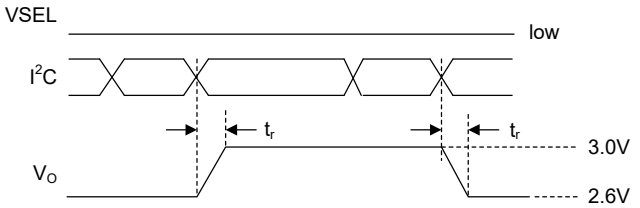

**Figure 16. Block Diagram of the Dynamic Voltage Scaling**




$$t_r = t_f = \frac{|V_{O(1)} - V_{O(2)}|}{SR}$$

Where:
$V_{O(1)}$ is the output voltage set by the VOUT1 register;
$V_{O(2)}$ is the output voltage set by the VOUT2 register;
SR is the slew rate set by the SLEW bits in the Control register.

**Figure 17. DVS Timing Diagram Initiated by a VSEL Change**




$$t_r = t_f = \frac{|3.0 - 2.6|}{SR}$$

Where:
SR is the slew rate set by the SLEW bits in the Control register.

**Figure 18. DVS Timing Initiated by a Write to the $V_{OUT}$ Register by I²C**

# DETAILED DESCRIPTION (continued)

## Protection Functions

### Input Voltage Protection (IVP)

When the output ramps down to a lower voltage by DVS, the current can flow from the output of the device back to the input, especially in light load condition. While the load does not sink enough current to discharge the output capacitors, the only path for the current released by the output capacitors will flow back to the input. This behavior can charge the input capacitor's voltage and cause the VIN voltage to rise in an uncontrolled manner. If the converter is operating in buck mode, a rapid VOUT change to a lower voltage in FPWM mode, the reverses current flow causes the converter to act as a boost from output to the input, temporarily.

The SGM62110 and SGM62111 provide IVP feature to ensure the voltage present on VIN pin never exceed higher than 5.7V during any conditions. Switching is immediately terminated when IVP is triggered and automatically resume switching when condition is removed.

The PG bit in the Status register is set to 1 when input over-voltage is triggered. This bit is cleared if the Status register is read and the not-good condition is ended.

### Current Limiting and Over-Current Protection

The SGM62110 and SGM62111 use a clamp circuit to limit the peak inductor current if the device is overloaded. The output current limit value depends on the operating conditions ($V_{IN}$ and $V_{OUT}$) and the operating mode (buck, buck-boost or boost) – see Figure 3 to Figure 6. Usually an overload results in higher power dissipation and increased junction temperature ($T_J$) in the device that can cause device shutdown triggered by the over- temperature protection.

### Thermal Shutdown

If the junction temperature exceeds the +150 ℃ threshold, the converter will turn off (OTP) to protect the device. The device will automatically resume operation when $T_J$ falls below +130℃. Note that the automatic recovery can result in a cyclic turn on and turn off if a permanent overload condition caused the OTP, because after each shutdown, the device is cooled down and restarts operating. The $I^2C$ interface is functional even when the device is shut down due to OTP. When an over-temperature is detected, the TSD bit in the Status register is set to 1. This bit will be cleared if it is read by $I^2C$ when $T_J$ is less than +130℃.

## Power-Good

The power-good indicates that the device output voltage is in regulation and $V_{OUT}$ > 95% of the nominal value. The device is in power-not-good condition if $V_{OUT}$ < 90% of the nominal value.

Upon detection of a power-not-good condition, the PG bit in the Status register is set to 1. It is cleared if it is read by the host during a power-good condition.

## Load Disconnect in Shutdown

Input and output are disconnected when the device is shutdown that blocks any current flow between the input and output of the device.

## Output Discharge

When a logic low is applied to the EN pin or ENABLE bit is set to 0, the VOUT will be pulled to ground actively to discharge the output. This feature is beneficial for systems requiring strict power-down sequence.

## Device Functional Modes (UVLO)

Two functional modes (on and off) are defined for the device. If the $V_{IN}$ voltage is above the UVLO threshold and EN pin is pulled high, the device is in on mode. The device will enter the off mode if a UVLO occurs or if EN is pulled low.

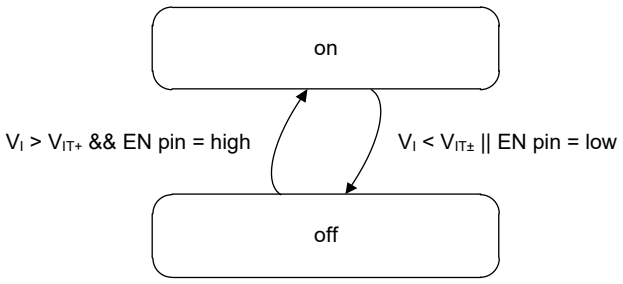



**Figure 19. ON and OFF Functional Modes**

## DETAILED DESCRIPTION (continued)

### I²C Serial Interface and Programming

I2C™ is a widely used 2-wire, bi-directional serial communication interface. It is used for the SGM62110 and SGM62111 support I²C communication for parameter programming, receiving and reporting device status. The use of I²C significantly improves the design flexibility because most of the device functions can be programmed and adapted to the application requirements.

The I²C bus uses two open-drain lines called serial data (SDA) and a serial clock (SCL) for communication. The SDA and SCL pins must be pulled up to the bus high voltage by a current source or pull-up resistors. All devices connected to the bus have their own addresses (7-bit) and each may act as a master or slave during a data transfer. The master is usually a processor or another host device that initiates a data transfer and generates the clock signals to allow transmission of the data bit. Any device that is addressed in a transfer sequence is considered as a slave. For more details about I²C refer to the “UM10204: I²C-bus specification and user manual, revision 6”.

The SGM62110 and SGM62111 are slave devices with 75h (1110101b) address and only support 7-bit addressing. The 10-bit addressing, or the general call address are not supported. The devices support standard-mode (100kbps), fast-mode (400kbps) and fast-mode plus (1Mbps) data transfer speeds. The devices have five 8-bit registers with individual internal addresses that can be read or written (except the read-only bits) by a host. See the Register Map section for details. Register contents remain intact if $V_{IN}$ voltage remains above 2.1V. The data transfer protocol for the standard and fast speed modes are the same.

#### START and STOP Conditions (For All Modes)

In the idle state condition, both SDA and SCL line are high. A transaction is initiated by a master who takes the control of the bus when it is free (idle) by sending a START or S condition to initiate the exchange of data as shown in Figure 20. When the data transfer job is done the master sends one (or more) STOP or P conditions to terminate the transaction and releases the bus. To ensure that the bus is properly reset after bus power up, it is recommended to initiate the bus by sending a STOP condition after power up.

A START condition is generated by pulling SDA from high to low when SCL is high. START is detected by all devices on the bus. Similarly, a STOP is applied on the bus by pulling SDA from low to high when SCL is high. The START and STOP conditions are always generated by a master. After a START and before a STOP the bus is considered busy. The master may not release the bus after a complete transaction with the slave and send a repeated START (Sr) to initiate a new data exchange with the slave.

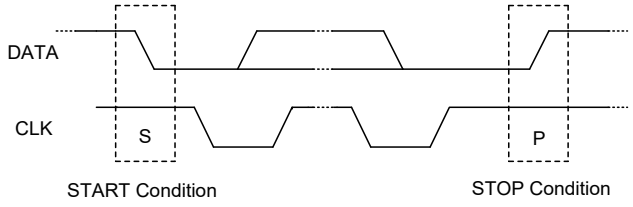



**Figure 20. START and STOP Conditions**

#### Data Bit Transmission and Validity

During a transaction all data bit (high or low) must remain stable on the SDA line during SCL = H period. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by the master. Bit transferring procedure is shown in Figure 21.

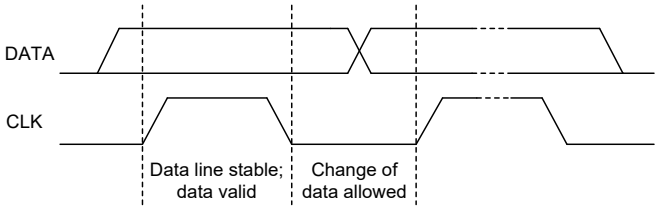



**Figure 21. Bit Transfer on the Serial Interface**

## DETAILED DESCRIPTION (continued)

### I²C Data Format

The data is transmitted one byte at a time. After detecting the START condition, the transmitter will send one byte (8-bit) of data, bit by bit starting from the most significant bit (MSB). With each SCL pulse a new bit is placed on the SDA line. After sending the 8th bit, the transmitter releases the SDA line during the 9th SCL pulse in order to receive an acknowledgement bit from the receiver. Therefore, a total of 9 bits is exchanged for each byte. The number of bytes in one transaction is not limited. After sending the ACK bit, if the receiver is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the sender in wait state (clock stretching). When it is ready for another byte of data, it releases the clock line and the data transfer can continue with clocks generated by the master.

The 9th bit is the receiver response (slave or master) to show that the byte is received. Sending a low during the 9th clock cycle is interpreted as ACK. If the receiver responds a high or does not respond at all, the sender will receive a high for the 9th bit that is considered as not ACK (= NCK). An NCK means that the receiver is not expecting more data. Therefore, the response of the receiver to the last byte in a transaction is a NCK. It can also show that there is a problem in the communication link (rare). After the 9th bit a STOP or a repeated START (Sr) should be sent by master. Figure 22 and Figure 23 show the byte transfer and acknowledgment procedures of the I²C interface.

### I²C Data Communication Protocol

After power up it is recommended to send a STOP condition by the host to assure all I²C slaves are reset and ready. All connected I²C devices recognize the STOP condition and know when the bus is idle to monitor the bus for START condition followed by an address. To communicate with an specific device, after the host or master sends a START condition it generates the SCL (clock) pulses and transmits the 7-bit address of the destination device along with an 8th (R/W) data-direction bit as one byte. All devices compare the address to their own fixed address. The SDA line is released after the 8th bit for the target receiver to reply with an ACK (by pulling the SDA line low during the high period of the 9th clock). By receiving the ACK, the master realizes that the slave is ready and the link is OK.

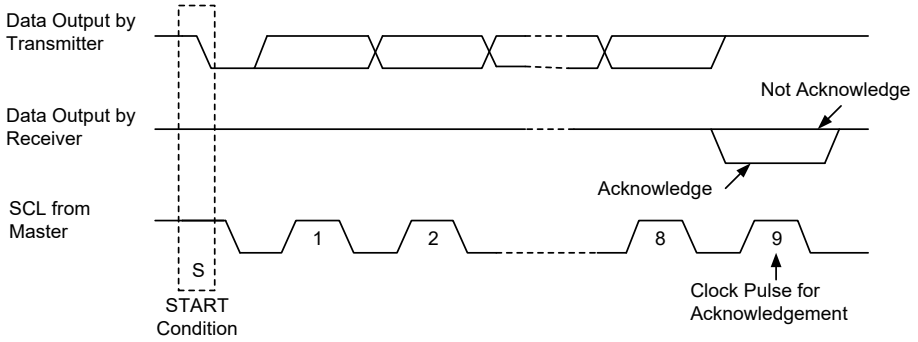



**Figure 22. Acknowledgement on the I²C Bus**

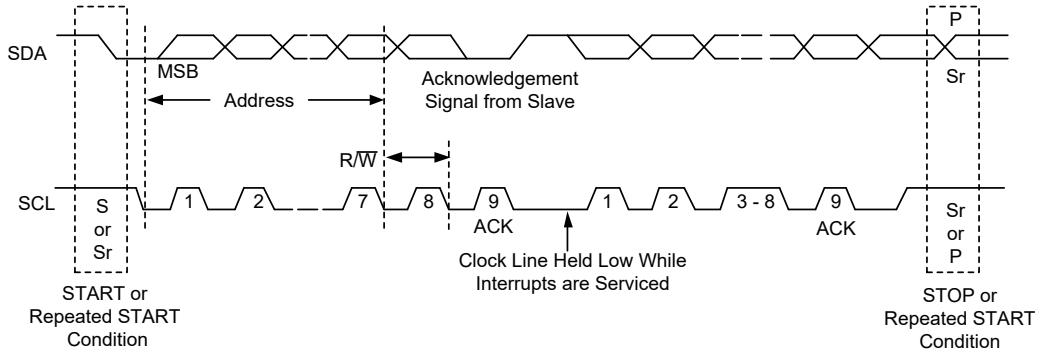



**Figure 23. I²C Data Communication Protocol**

# DETAILED DESCRIPTION (continued)

## Register Read and Write

After sending a START condition, the master sends the slave address along with an 8th bit (R/W) to inform the slave if the following byte of data is supposed to be a received by slave (Write) or the slave should send a byte of data back to master (Read). After receiving the ACK from the addressed slave, the master continues to send more clock pulses for future read or write.

The second byte is a write containing the register address that the master wants to access in the slave.

If the sequence is a single write and the master wants to write in the addressed register in the slave, the third byte will be the content of the addressed register (a write). Ignoring the slaves reply (ACK or NCK), the master issues a STOP and the transaction is ended. The format of a single write to a device register is shown in the Figure 24.

If the sequence is a single read, and the master wants to read the content of the addressed register in the slave, the master first sends a new START (repeated START) before the third byte because the direction of read/write needs to be changed from write to read. So, the third byte is still the slave address and the 8th bit will be R/W = 1. The slave will send an ACK bit followed by the content of the register as the fourth byte. Master may reply with an ACK or NCK and then issues a STOP condition. The format of a single read from a device register is shown in the Figure 25. Reading data from a register address that is not listed will be 00h.

The device register contents are updated on the falling edge of the acknowledge signal after the last byte.

The transmission of 9-bit valid data sequences (8-bit data and 1-bit acknowledge) can continue as long as needed.

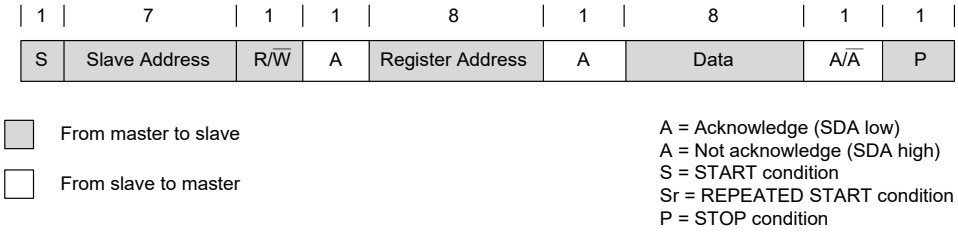



**Figure 24. The Format of a "Write" into a Device Register in the Standard, Fast and Fast-Plus Modes**

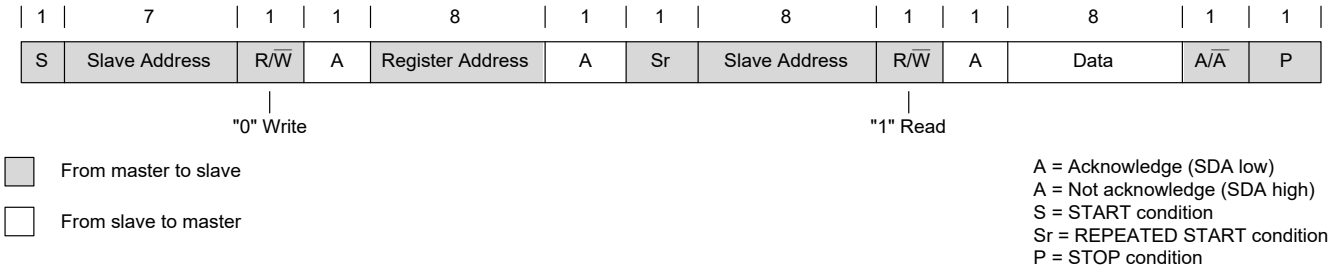



**Figure 25. The Format of a "Read" from a Device Register in the Standard, Fast and Fast-Plus Modes**

# REGISTER MAP

Table 2 lists the map of the SGM62110 and SGM62111 registers. Any register address not listed in Table 2 should be considered as a reserved location and no write should be tried to modify them (They may be used in future revisions).

**Table 2. Device Registers**

| ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 01h | CONTROL | Control Register |
| 02h | STATUS | Status Register |
| 03h | DEVID | Device Identity Register |
| 04h | VOUT1 | VOUT1 Register |
| 05h | VOUT2 | VOUT2 Register |

## Control Register (Address = 01h) [reset value = 20h for SGM62110 and 00h for SGM62111]

Control register is used to configure the device operation. The bit details are shown in Table 3. It is a read/write register, but no write is allowed to the reserved bits. CONTROL is a volatile register and loses its contents if $V_{IN}$ falls below UVLO threshold or the device is disabled by applying a low to the EN pin.

**Table 3. Control Register Details**

| BITS | BIT NAME | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| D[7] | RESERVED | R | 0 | Reserved |
| D[6] | RANGE | R/W | 0 | This bit selects the output voltage range.<br>0: Low range (1.800V to 4.975V) (default)<br>1: High range (2.025V to 5.200V) |
| D[5] | ENABLE | R/W | x | This bit controls operation of the converter.<br>0: Converter operation disabled (Start-up value for SGM62111)<br>1: Converter operation enabled (Start-up value for SGM62110) |
| D[4] | RESERVED | R/W | 0 | Reserved for future use.<br>This bit can be written to and read from but it has no function. For compatibility with possible future device variants, it is recommended to program this bit to 0. |
| D[3] | FPWM | R/W | 0 | Set forced-PWM operation.<br>0 = Disable forced-PWM (default)<br>1 = Enable forced-PWM |
| D[2] | RPWM | R/W | 0 | Set ramp-PWM operation.<br>0 = Disable ramp-PWM (default)<br>1 = Enable ramp-PWM |
| D[1:0] | SLEW[1:0] | R/W | 00 | Set the slew rate of the output voltage change to a new value.<br>00 = 1V/ms (default)<br>01 = 2.5V/ms<br>10 = 5V/ms<br>11 = 10V/ms |

## Status Register (Address = 02h) [reset value = 00h]

Status register bit details are shown in Table 4. This is a read only register containing the device status information. A read operation clears all bits of this register (unless a status is still valid during the read and sets the bit again). It is a volatile register and loses its value if the $V_{IN}$ falls below UVLO or by applying a low to the EN pin (disable).

## REGISTER MAP (continued)

**Table 4. Status Register Details**

| BITS | BIT NAME | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| D[7:4] | RESERVED | R | 000 | Reserved |
| D[3] | HD | R | 0 | This bit shows the status of the hot-die function.<br>0: Normal operation (default)<br>1: A hot-die event was detected |
| D[2] | OC | R | 0 | This bit shows the status of the over-current function.<br>0: Normal operation (default)<br>1: An over-current event was detected |
| D[1] | TSD | R | 0 | Thermal Shutdown. It is cleared if this register is read and if the over-temperature condition no longer exists.<br>0 = Temperature good<br>1 = An OTP event occurred |
| D[0] | PG | R | 0 | Output Power-Good. PG is cleared with a read if the power-not-good condition no longer exists.<br>0 = Power-good<br>1 = A power-not-good event was detected |

### Device Identity Register (Address = 03h) [reset value = 40h]

DEVID register bit details are shown in Table 5. This is a read only register that holds the die revision of the device.

**Table 5. Device Identity Register Details**

| BITS | BIT NAME | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| D[7:4] | MANUFACTURER | R | 0100 | Manufacturer ID (0000 = SGMICRO). |
| D[3:2] | MAJOR[1:0] | R | 00 | Major die revision:<br>00 = A (initial silicon)<br>01 = B (first major revision)<br>10 = C (second major revision)<br>11 = D (third major revision) |
| D[1:0] | MINOR[1:0] | R | 00 | Minor die revision:<br>00 = 0 (initial silicon)<br>01 = 1 (first minor revision)<br>10 = 2 (second minor revision)<br>11 = 3 (third minor revision) |

### VOUT1 Register (Address = 04h) [reset value = 3Ch]

VOUT1 bit details are shown in Table 6. VOUT1 determines the output voltage if the VSEL pin is logic low. It is a volatile register and its value is lost if the $V_{IN}$ voltage falls below UVLO or the EN pin is pulled low.

**Table 6. VOUT1 Register Details**

| BITS | BIT NAME | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| D[7] | RESERVED | R | 0 | Reserved |
| D[6:0] | VOUT1[6:0] | R/W | 0111100 | If VSEL pin is low, these bits set the output voltage:<br>$V_{OUT}$ = 1.8 + (VOUT1[6:0] × 0.025) volts (RANGE = 0, default 3.3V)<br>$V_{OUT}$ = 2.025 + (VOUT1[6:0] × 0.025) volts (RANGE = 1, default 3.525V) |

### VOUT2 Register (Address = 05h) [reset value = 42h]

VOUT2 bit details are shown in Table 7. VOUT2 determines the device output voltage if the VSEL pin is logic high. It is a volatile register and its value is lost if the $V_{IN}$ falls below UVLO or the EN pin is pulled low.

**Table 7. VOUT2 Register Details**

| BITS | BIT NAME | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| D[7] | RESERVED | R | 0 | Reserved |
| D[6:0] | VOUT2[6:0] | R/W | 1000010 | If VSEL pin is high, these bits set the output voltage:<br>$V_{OUT}$ = 1.8 + (VOUT2[6:0] × 0.025) volts (RANGE = 0, default 3.45V)<br>$V_{OUT}$ = 2.025 + (VOUT2[6:0] × 0.025) volts (RANGE = 1, default 3.675V) |

# APPLICATION INFORMATION

The SGM62110 and SGM62111 are perfect choices for applications that demand for a power supply with high efficiency over a wide load range and their input voltage can vary from below, near and above the desired output voltage. The peak currents in the internal switches of the device are typically limited to a maximum of around 6A. Input and output voltage ranges are 2.2V to 5.5V and 1.8V to 5.2V respectively.

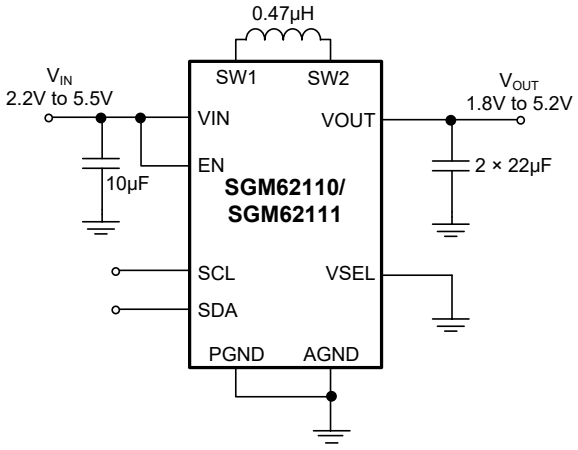



**Figure 26. Application Example of Smartphone 2A Power Supply with 1.8V to 5.2V Output**

## Design Requirements

This example uses the design parameters listed in Table 8.

**Table 8. Design Parameters**

| Design Parameter | Symbol | Example Value |
|---|---|---|
| Input Voltage | $V_{IN}$ | 2.5V to 4.8V |
| Output Voltage | $V_{OUT}$ | 1.8V to 5.2V |
| Output Current | $I_{OUT}$ | 2A |
| I²C Bus Voltage | $V_{BUS}$ | 3.3V |
| I²C Bus Capacitance | $C_B$ | 100pF |
| I²C Bus Speed | | Fast-mode (400kHz) |

## Design Procedure

### Input Capacitor

The total input capacitance after considering the DC bias de-rating is recommended to be above 5μF. A 10μF, 6.3V ceramic capacitor should fit most of the applications. If the source is far away from the device, additional bulk capacitance (such as a 47μF electrolytic or tantalum capacitor) is recommended for better stability.

### Inductor

A 0.47μH inductor is recommended for use with SGM62110 and SGM62111. Lower DCR inductors are recommended for better efficiency. The rated saturation current ($I_{sat}$) must be at least 20% above the maximum peak current in the worst cases including transients. Usually the worst cases happen in the boost mode when operating at the lowest input voltage, highest output voltage and with the maximum load. Use Equation 1 to calculate the maximum duty cycle in boost mode (corresponds to the maximum inductor current).

$$D_{MAX} = \frac{V_{OUT\_MAX} - V_{IN\_MIN}}{V_{OUT\_MAX}} \quad (1)$$

Where:

$D_{max}$ is the maximum duty cycle in boost mode.

$V_{IN,min}$ is the lowest input voltage.

$V_{OUT,max}$ is the maximum output voltage.

In this application:

$$D_{MAX} = \frac{5V - 2.5V}{5V} = 0.5V$$

the maximum inductor current can be calculated by:

$$I_{LM} = \frac{I_{OUT}}{\eta(1-D_{MAX})} + \frac{D_{MAX} \times V_{IN\_MIN}}{2fL} \quad (2)$$

Where:

$I_{LM}$ is the peak inductor current.

$I_{OUT}$ is the maximum output current.

η is the converter efficiency (use application curves or choose 90%).

$V_{IN}$ is the input voltage.

f is the switching frequency (= 3MHz).

L is the inductance (0.47μH).

Choose the $I_{sat}$ value at least 20% higher than the calculated $I_{LM}$ value. In this example, $I_{LM}$ ≈ 5.1A and the selected inductor saturation current is 6.1A.

## APPLICATION INFORMATION (continued)

### Output Capacitor

It is recommended to have at least 16μF effective output capacitance (after de-rating) for the SGM62110 and SGM62111. Using two 22μF, 6.3V ceramic capacitors should be sufficient for most applications. To reduce high frequency noise, a 100nF ceramic capacitor in 0201 or 0402 package is recommended to place as close to the VOUT and GND pins as possible in parallel to the other output capacitors.

There is no upper limit for the SGM62110 and SGM62111 output capacitance. However, using large output capacitance results in slower response to the transients and can cause other issues when the output is discharged.

### I²C Pull-up Resistors

The standard I²C specifications and User Manual can be used to setup the I²C bus. The maximum pull-up resistor value for the required bus speed can be calculated from Equation 3:

$$R_{P\_MAX} = \frac{t_R}{0.8473 \times C_B} \quad (3)$$

Where:

$t_R$ = maximum allowed rise time (300ns for fast-mode).
$C_B$ = total capacitive load on each bus line.

$$R_{P\_MAX} = \frac{300ns}{0.8473 \times 100pF} = 3.541k\Omega$$

If the bus capacitance is not known for the application, measure the rise time with an oscilloscope starting with a 1kΩ pull-up and then calculate the $C_B$ from Equation 3 to find the maximum allowed pull-up resistor.

To find the minimum permitted pull-up resistor value for a specific bus speed, use Equation 4.

$$R_{P\_MIN} = \frac{V_{BUS} - V_{OL}}{I_{OL}} \quad (4)$$

Where:

$V_{BUS}$ is the I²C bus pull-up voltage.
$V_{OL}$ is the low-level output voltage (0.4V).
$I_{OL}$ is the low-level output current (3mA for the fast mode).

$$R_{P\_MIN} = \frac{3.3V - 0.4V}{3mA} = 967\Omega \quad (5)$$

The $R_P$ = 3.3kΩ pull-up resistor meets both requirements.

### Application Curves

Table 9 lists the component values and part numbers used for the tests and measurements outlined in the characteristic curves.

**Table 9. Components used for Characteristic Curves**

| Reference | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_1$ | Capacitor, 10μF, 6.3V, 0603, ceramic | GRM155R60J106ME15 | Murata |
| $C_2$, $C_3$ | Capacitor, 22μF, 6.3V, 0603, ceramic | GRM188R61A226ME15 | Murata |
| $L_1$ | Inductor, 0.47μH | XFL4015-471MEC | Coilcraft |
| $U_1$ | Integrated circuit | SGM62110 | SGMICRO |

# LAYOUT

## Layout Guidelines

The PCB layout is a critical part of any high-performance electronic design. The following principles should be considered in the layout design to maximize the device performance.

• Place the input and output capacitors close to their corresponding device pins in order to minimize the input and output high frequency current loop areas.

• Place the smallest capacitor of a combinational capacitance (different sizes) closest to the device.

• Use short and wide PCB traces for interconnections to minimize the parasitics.

• Use at least a 4 layer PCB stack or similar for the power supply:

Top Layer (1): Place all components and power traces

Mid layer (2): Signals

Mid layer (3): Signals

Bottom Layer (4): Ground plane

An example of the PCB layout that is used for the measurement data in Application Curves is given in Figure 27.

## Layout Example

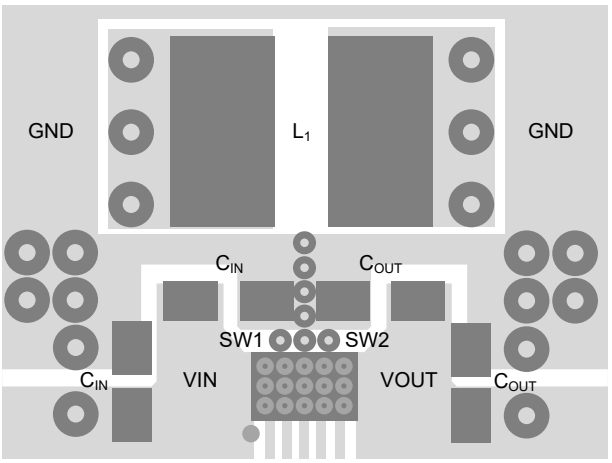
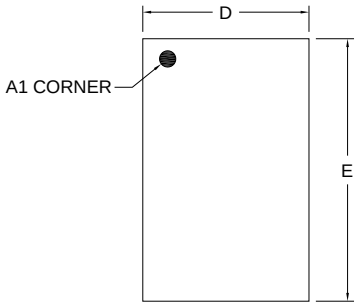


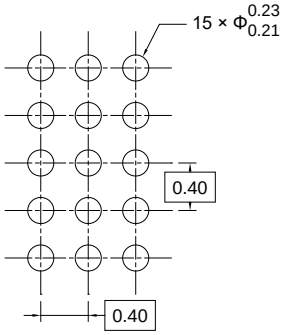

**Figure 27. Recommended PCB Layout**

# PACKAGE OUTLINE DIMENSIONS

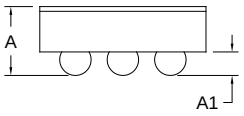
## WLCSP-2.21×1.40-15B



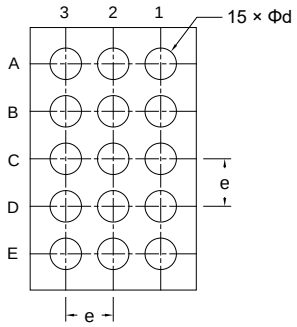

TOP VIEW




**RECOMMENDED LAND PATTERN** (Unit: mm)




SIDE VIEW



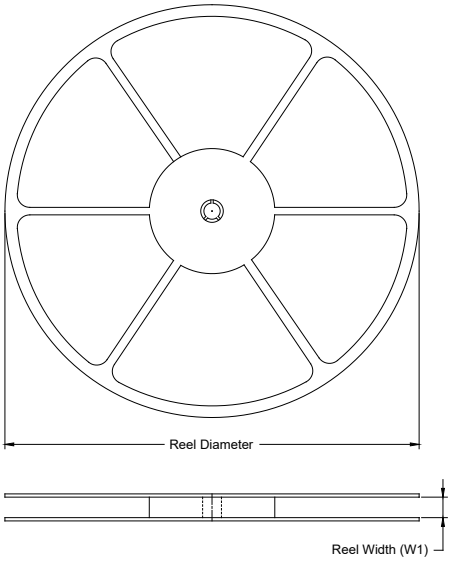

BOTTOM VIEW

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | 0.542 | 0.580 | 0.618 |
| A1 | 0.178 | 0.198 | 0.218 |
| D | 1.380 | 1.405 | 1.430 |
| E | 2.190 | 2.215 | 2.240 |
| d | 0.245 | 0.265 | 0.285 |
| e | 0.400 BSC | | |

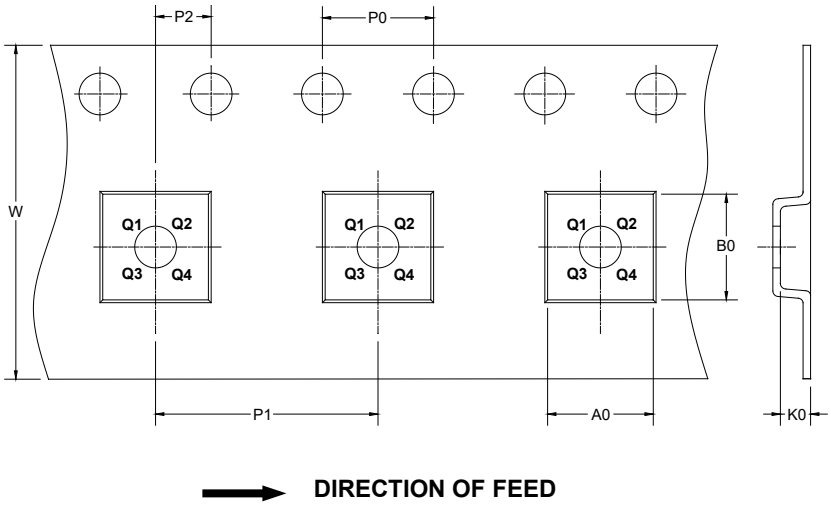
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



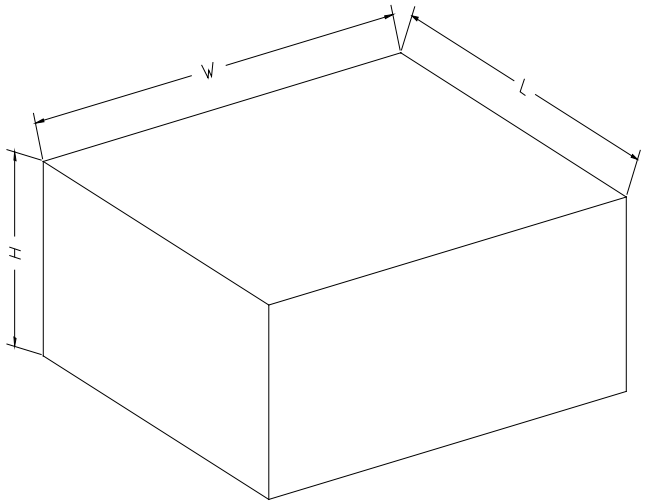

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP-2.21×1.40-15B | 7″ | 9.5 | 1.53 | 2.38 | 0.73 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002