SGM834A
140dB Range (1nA to 10mA) Logarithmic Current-to-Voltage Converter

GENERAL DESCRIPTION

The SGM834A is a single-supply logarithmic current-to-voltage converter for measuring the low frequency current signals over a large range from 1nA to 10mA. With capabilities such as photodiode adaptive biasing, active-shielding (guard driving), output buffer amplifier conditioning and voltage reference on a single chip, this device is optimized for measuring the power of optical signals by using a photodiode operating in the photo current mode. The measured current is converted and compressed to a logarithmic voltage by using transistor I-V characteristics and a compensation circuit.

The SGM834A operates with a single 3V to 5.5V supply and is equipped with a disable input to shut down the device. The input current (I_{PD}) is converted to an internal 40μA/dec logarithmic scaled current that is injected into an internal 5kΩ resistance to provide an output voltage with 10mV/dB (or 200mV/dec) logarithmic slope on the VLOG output pin. This slope can be reduced by an external shunt resistor. The intercept point (the output voltage corresponding to the selected intercept current) and the scale (to change the slope) can be adjusted by the on-chip buffer amplifier.

This device is available in a Green TSSOP-14 package and is specified over a temperature range of -40℃ to +85℃.

FEATURES

- **Patents Pending Proprietary Circuits**
- **Seven Full Decades Range**
- **3V to 5.5V Single-Supply Operation**
- **Low Power and Temperature Stable**
- **Precise Trimmed Scaling**
- **10mV/dB Logarithmic Slope at VLOG Pin**
- **100pA Basic Logarithmic Intercept**
- **Simple Slope and Intercept Adjustments**
- **15V/μs Slew Rate**
- **3.3mA (TYP) Quiescent Current (Enabled)**
- **9μA (TYP) Shutdown Current (Disabled)**
- **Available in a Green TSSOP-14 Package**

APPLICATIONS

High Accuracy Optical Power Measurement
Wide Range Baseband Log Data Compression
Versatile Detector for Automatic Power Control Loops

TYPICAL APPLICATION

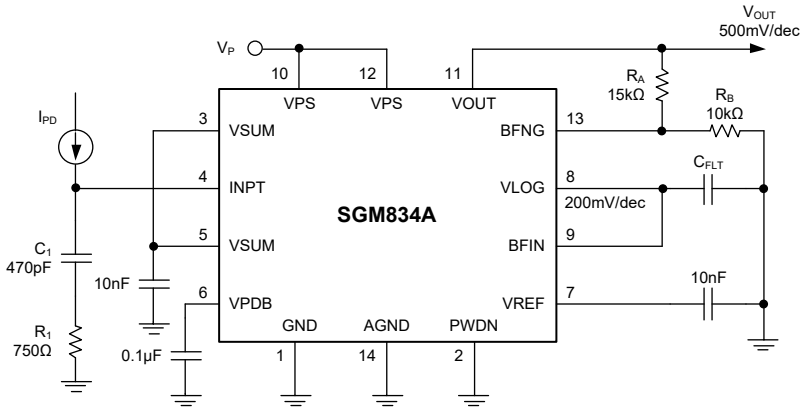


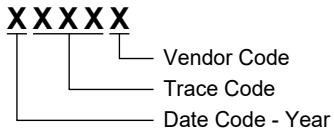
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM834A	TSSOP-14	-40℃ to +85℃	SGM834AYTS14G/TR	SGM834A YTS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines “Green” to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Input Current 20mA
Internal Power Dissipation 270mW
Package Thermal Resistance
TSSOP-14, θ_{JA} ..... 124℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 3V to 5.5V
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

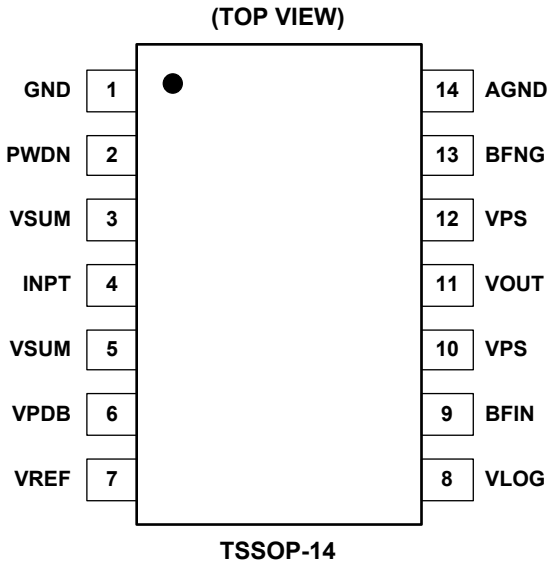
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	GND	Power Supply Ground.
2	PWDN	Power-Down (Disable) Logic Input. Pulling this pin high will disable the device, and pulling this pin low will enable the device.
3, 5	VSUM	Guard Pins. These pins are located on both sides of the INPT pin and can be connected to the shield guard of the INPT current signal for active shielding.
4	INPT	Photodiode Current Input. INPT pin is typically connected to the photodiode anode. The photo current flows into the INPT pin. (The photodiode junction is slightly reverse biased to operate as detector.)
6	VPDB	Photodiode Bias Output. VPDB pin can be connected to the photodiode cathode to provide adaptive bias control. The adaptive bias increases the reverse bias voltage as diode current increases to compensate the resistive drops inside the diode and keeps a sufficient reverse bias across the junction, such that the diode current is only determined by the incoming optical power. Otherwise, leave the pin floating.
7	VREF	Output of the 2V Internal Voltage Reference. It can be used to set the intercept point for buffer output.
8	VLOG	Output of The Logarithmic Front-End. Output of the logarithmic converter with an internal shunt resistance is R_{OUT} = 5kΩ to ground. Provide a logarithmic output voltage with a 100pA intercept and a fixed 200mV/dec slope (200mV change for each 1-decade change in the input current). The lower margin of VLOG is less than 0.1V but cannot reach 0V. Therefore, for input currents below 1nA, this output is saturated (the intercept point is out of range). The VLOG output impedance is 5kΩ.
9	BFIN	Internal Buffer Amplifier Non-Inverting Input (High Impedance).
10, 12	VPS	Positive Supply, V_P (3.0V to 5.5V).
11	VOUT	Internal Buffer Amplifier Output (Low Impedance).
13	BFNG	Internal Buffer Amplifier Inverting Input.
I4	AGND	Analog Ground (Return for the output signals and VREF).

ELECTRICAL CHARACTERISTICS

(V_P = 5V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Interface (INPT, VSUM)						
Specified Current Range	Flows into INPT pin		1nA		10mA	
Input Node Voltage	Internally preset; can be altered	T_J = +25℃	0.47	0.5	0.53	V
		T_J = -40℃ to +85℃	0.465	0.5	0.535	
Temperature Drift	T_J = -40℃ to +85℃			0.02		mV/℃
Input Guard Offset Voltage	V_{IN} - V_{SUM}, T_J = +25℃		-20		20	mV
Photodiode Bias (1) (Established between VPDB and INPT)						
Minimum Value	I_{PD} = 1nA, T_J = +25℃		70	100		mV
Trans-Resistance				300		mV/mA
Logarithmic Output (VLOG)						
Slope	1μA < I_{PD} < 1mA	T_J = +25℃	194	200	207	mV/dec
		T_J = 0℃ to +70℃	192	200	209	
	1nA < I_{PD} < 1μA	T_J = +25℃	192	200	212	
		T_J = 0℃ to +70℃	189	200	214	
Intercept (I_Z)	T_J = +25℃		70	100	130	pA
	T_J = 0℃ to +70℃		60		140	
Law Conformance Error (2)	10nA < I_{PD} < 1mA, peak error, T_J = +25℃			0.05	1.1 (3)	dB
	1nA < I_{PD} < 1mA, peak error, T_J = +25℃			0.08	2 (3)	
Maximum Output Voltage				1.6		V
Minimum Output Voltage				0.1		V
Shunt Output Resistance (R_{OUT})	T_J = +25℃		4.95	5	5.05	kΩ
Reference Output (VREF)						
Voltage (Referred to AGND)	T_J = +25℃		1.98	2	2.02	V
	T_J = -40℃ to +85℃		1.97	2	2.03	
Output Resistance				0.1		Ω
Output Buffer Amplifier (BFIN, BFNG, VOUT)						
Input Offset Voltage	T_J = +25℃		-20		20	mV
Input Bias Current	Flowing out of BFIN or BFNG pins			20		pA
Incremental Input Resistance (dv/di)				25		GΩ
Output High Voltage	Loaded with R_L = 1kΩ to ground			V_P - 0.1		V
Output Resistance				0.1		Ω
Wide-Band Noise (4)	I_{PD} > 1μA			1		μV/√Hz
Small Signal Bandwidth (4)	I_{PD} > 1μA			10		MHz
Slew Rate	0.2V to 4.8V output swing			15		V/μs

ELECTRICAL CHARACTERISTICS (continued)

(V_P = 5V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Input (PWDN)					
Logic High Level Voltage	2.7V < V_P < 5.5V	2			V
Logic Low Level Voltage	2.7V < V_P < 5.5V			1	V
Power Supply (VPS)					
Positive Supply Voltage		3	5	5.5	V
Quiescent Current (Enabled)	T_J = +25℃		3.3	5	mA
Shutdown Current (Disabled)			9		μA

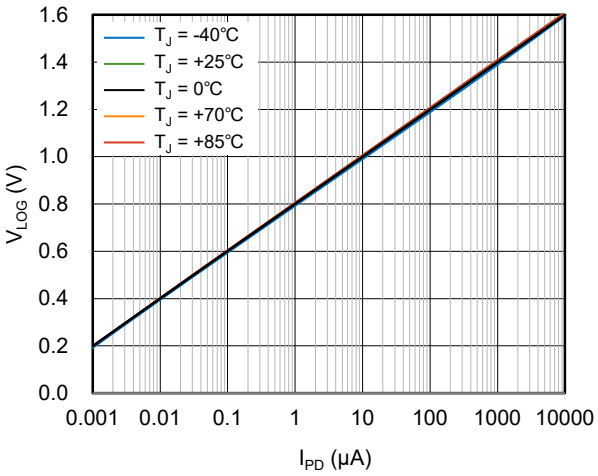
NOTES:

1. This bias is internally arranged to track the input voltage at INPT; it is not specified relative to ground.
2. The deviation of VLOG from the ideal relationship expressed as V_{LOG} = Slope × (I_{PD} - I_Z) with quantities expressed in logarithmic (dB) scale.
3. The specified minimum and maximum values are guaranteed by ATE, excluding the reliability shift.
4. Output noise and incremental bandwidth are functions of the input current.

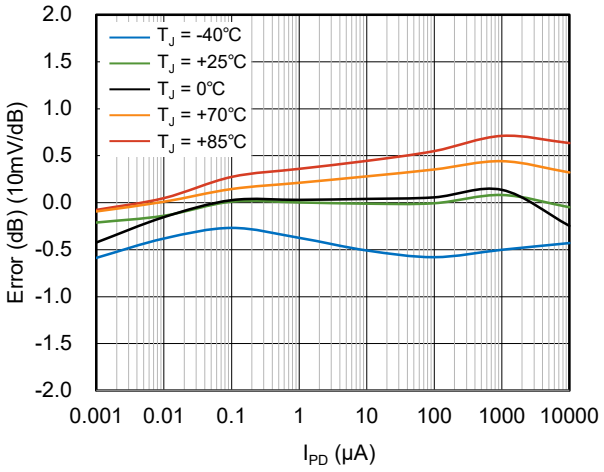
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃ and V_P = 5V, unless otherwise noted.

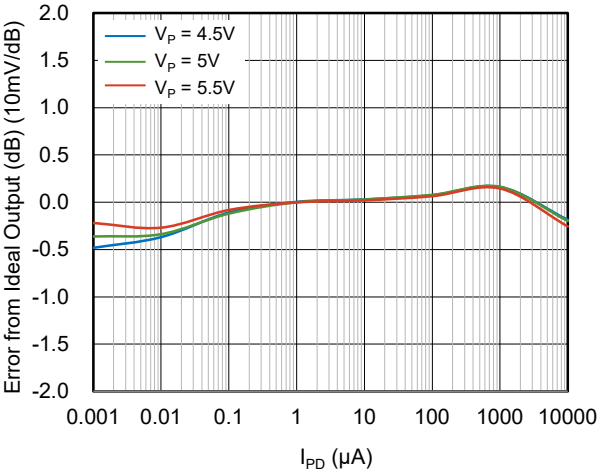
V_{LOG} vs. I_{PD}



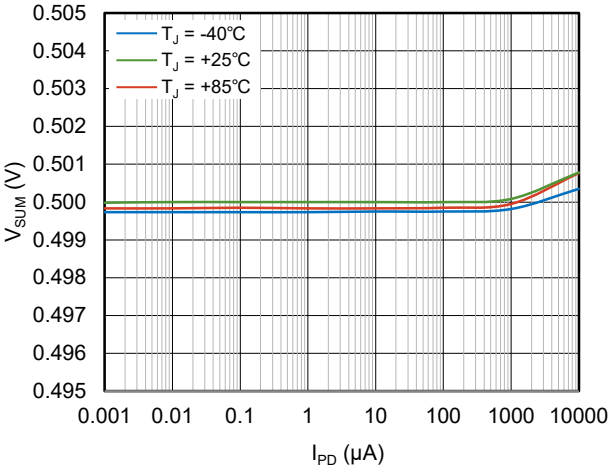
Logarithmic Conformance (Linearity) for V_{LOG}



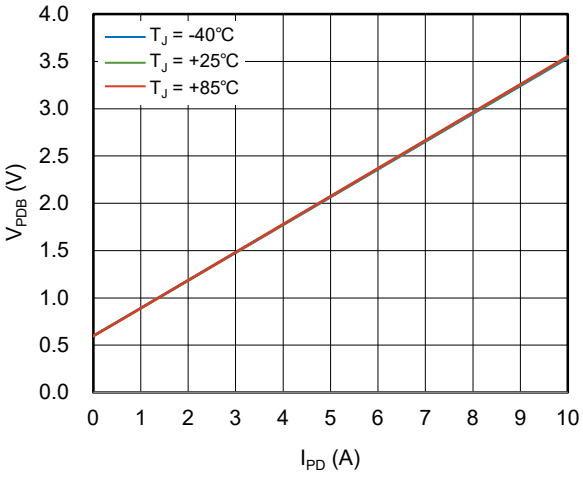
Absolute Deviation from Nominal Specified Value of V_{LOG} for Several Supply Voltages



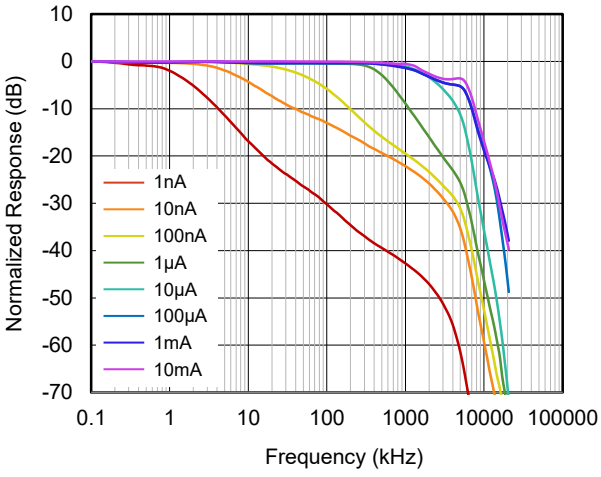
V_{SUM} vs. I_{PD}



V_{PDB} vs. I_{PD}



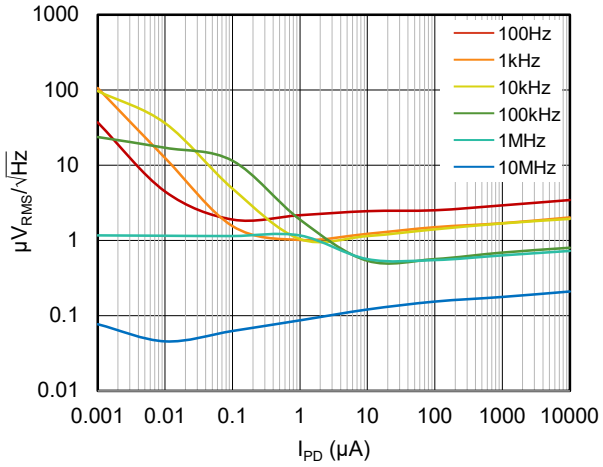
Small Signal AC Response, I_{PD} to V_{LOG} (5% Sine Modulation of I_{PD} at Frequency)



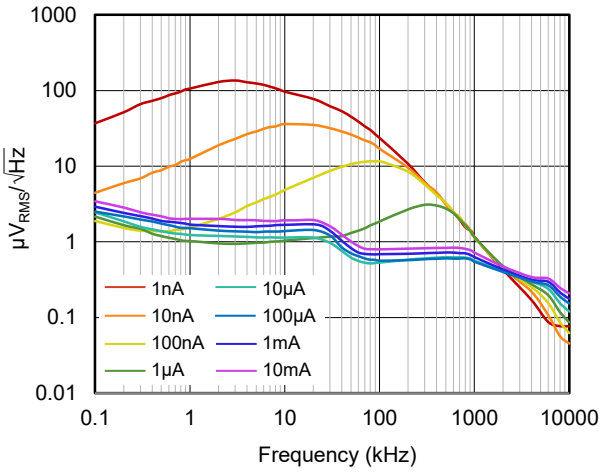
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_P = 5V, unless otherwise noted.

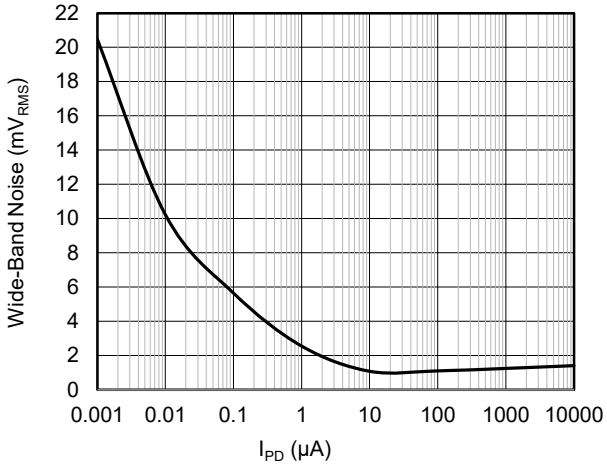
Spot Noise Spectral Density at V_{LOG} vs. I_{PD}



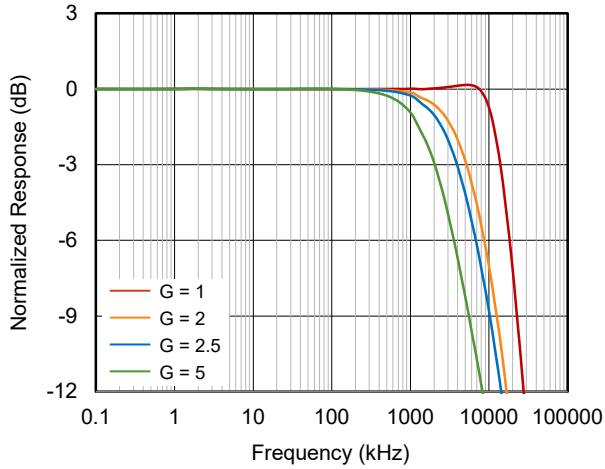
Spot Noise Spectral Density at V_{LOG} vs. Frequency



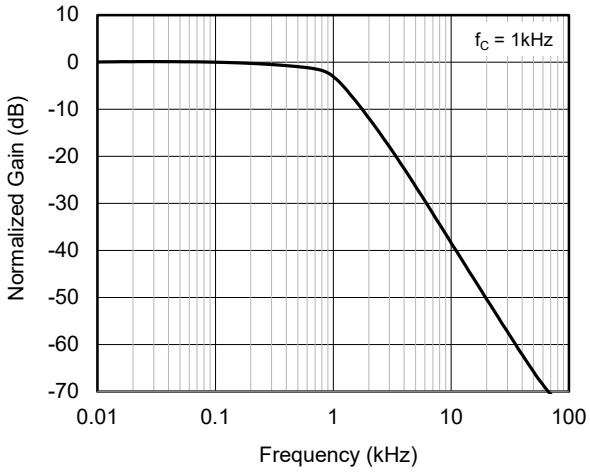
Total Wide-Band Noise Voltage at V_{LOG} vs. I_{PD}



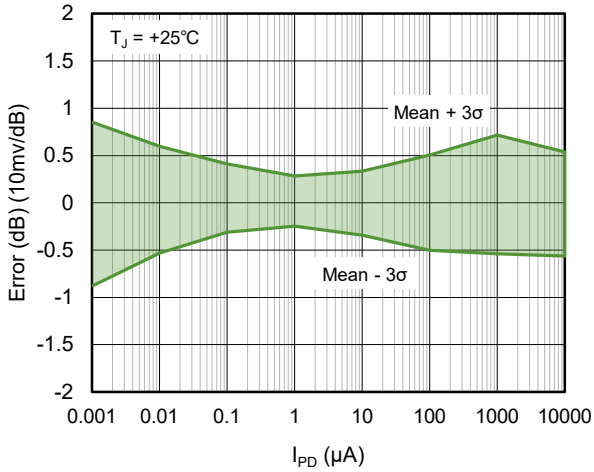
Small Signal Response of Buffer



Small Signal Response of Buffer Operating as Two-Pole Filter



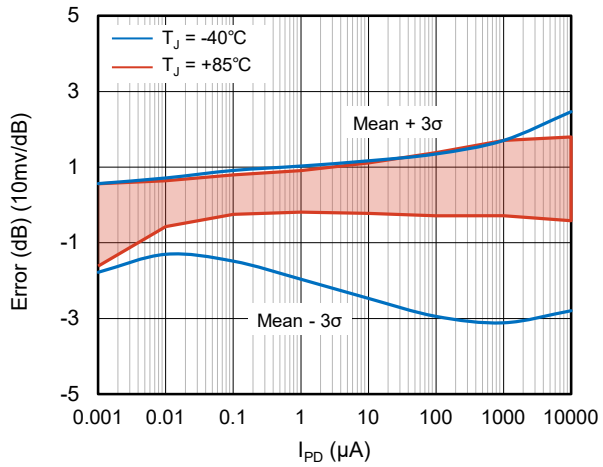
Logarithmic Conformance Error Distribution



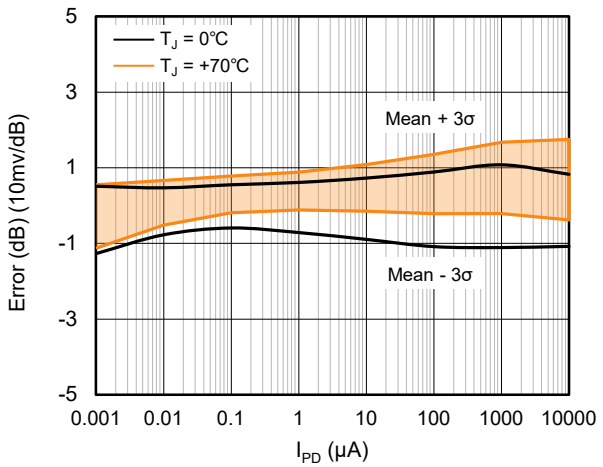
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_P = 5V, unless otherwise noted.

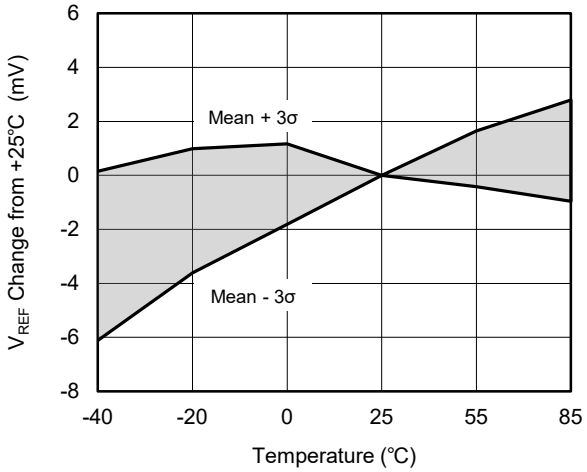
Logarithmic Conformance Error Distribution



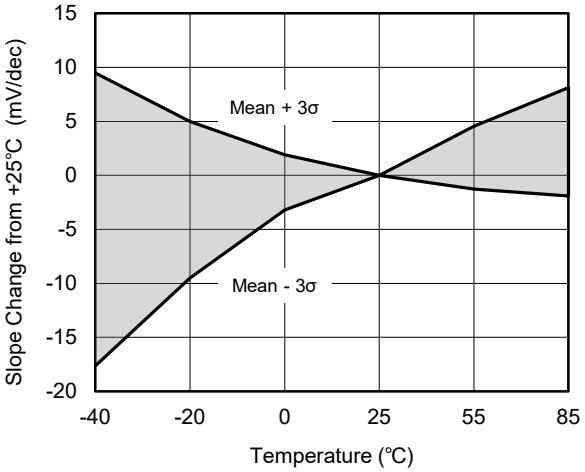
Logarithmic Conformance Error Distribution



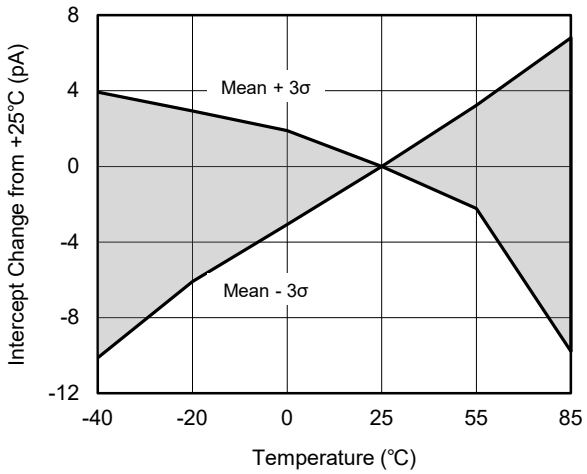
V_{REF} Drift vs. Temperature



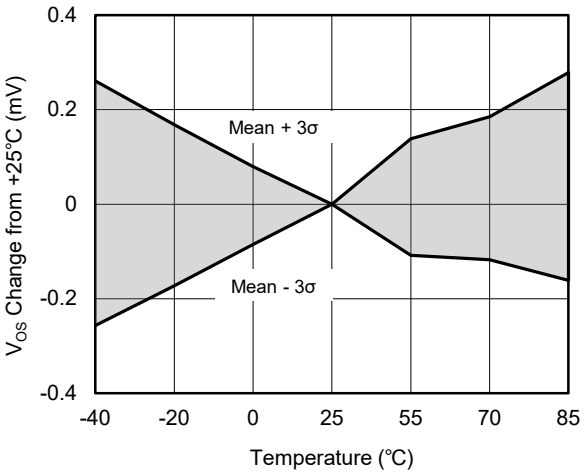
Slope Drift vs. Temperature



Intercept Drift vs. Temperature



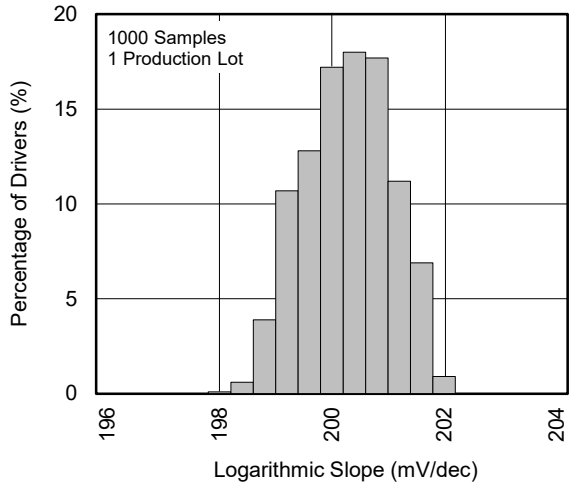
Output Buffer Offset vs. Temperature



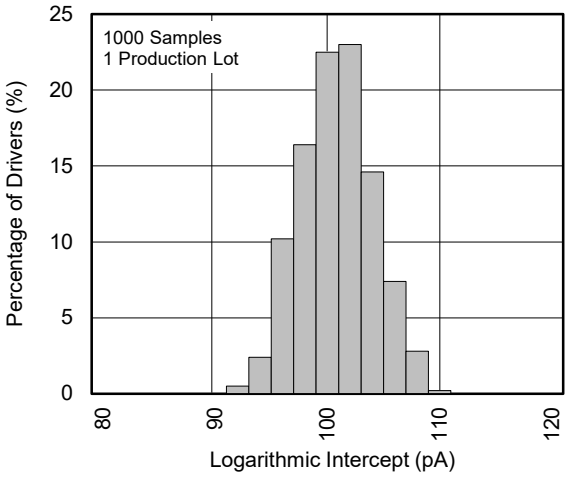
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_P = 5V, unless otherwise noted.

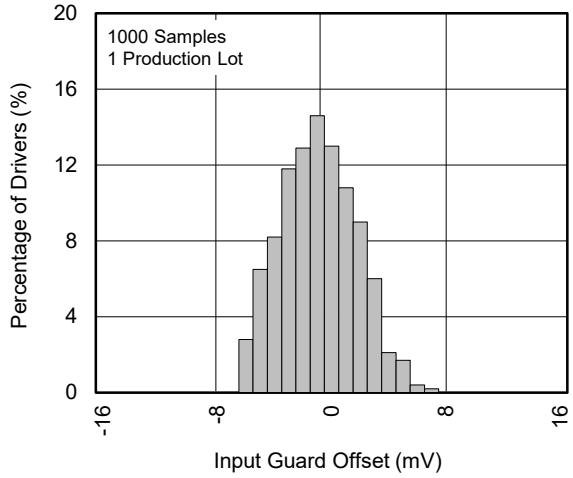
Distribution of Logarithmic Slope



Distribution of Logarithmic Slope Intercept



Distribution of Input Guard Offset Voltage (V_{INPT} - V_{SUM})



FUNCTIONAL BLOCK DIAGRAM

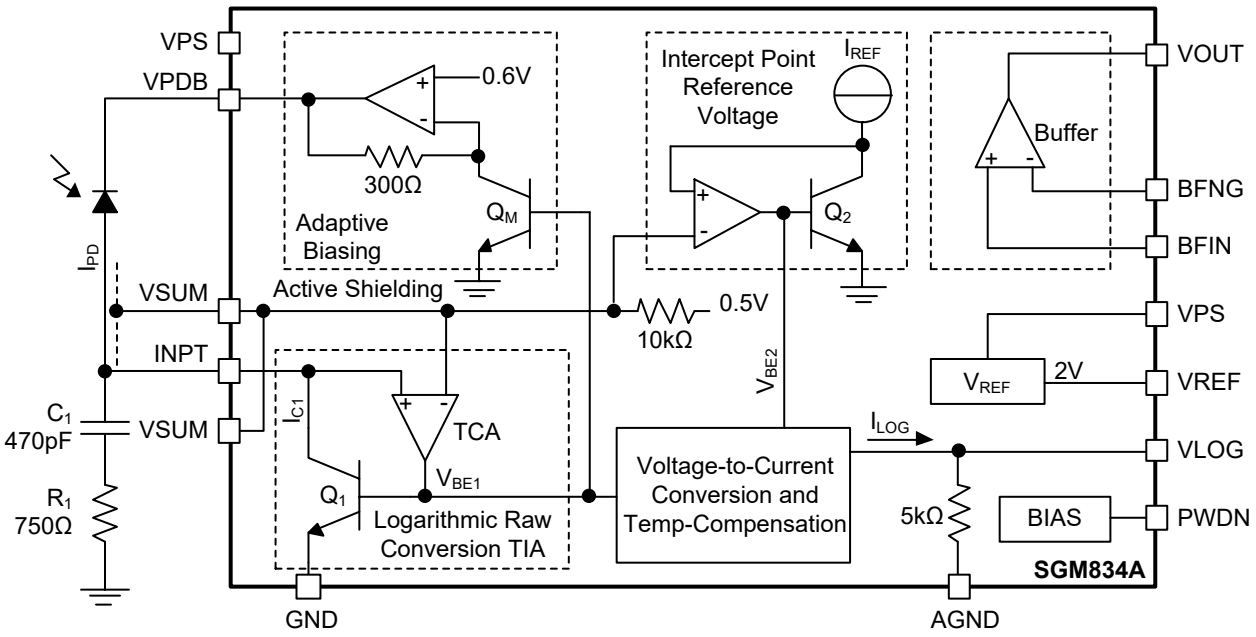


Figure 2. Functional Block Diagram

CHARACTERIZATION TEST SETUP

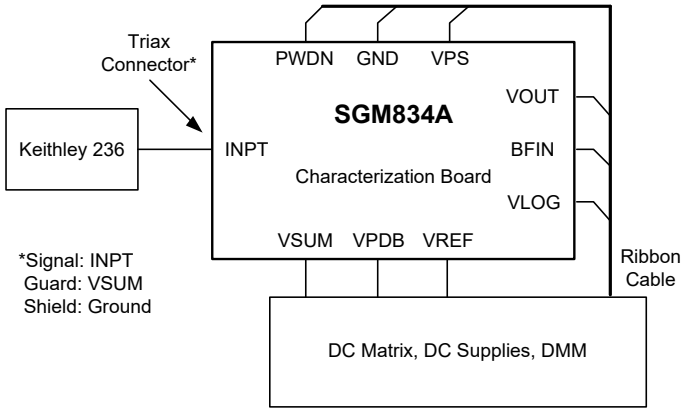


Figure 3. Primary Characterization Setup

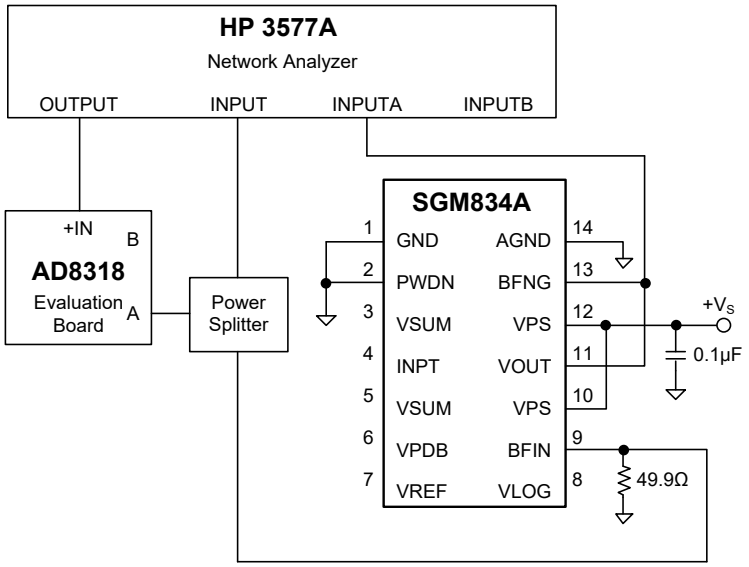


Figure 4. Buffer Amplifier Bandwidth Measurement

CHARACTERIZATION TEST SETUP (continued)

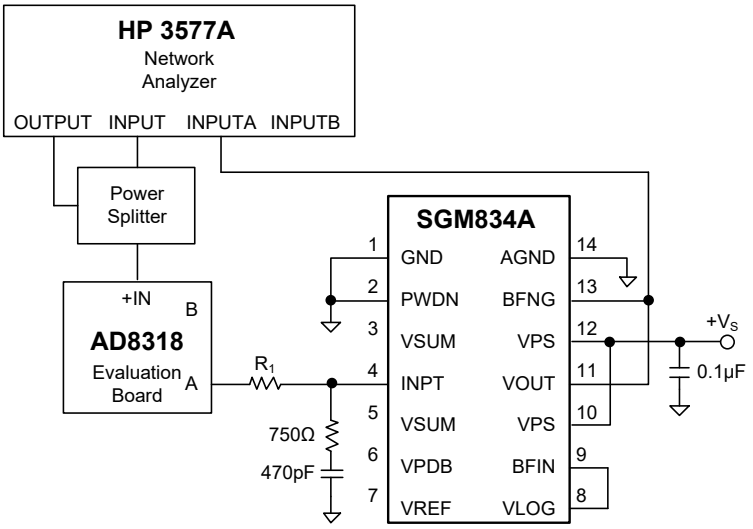


Figure 5. Converter Small Signal Bandwidth Measurement Setup

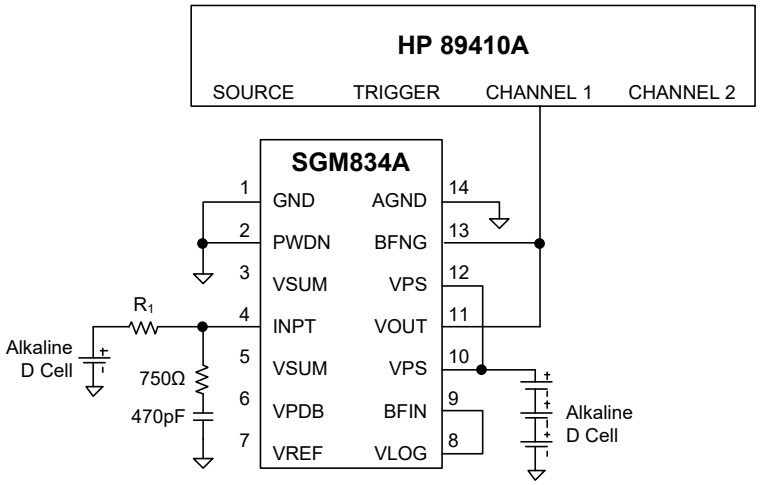


Figure 6. Noise Spectrum Measurement Setup

DETAILED DESCRIPTION

Conversion Operating Principle

Figure 2 shows the block diagram of the SGM834A, including the logarithmic conversion blocks and the required compensations blocks for law conformance. The Q_1 collector voltage is stabilized at 0.5V by a closed loop bias circuit. The 0.5V is an optimal voltage level for biasing the photodiode anode, and provides a good compromise between the diode ohmic leakage current errors that are significant at lower currents and the diode series resistance errors that are significant at higher currents. The adaptive bias block tries to keep the reverse bias across the diode junction to almost stable 0.1V by increasing the bias voltage at higher I_{PD} currents to compensate the diode bulk resistive drops. The inherent relationship of the collector current (I_C) and the base-emitter voltage (V_{BE}) in a bipolar transistor (like Q_1) is expressed as:

$$V_{BE} = V_T \times \log_e(I_C/I_S) \quad (1)$$

$$V_T = kT/q \quad (2)$$

where:
I_S is the saturation current of the transistor,
$\log_e$ is the natural logarithm operator,
V_T is the thermal voltage,
k is the Boltzmann constant (~1.38×10^{-23}J/K),
T is the absolute temperature in Kelvin (K),
q is the electron charge in Coulomb (~1.6×10^{-19}C).

Equation 1 provides the raw logarithmic principle that is used to convert the diode I_{PD} current flowing in the Q_1 collector to the logarithmic voltage V_{BE1}. Note that the fundamental relationship between V_{BE} and I_C can be scaled by both I_S and V_T. The $I_C = I_S$ determines the $V_{BE} = 0$ intercept point. The I_S and the intercept point are highly temperature and process dependent and have to be compensated such that the output is independent of the I_S and T. To compensate the I_S variations, an identical dummy transistor (Q_2) with the same geometrics and process as Q_1 is implemented in the device to generate the reference voltage (V_{BE2}) for the intercept point by setting its collector current to an stable and accurate reference current (I_{REF}). The I_{REF} has an input referenced equalization stabilized around 1μA that is 10000 times higher than the intercept current (I_Z = 100pA typical).

Because Q_1 and Q_2 have the same saturation currents and temperature dependence, the V_{BE1} - V_{BE2} is temperature and process independent at the intercept point (note that I_{REF}/I_Z is a constant).

$$V_{BE1} - V_{BE2} = kT/q \times \log_e(I_{PD}/I_{REF}) \quad (3)$$

However, at other currents, the relationship of V_{BE1} - V_{BE2} to I_C is still temperature dependent by a direct multiplication factor (proportional to T). A current mirror multiplier and a voltage to current conversion multiplier are used to compensate the temperature variations and to convert the V_{BE1} - V_{BE2} voltage to a temperature and I_S independent current (I_{LOG}). This current passes through an internal 5kΩ resistor for current to voltage conversion that provides the intermediate output voltage (V_{LOG} = 5kΩ × I_{LOG}) with a fixed 200mV/dec typical slope (200mV increase per one decade or 10× increase of I_{PD}). The logarithmic conversion is represented by:

$$V_{LOG} = 5k\Omega \times 40\mu A \times \log_{10}(I_{PD}/100pA) = 0.2V \times \log_{10}(I_{PD}/100pA) \quad (4)$$

$$\frac{\log_{10}(x)}{\log_e(x)} \approx 0.4343 \quad (5)$$

$\log_{10}$ is more convenient than $\log_e$ for per decade units used for the slope. I_Z = 100pA is the SGM834A intercept current.

Optical Power Measurement

The photodiode sensitivity defined by quantum efficiency is the number of electrons emitted as a result of the received photonic irradiation. Because the electron velocity is stable in a given electric field, the number of electrons (photo current) will be proportional to the incoming optical power. So, the I_{PD} can be measured and calibrated as an equivalent quantity with the optical power.

The logarithmic current to voltage conversion facilitates optical measurement in decibel scaling, in which the optical power is measured as a ratio to a given reference power, such as dBm that is the ratio to a 1mW reference. If the system is calibrated such that a 1mW optical power results in 1V output, then if a measurement reading is 1.2V, the optical power is calculated from 200mV × $\log_{10}$(P/1mW) = (1.2V - 1V) equation that results in P/1mW = 10 or P = 10dBm.

DETAILED DESCRIPTION (continued)

Available Output Range

The low margin for the VLOG output for proper trimming and cancellation is limited (0.1V, TYP). So, when the actual input is very close to the intercept point (I_Z = 100pA), the output is saturated to the low limit because VLOG cannot reach to zero. However, from almost a decade higher (1nA), the output is valid. The VLOG output impedance is 5kΩ. The adaptive biasing and compensation block are fully functional over the whole 3V to 5.5V supply range that helps in lowering the errors caused by diode resistive drops that could limit the effective high output range. The buffer amplifier provides a much smaller (0.1Ω, TYP) output impedance. With a 1kΩ load, this output can swing up to V_P - 0.1V. If the output is near V_P - 0.1V, the law conformance might have been lost already, because it shows that the input current is above the guaranteed operating range.

DC and AC Components

The logarithmic conversion is valid for the steady state (settled DC) component of the input signal. The high frequency AC component of the I_{PD} should be filtered and blocked from entering into the INPT pin. Otherwise, large measurement errors are expected. Compared to the averaging before conversion, the signal averaging at the output of the converter adds much more error. For example, a 50% duty cycle input pulse signal with P_{PK} (dB) power peak, results in a realistic P_{PK} - 3dB average power if the signal is averaged before conversion. However, if the converter output is averaged, the result will be a meaningless average value of P_{PK}/2 (dB) and also depends on 0dB reference.

Bandwidth and Noise

Even though the AC transfer function is meaningless for the nonlinear conversion circuit, the bandwidth data can help the evaluation of the output settling time. This is an important factor for reading and sampling the output with high accuracy and fast rate. The Q_1 acts as a feedback path in the trans-impedance amplifier (TIA) conversion (I_{PD} to V_{BE}). With low I_{PD} values, the trans-conductance (trans-linear) is very high and the loop gain is low that limits the bandwidth. It means the settling time will be long at low currents and short at higher currents due to the large variation of the loop gain. The bandwidth of TIA and the compensation network are both increased when the I_{PD} current goes high. It is necessary to stabilize the loop gain and the bandwidth. To this end, the external R_1-C_1 network is shunted with the Q_1. This will reduce the low current bandwidth even further. By using the buffer amplifier, the large bandwidth at higher currents is also limited by the buffer bandwidth.

DETAILED DESCRIPTION (continued)

Active Shielding and Adaptive Biasing

The INPT voltage level is kept at 0.5V as shown in Figure 2. The same voltage is connected to VSUM pins that are located on the two sides of the INPT pin. It is recommended to surround the photodiode anode copper stripe that connects to the INPT pin, with the same voltage that is available on VSUM pins to minimize the I_{PD} leakage by creating a zero voltage difference between the INPT and the surrounding guard.

The Q_M is a current mirror to Q_1 and its current is proportional to the Q_1 current. The Q_M current flows into a current to voltage amplifier with a 0.6V offset to generate an adaptive bias for the photodiode. The photodiode bias increases from 100mV (= 0.6V - 0.5V) minimum up to 300mV/mA × I_{PD} (mA), or the headroom limit, whichever is less. The reverse bias voltage is increased at higher currents to compensate the resistive drops in the photodiode. Note that for higher range of the input current, the supply voltage needs to be high enough for proper operation of the adaptive bias. For example, with a 10mA input, the supply voltage must be at least 3.7V, otherwise the VPDB output will be saturated that may cause measurement error. An external bias can be applied to VSUM if the INPT voltage needs to be changed from 0.5V.

The Reference and Buffer

A 2V reference and a buffer operational amplifier (OPA) are integrated on the chip. The OPA can be used for VLOG conditioning or as a conventional op-amp or comparator.

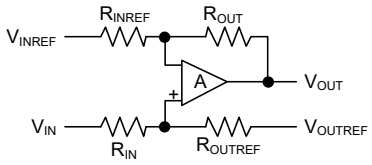


Figure 7. Re-scaling and Level-Shifting by an OPA

Figure 7 shows how the buffer can be used to shift the VIN signal that is referenced to V_{INREF} to a re-scaled V_{OUT} output signal referenced to the V_{OUTREF} voltage. The gain and level-shift are set by the four resistors.

Chip Enable

Pulling up the PWDN pin to logic high level will power down and disable the device. In this mode, the supply current drops to 9μA (TYP).

APPLICATION INFORMATION

Shielding, guarding, filtering and proper diode biasing are critical factors to minimize the noise voltage coupled to the INPT, especially when the diode current is low and the feedback signal through Q_1 is high. The diode resistive leakage (dark current) along with the multiplication and self-demodulation in the compensation multipliers can increase the errors significantly. Therefore, proper shielding, filtering and diode bias are essential before feeding the current signal for conversion.

Figure 8 shows how the parasitic leakage and R_1-C_1 network can cause delay in the negative feedback loop. It also shows how the active shielding loop provides positive feedback (bootstrap) at high I_{PD} currents by increasing the diode bias. The advantage of active shielding is insulating the INPT from ground leakage through the parasitic C_{PG} and R_{PG} elements and also from EMI pick-up. However, the penalty of shielding is larger parasitic C_{PS} that increases the delay in the negative feedback loop. Setting the corner frequency of external R_1-C_1 network to smaller values will cause slower settling at lower I_{PD} currents but quicker settling at high currents. So the span of the desired operating range and the stability (or settling) of the converter need to be compromised depending on the application requirements.

Figure 9 shows some additional circuits for the photodiode bias and I_{PD} signal filtering. The C_{PDB}-R_{PDB} low pass R-C network reduces the bandwidth of the adaptive biasing loop and helps the stability at high currents. The C_{PD}-R_{PD} RC low pass filter network averages the I_{PD} before feeding it to the converter to suppress the error caused by the multiplication self-demodulation at low bit rate data communication applications.

Note that VLOG output filtering is not helpful for error suppression.

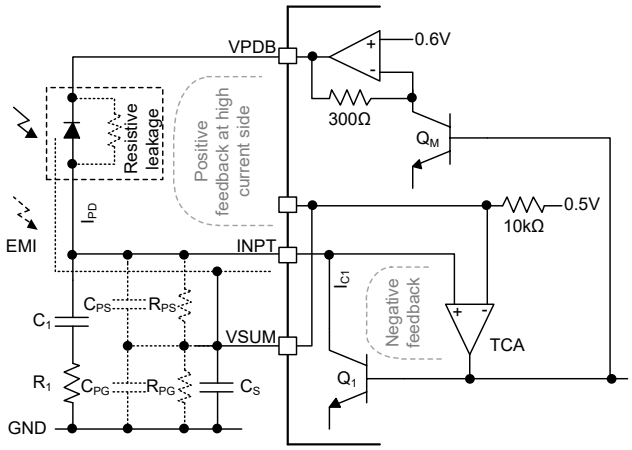


Figure 8. Conversion Loop and Active Shielding Loop

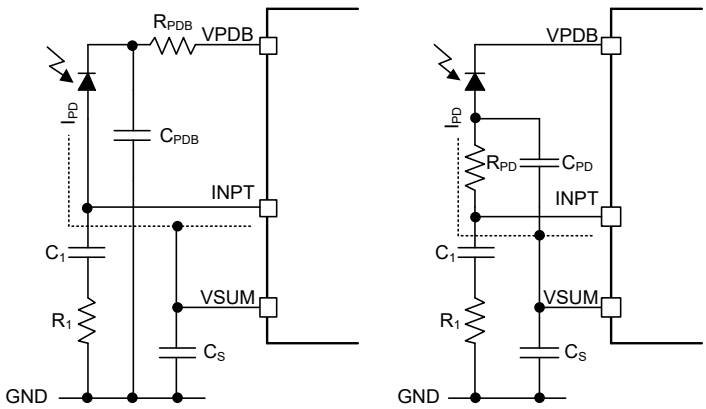
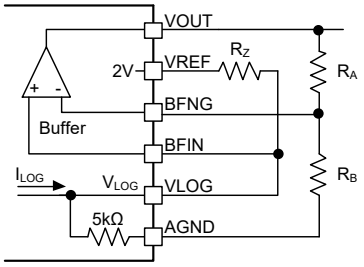


Figure 9. Filtering the VPDB and I_{PD}

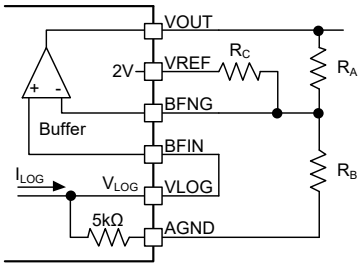
APPLICATION INFORMATION (continued)

VLOG Output Conditioning

The on-chip buffer amplifier and voltage reference can be used for adjusting the output intercept point and the scaling needed to match the desired signal level of the downstream process. Figure 10 shows the circuits that can be used for lowering or raising the intercept point.



(a) Lowering the intercept point



(b) Raising the intercept point

Figure 10. Adjusting the Intercept Point and Scaling

Table 1 lists some examples for selecting resistors for a few slope scales values while the intercept point is reduced from the I_Z = 100pA. V_Y in mV/dec is called the slope voltage.

Table 1. Some Examples of Lowering the Intercept Point

V_Y (mV/dec)	I_Z (pA)	R_A (kΩ)	R_B (kΩ)	R_Z (kΩ)
200	1	20.0	100	25
200	10	10.0	100	50
200	50	3.01	100	165
300	1	10.0	12.4	25
300	10	8.06	12.4	50
300	50	6.65	12.4	165
400	1	11.5	8.2	25
400	10	9.76	8.2	50
400	50	8.66	8.2	165
500	1	16.5	8.2	25
500	10	14.3	8.2	50
500	50	13.0	8.2	165

The following equation can be used for calculating the resistors when a lower intercept point is desired:

$$V_{OUT} = G \times \left[V_Y \times \frac{R_Z}{R_Z + R_{LOG}} \times \log_{10}\left(\frac{I_{PD}}{I_Z}\right) + V_{REF} \times \frac{R_{LOG}}{R_{LOG} + R_Z} \right] \quad (6)$$

where: $G = 1 + \frac{R_A}{R_B}$ and R_{LOG} = 5kΩ.

Usually it is more useful to raise the intercept point. Note that raising the intercept point reduces all output values. Figure 10 (b) shows how the intercept point is raised by placing the R_C between the BFNG and VREF pins. This arrangement raises the BFNG voltage (with zero input signal) and pushes the VOUT to lower values. Note that with the R_C connected to the BFNG pin, the gain (G) is also affected, but it can be compensated and re-adjusted by R_A and R_B. Use the following equation for calculating the resistors (Figure 10 (b)):

$$V_{OUT} = G\left[V_Y \times \log_{10}\left(\frac{I_{PD}}{I_Z}\right) - V_{REF} \times \frac{R_A \,||\, R_B}{R_A \,||\, R_B + R_C} \right] \quad (7)$$

where: $G = 1 + \frac{R_A}{R_B \,||\, R_C}$ and $R_A \,||\, R_B = \frac{R_A \times R_B}{R_A + R_B}$.

Table 2. Some Examples for Raising the Intercept

V_Y (mV/dec)	I_Z (nA)	R_A (kΩ)	R_B (kΩ)	R_C (kΩ)
300	10	7.5	37.4	24.9
300	100	8.25	130	18.2
400	10	10	16.5	25.5
400	100	9.76	25.5	16.2
400	500	9.76	36.5	13.3
500	10	12.4	12.4	24.9
500	100	12.4	16.5	16.5
500	500	11.5	20.0	12.4

APPLICATION INFORMATION (continued)

In most cases, a single-pole filter made by a capacitor (C_{FLT}) between the VLOG and AGND works well for output filtering as shown in Figure 1. If a high-performance measurement system with lower noise is required, a slightly more complex filter such as a two-pole Sallen-Key filter can be used as shown in Figure 11. The precise 5kΩ source impedance is needed as a part of the Sallen-Key filter network (considering the Thevenin equivalent of the VLOG output).

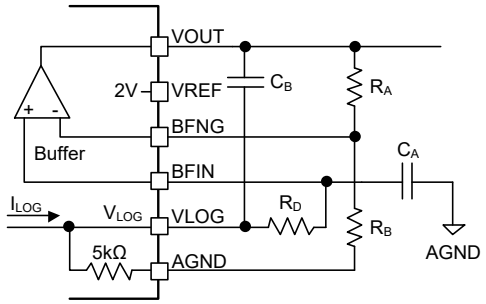


Figure 11. Using Sallen-Key Filter to Improve Settling

Some starting points for selecting the filter components for a few gain (G) examples and 1kHz cut-off frequency are provided in Table 3. The cut-off frequency can be increased or decreased by scaling the capacitor values. For example, to reduce the cut-off frequency to 100Hz, C_A and C_B should be increased by a factor of 10.

The values of R_D, G, and C_A/C_B ratio should not deviate from the suggested values in Table 3 to maintain the shape of the filter response.

Table 3. Filter Parameters for 1kHz Cut-off Frequency

R_A (kΩ)	R_B (kΩ)	G	V_Y (V/dec)	R_D (kΩ)	C_A (nF)	C_B (nF)
0	open	1	0.2	11.3	12	12
10	10	2	0.4	6.02	33	22
12	8	2.5	0.5	12.1	33	18
24	6	5	1.0	10.0	33	18

SGM834A Evaluation Board

An evaluation board is available for the SGM834A with the schematic provided in Figure 12. The EVB can be configured for a wide variety of experiments. By default, the EVB is factory-set for a diode detector in photoconductive mode with a buffer gain of unity, 10mV/dB slope, and 100pA intercept point. By configuring the EVB resistors and capacitors, all application circuits and options presented in this datasheet can be evaluated as summarized in Table 4.

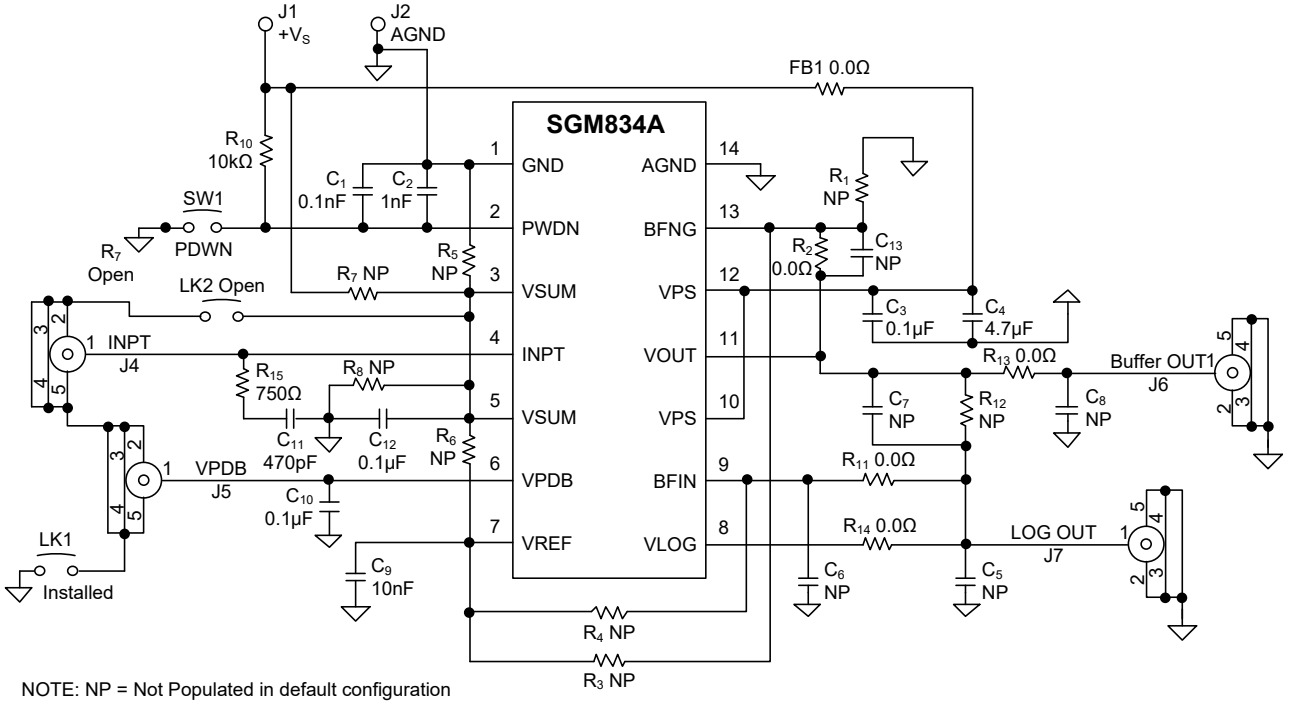


Figure 12. SGM834A Evaluation Board Schematic

APPLICATION INFORMATION (continued)

Table 4. Evaluation Board Configuration Options

Component	Function	Default Condition
V_S, AGND	Positive Supply and Ground Pins	NA
SW1, R_{10}	Device Enable: With SW1 switch in the “0” position, the PWDN pin is grounded and the SGM834A operates in normal mode.	SW1 = Installed R_{10} = 10kΩ
R_1, R_2	Buffer Amplifier Gain/Slope Adjustment: The logarithmic slope of the SGM834A can be changed by gain-setting resistors (R_1 and R_2) of the buffer amplifier.	R_1 = Open R_2 = 0Ω
R_3, R_4	Intercept Adjustment: These resistors can apply DC offset to the buffer amplifier inputs to adjust the effective logarithmic intercept.	R_3 = NP
		R_4 = NP
R_5, R_6, R_7, R_8	Bias Adjustment: The VSUM and INPT voltages can be set by these resistors.	R_5 = R_6 = NP R_7 = R_8 = NP
C_1, C_2, C_3, C_4, C_9	Power Supply, VREF and PWDN Decoupling Capacitors.	C_1 = 0.1nF C_2 = 1nF C_3 = 0.1μF C_4 = 4.7Mf C_9 = 10nF
C_{10}	Photodiode Bias Output Decoupling Capacitor: Provides high frequency decoupling for the adaptive bias output at pin VPDB pin.	C_{10} = 0.1μF
C_{12}	VSUM Decoupling Capacitor.	C_{12} = 0.1μF
C_5, C_6, C_7, C_8, R_{11}, R_{12}, R_{13}, R_{14}	Output Filter Configuration: These components can be used to implement a variety of filter configurations, from a simple low-pass RC filter to a three-pole Sallen-Key filter.	C_5 = C_6 = NP C_7 = C_8 = NP R_{11} = R_{13} = 0Ω R_{12} = NP R_{14} = 0Ω
R_{15}, C_{11}	Input Filtering: This RC network sets the essential HF compensation at the input pin (INPT).	R_{15} = 750Ω C_{11} = 470pF
LK1, LK2	Guard/Shield Options: The shells of the SMA input connectors for the photodiode and bias can be either connected to active shield driver on the VSUM pin or connected to ground.	LK1 = Installed LK2 = Open

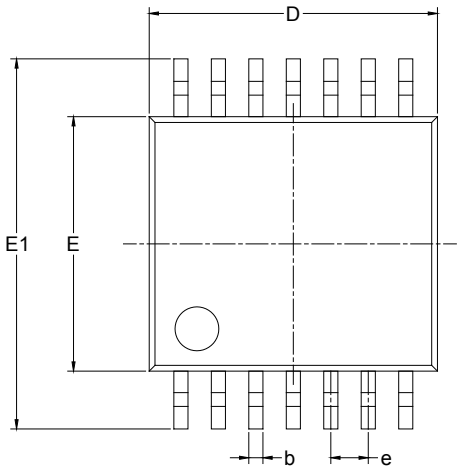
REVISION HISTORY

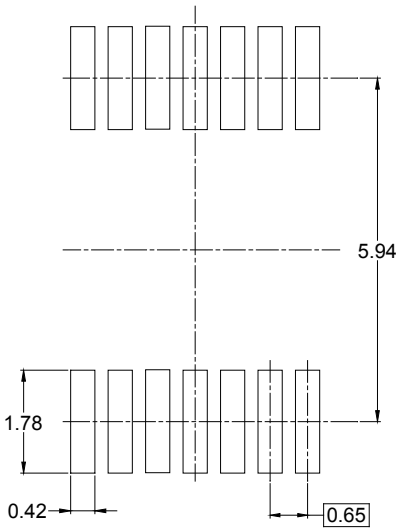
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (FEBRUARY 2022) to REV.A	Page
Changed from product preview to production data	All

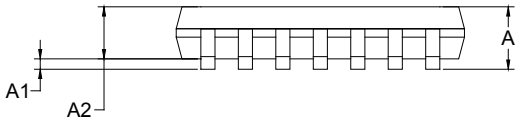
PACKAGE OUTLINE DIMENSIONS

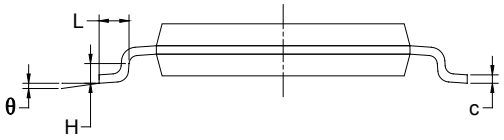
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

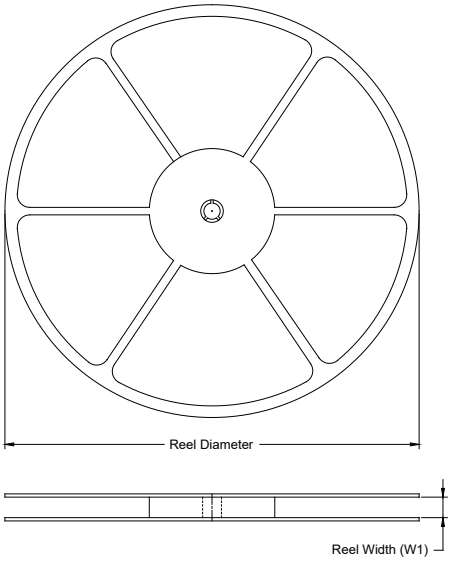




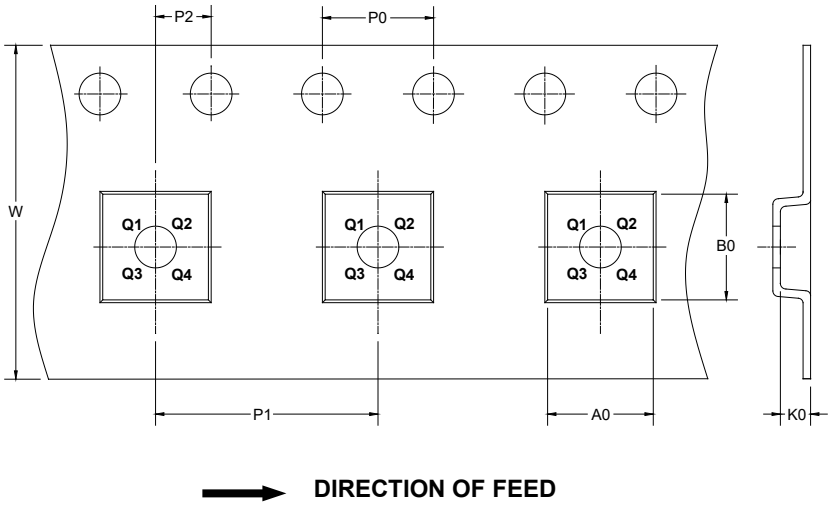
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

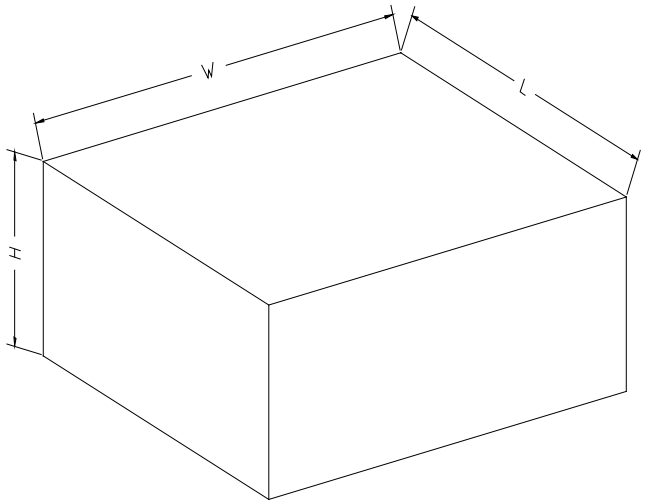
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002