SGM2541
28V/16V Bidirectional Load Switch with Wireless/Dual Input Capability

GENERAL DESCRIPTION

The SGM2541 is a high-current, low-loss bidirectional load switch and over-voltage protection (OVP) device with wireless/dual input capability.

The device supports up to 20V DC operating input voltage (28V DC withstand) at USBIN pins, and a 16V DC reverse voltage blocking feature at OUT pins. The SGM2541 provides input voltage-clamped protection for input surge events up to 130V. The integrated high-speed input over-voltage protection capability ensures safe operation for surge events that occur during the on-state (conducting) or off-state (non-conducting). The two OVP threshold voltages (17V/13V) can be programmed through VP pin.

A second input and 2:1 power multiplexer can be achieved by connecting a compatible wireless receiver (wireless Rx) output to the load switch OUT pins.

The bidirectional device can detect and support USB-OTG applications. It also includes under-voltage lockout, over-voltage lockout and over-temperature protection circuits designed to automatically isolate the power switch terminals when a fault condition occurs.

The SGM2541 is available in a Green WLCSP-2.43×1.75-20B package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Bidirectional Switch for USBIN and OUT to Allow On-The-Go (OTG) Mode**
- **Input Voltage Range:**
  3V to 20V at USBIN and 3V to 16V at OUT
- **Programmable OVP Threshold Voltages**
- **28V Tolerance on USBIN Pin**
- **130V Surge Protection**
- **5A Continuous Current from USBIN to OUT**
- **5A Continuous Current from OUT to USBIN in OTG Mode**
- **Low On-Resistance: 29mΩ (TYP)**
- **1.4V Control Logic**
- **Soft-Start to Reduce Input Peak Current**
- **Available in Green WLCSP-2.43×1.75-20B Package**
- **-40℃ to +85℃ Operating Temperature Range**

APPLICATIONS

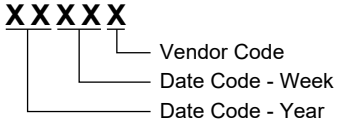
Smart Phone
Tablet PC
Mobile Devices with Wireless Charging Options

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2541	WLCSP-2.43×1.75-20B	-40℃ to +85℃	SGM2541YG/TR	XXXXX 2541YG	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{USBIN_ABSMAX} 28V
V_{USBIN} to V_{OUT} (Differential Input, Blocking) 28V
V_{OUT} to V_{USBIN} (Differential Input, Blocking) 16V
V_{OUT_MAX}, V_{USB_SNS} 20V
Control Pin Voltages 6V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 3V to 20V
Operating Ambient Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

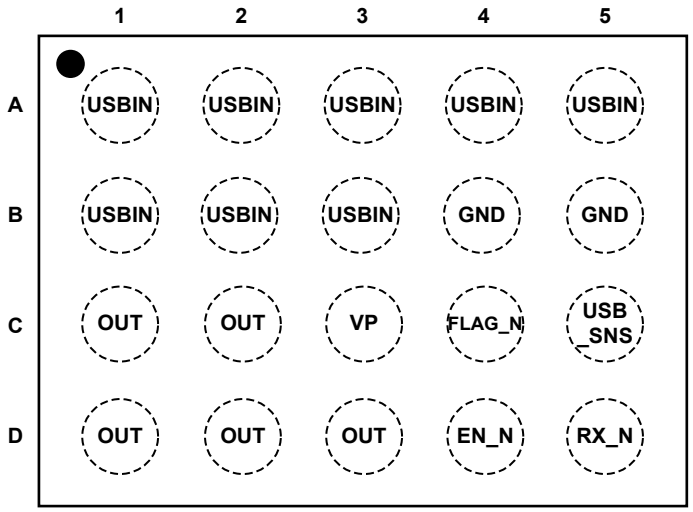
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.43×1.75-20B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1 - A5, B1 - B3	USBIN	Power Pin, Load Switch Input Pin. Connect a capacitor from this pin to the GND plane.
B4, B5	GND	Ground Pin. Connect this pin to the external ground plane close to the USBIN decoupling capacitors.
C1, C2, D1 - D3	OUT	Power Pin, Load Switch Output Pin. Connect this pin to the output capacitors, charger input pin, and wireless Rx output node for dual input configurations.
C3	VP	Digital Input. OVP voltage programming pin allows programming of one of two OVP-fast voltage thresholds. Connect the pin to GND to select 17V (TYP). Float the pin to select 13V (TYP).
C4	FLAG_N	Digital I/O Pin. The flag pin is pulled high to indicate to the system that OTG mode can be triggered in autonomous mode. Slave mode: Pull this pin logic low, or tie to external GND plane. Autonomous mode: Connect to the system digital input/output pin (or equivalent) that pulls logic low to enter OTG mode when USBIN is connected to an OTG load and a power source is applied to OUT.
C5	USB_SNS	Analog Output Pin. USB_SNS is a Clamped USBIN Sense Pin. In slave mode, connect this pin to the system's input sense pin that can respond to a valid USBIN voltage. This pin is optional in autonomous mode for system diagnostic purposes. An optional ceramic capacitor may be added from this pin to GND, sized as needed.
D4	EN_N	Digital Input Pin. Active Low Logic Enable Pin. Slave mode: Connect this pin to the system's enable logic pin. Autonomous mode: Pull this pin logic low, or tie it to the external GND plane.
D5	RX_N	Digital I/O Pin. Wireless Rx Active Low Logic Enable Pin. Slave mode: Pull this pin logic low, or tie to an external GND plane. Autonomous mode: Connect this pin to the wireless Rx active low enable pin if a system output control pin is not available.

ELECTRICAL CHARACTERISTICS

(V_{USBIN} = 5V, V_{OUT} = 5V, C_{USBIN} = 1μF, C_{OUT} = 10μF, C_{USB_SNS} = 1μF, Full = -40℃ to +85℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{USBIN}		Full	3		20	V
Output Voltage Range	V_{OUT}		Full	3		V_{OVP}	V
Input/Output Under-Voltage Lockout	V_{UVLO_USBIN}	Rising	+25℃		2.84	2.97	V
	V_{UVLO_OUT}	Rising	+25℃		2.65	2.78	
UVLO Hysteresis	V_{UVLO_HYS}		+25℃		0.52		V
Input Over-Voltage Protection Threshold	V_{OVP}	V_{USBIN} > V_{OVP} enters fault state; the VP pin is tied to ground.	Full	16.38	17	17.62	V
		V_{USBIN} > V_{OVP} enters fault state; the VP pin is floating.	Full	12.52	13	13.46	V
V_{OVP} Hysteresis	V_{OVP_HYS}		+25℃		0.43		V
Maximum USB_SNS Pin Clamping Voltage	V_{USB_SNS}	I_{USB_SNS} = 0, the VP pin is tied to ground.	Full	16.61	17.3	18	V
		I_{USB_SNS} = 0, the VP pin is floating.	Full	12.75	13.3	13.76	V
Sense Pin Voltage Drop When Loaded	ΔV_{USB_SNS}	I_{USB_SNS} = 20mA	+25℃		30	50	mV
Input Quiescent Current in Operating State	$I_{Q\_USBIN\_OP}$	Switch conducting, USBIN = 5V.	Full		123	190	μA
	$I_{Q\_OUT\_OP}$	Switch conducting, OUT = 5V.	Full		125	190	
Input Quiescent Current in Clamping State	$I_{Q\_USBIN\_CLAMP}$	USBIN-GND current (clamping).	+25℃			5	mA
OUT Float Voltage	$V_{USBIN-OUT(FLOAT)}$	Switch not conducting, V_{USBIN} = 4.5V to 20V. 4MΩ resistor is always connected between OUT and GND.	+25℃			2	V
USBIN Float Voltage	$V_{OUT-USBIN(FLOAT)}$	Switch not conducting, V_{OUT} = 4.5V to V_{OUT_MAX}. 2MΩ resistor is always connected between USBIN and GND.	+25℃			2	V
On-Resistance	R_{ON}	Measured between USBIN and OUT when the switch is conducting, EN_N = low.	+25℃		29	39	mΩ
Continuous Output Current	I_{OUT}, I_{OTG}		+25℃		±5.0		A
OUT Discharge Resistance	R_{DIS_USBIN}	Measured from the USBIN to GND during the discharge event.	+25℃		1200		Ω
	R_{DIS_OUT}	Measured from the OUT to GND during the discharge event.	+25℃		500		
Input Debounce Time	t_{DEB}	V_{UVLO} < V_{USBIN} < V_{OVP}, soft-start starts after the debounce time (rising UVLO, falling OVP); EN_N = low.	+25℃		50		ms
Discharge Time	t_{DIS_OUT}	Discharge of OUT	+25℃		50		ms
	t_{DIS_USBIN}	Discharge of USBIN	+25℃			25	
Input Rising Disable Delay	$t_{OVP-DLY}$	Valid V_{USBIN} which transitions to V_{USBIN} > OVP fast event.	+25℃		80		ns
Initialization Time of Power	t_{INIT}	Upon USBIN or OUT crossing UVLO	+25℃		150		μs
Logic Pin Turn-On/Off Delay: EN_N, FLAG_N	t_{LDELAY}	Time delay from EN_N/FLAG_N enable/ disable load switch, excluding a soft-start.	+25℃		100		μs
Input Capacitance	C_{USBIN}	Actual capacitance.	+25℃			10	μF
OTG Hot Swap Capacitance	C_{OTG}	Actual capacitance.	+25℃			200	μF
Output Capacitance	C_{OUT}	Actual capacitance.	+25℃			20	μF
Input Leakage Current: EN_N, FLAG_N	I_{LEAK}	V_{USBIN}/V_{OUT} = 5V.	+25℃			1	μA

ELECTRICAL CHARACTERISTICS (continued)

(V_{USBIN} = 5V, V_{OUT} = 5V, C_{USBIN} = 1μF, C_{OUT} = 10μF, C_{USB_SNS} = 1μF, Full = -40℃ to +85℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ENABLE, START-UP, CLAMP FEATURES							
Logic Input Threshold High Level	V_{IH}	EN_N, FLAG_N	Full	1.2			V
Logic Input Threshold Low Level	V_{IL}	EN_N, FLAG_N	Full			0.4	V
Logic Output Threshold High Level	V_{OH}	RX_N, FLAG_N	Full	1.6			V
Logic Output Threshold Low Level	V_{OL}	FLAG_N	Full			0.6	V
Open Drain Internal Pull-Up Resistance: FLAG_N/RX_N	$R_{PULL-UP}$		+25℃		500		kΩ
Open Drain Internal Pull-Down Resistance: RX_N	$R_{PULL-DOWN}$		+25℃		4.5		kΩ
Internal Pull-Up Current: VP	$I_{PULL-UP}$		+25℃		8.5		μA
Soft-Start Time	t_{SS_USBIN}	USBIN = 5V, OUT from 10% to 90% of USBIN	+25℃		0.35		ms
	t_{SS_OUT}	OUT = 5V, USBIN from 10% to 90% of OUT	+25℃		0.64		ms
	$t_{SS\_USB\_SNS}$	USBIN = 5V, USB_SNS from 0.5V to 4.5V, not loaded	+25℃		0.23		ms
THERMAL							
Over-Temperature Shutdown Threshold	t_{SD}	Temperature Rising.			157		℃
Over-Temperature Shutdown Hysteresis	t_{HYS}				21		℃

FUNCTIONAL BLOCK DIAGRAM

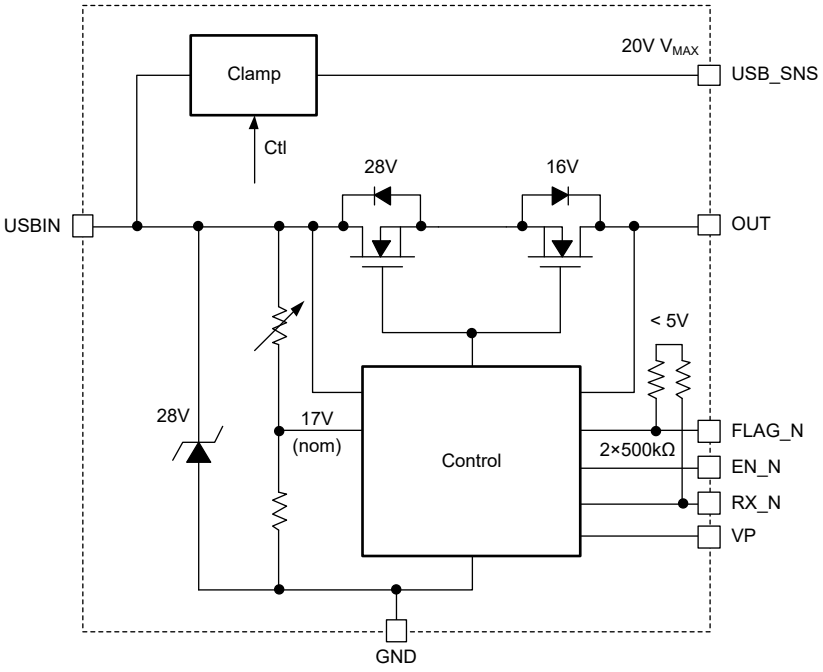
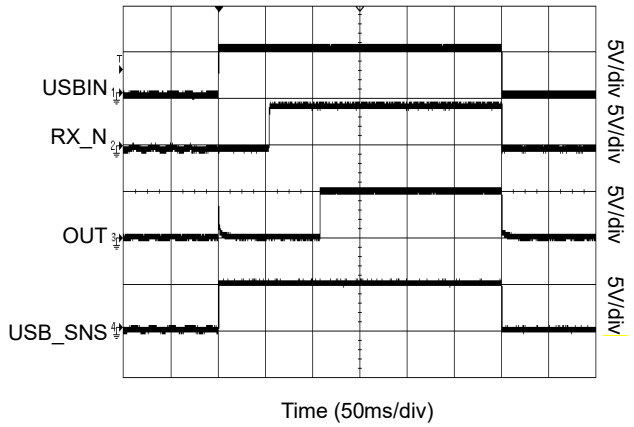


Figure 1. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

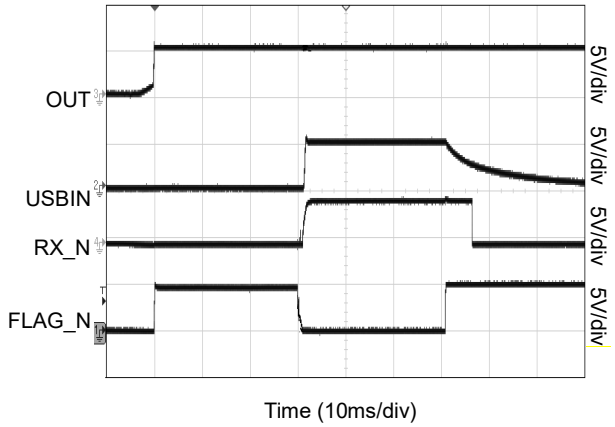
At T_A = +25℃, C_{USBIN} = 1μF, C_{OUT} = 10μF, C_{USB_SNS} = 1μF, unless otherwise noted.

Charging Power-Up and Power-Off in Autonomous Mode



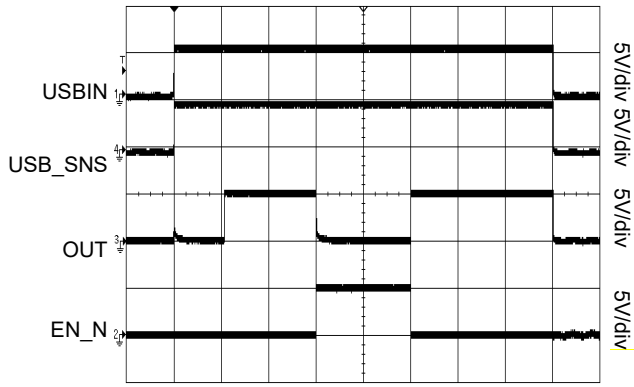
Time (50ms/div)

OTG Activate and Deactivate in Autonomous Mode



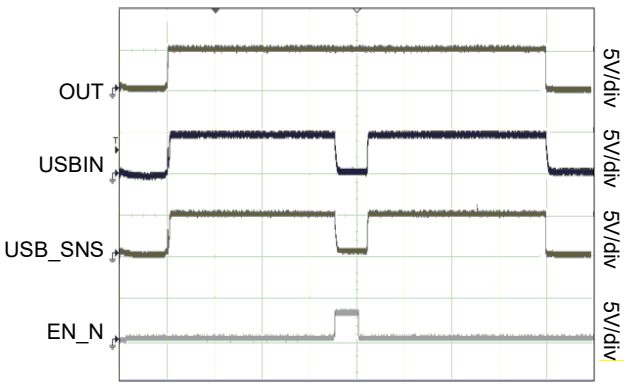
Time (10ms/div)

Charging Activate and Deactivate in Slave Mode



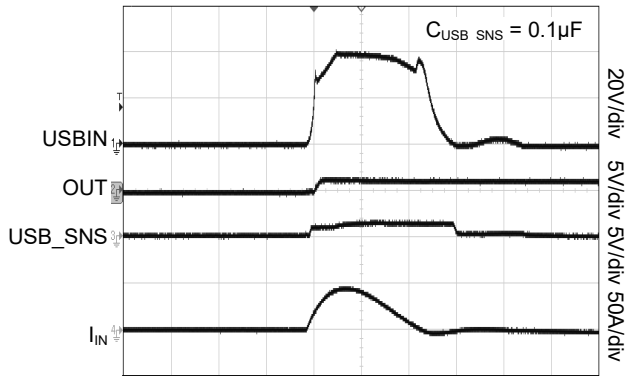
Time (50ms/div)

OTG Activate and Deactivate in Slave Mode



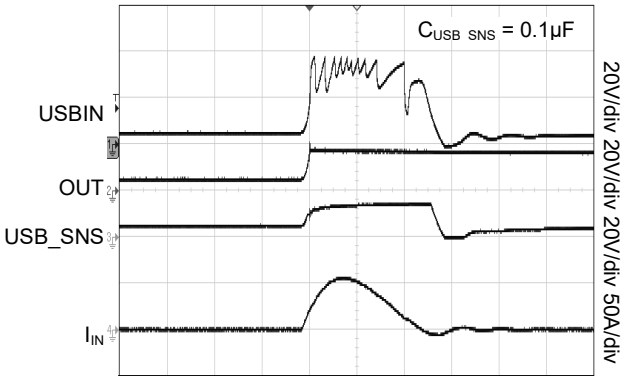
Time (20ms/div)

IN-GND 130V Off-State Surge Discharge Waveform



Time (10μs/div)

IN-GND 130V On-State Surge Discharge Waveform

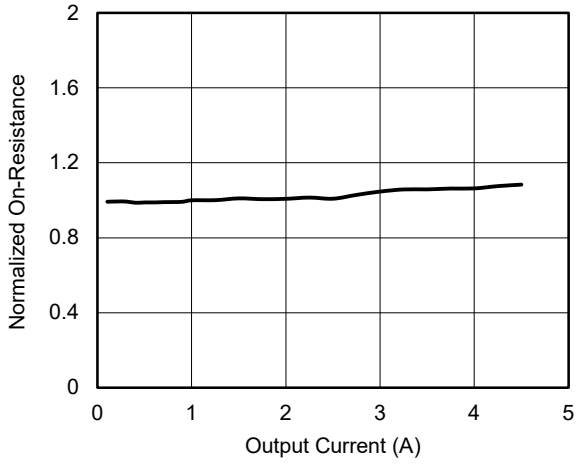


Time (10μs/div)

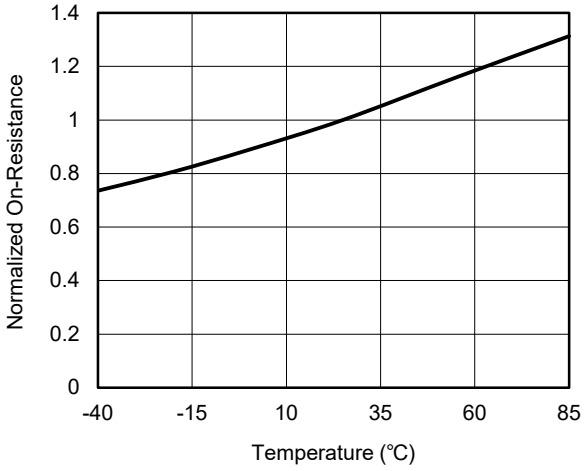
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, C_{USBIN} = 1μF, C_{OUT} = 10μF, C_{USB_SNS} = 1μF, unless otherwise noted.

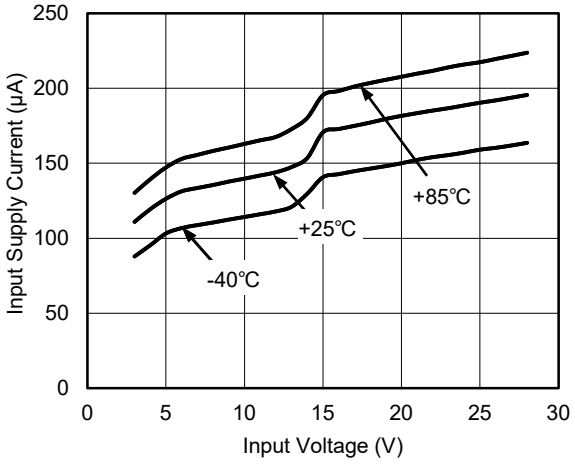
Normalized On-Resistance vs. Output Current



Normalized On-Resistance vs. Temperature



Input Supply Current vs. Input Voltage



TYPICAL APPLICATIONS

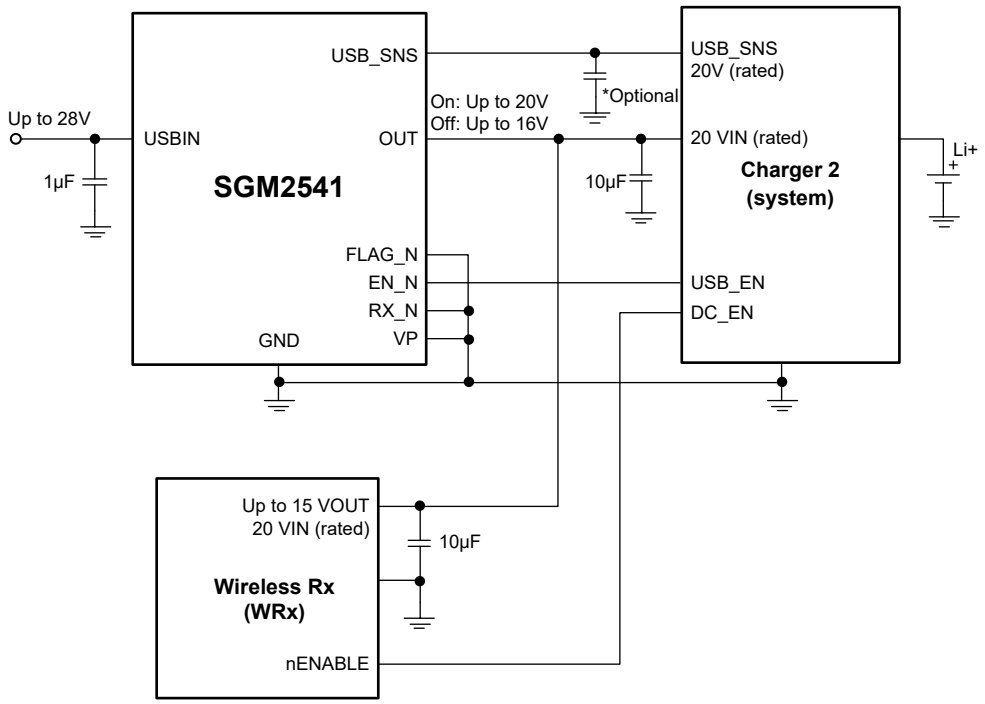


Figure 2. Typical Application, Slave Configuration

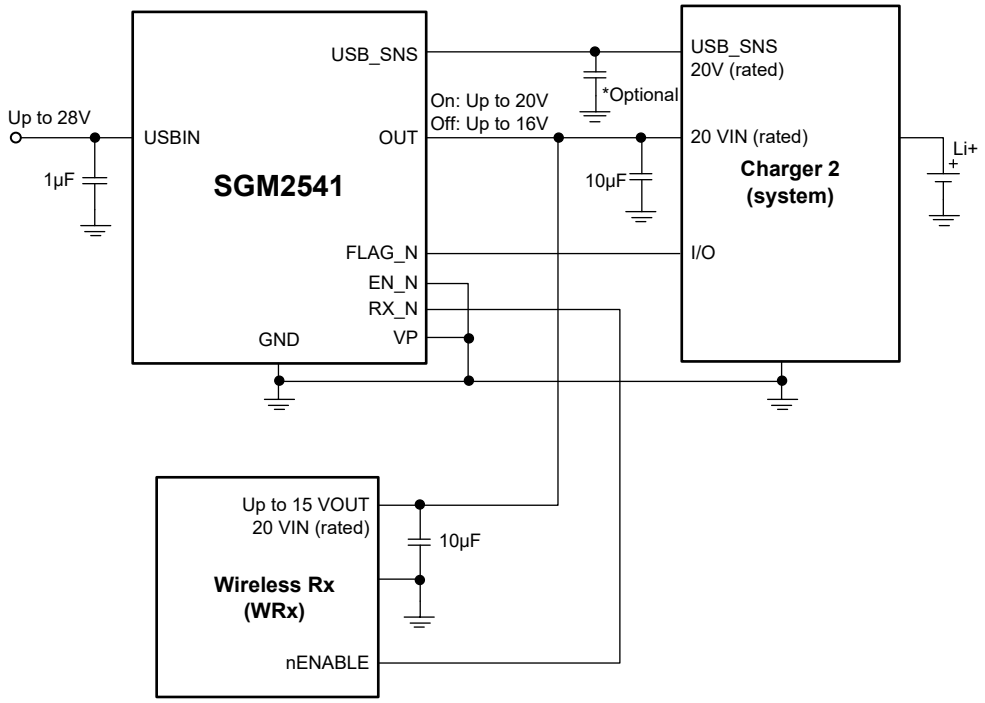


Figure 3. Typical Application, Autonomous Configuration

OPERATION

The SGM2541 bidirectional load switch is designed for systems or chargers with high voltage quick charge capability and wireless charging capability. The addition of a wireless Rx with an enable/disable pin allows the load switch to implement an equivalent 2:1 power multiplexer (PMUX) as shown in Figure 2. When disabled, the wireless Rx withstand voltage must be greater than or equal to 20V, the load switch's maximum output operating voltage.

PMUX Operating Modes

The 2:1 PMUX can operate in slave or autonomous modes. Slave mode allows the charger (system) to act as a master and determine the input priority, while autonomous mode assigns the input priority to the USBIN power source over the wireless Rx.

Both slave and autonomous modes include a 50ms input debounce delay and a soft-start time in rush periods. Autonomous mode includes a 50ms automatic break-before-make plus discharge period that is disabled in slave mode by grounding the RX_N pin.

Slave Mode

In slave mode, the charger (system) acts as the master, disables the wireless Rx, and activates the load switch on-state via the EN_N pin. The slave mode allows the system (charger) to assign the priority of the input power source when both power sources are active.

In OTG slave mode, a low input voltage threshold is detected at the USB_SNS pin. Toggling EN_N pin to low triggers OTG mode, the wireless Rx may be enabled by the charger (system) as follows: the system (charger) that controls OTG concurrent mode requires that the master enables the boost and/or wireless Rx. OTG mode is triggered when the master detects that the necessary conditions are met.

NOTE: Both the FLAG_N and the RX_N pins are tied to GND in slave mode. OTG concurrent mode requires slave mode.

Autonomous Mode

In autonomous mode, the load switch controls input/ wireless priority. The load switch controller disables the wireless Rx and activates the load switch ON-state after a fixed time delay when a valid USB_SNS voltage is detected. Autonomous mode gives priority to the USBIN input.

The system interfaces with valid USBIN or OUT, when a low input voltage threshold is detected at USBIN pin, it enters the OTG autonomous mode. Toggling FLAG_N pin to low triggers OTG mode since EN_N pin is tied to ground, disables the wireless Rx after RX_N pin is tied to high. See Figure 4 below.

NOTE: The EN_N pin is tied to ground in autonomous mode.

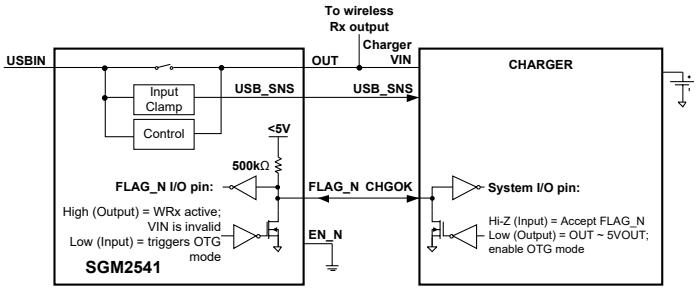
FLAG_N Logic in Autonomous Mode

The FLAG_N pin is a bidirectional input/output pin that controls the transition to and from OTG modes while in autonomous mode.

When USBIN pin is disconnected (floating) and a valid OUT voltage is detected, the FLAG_N pin serves as an output signal and FLAG_N = logic high. Subsequently, the load switch can be activated by toggling the FLAG_N = logic low, which triggers the OTG mode by transition into the on-state.

- After FLAG_N = logic low, OTG mode is triggered after logic turn-on delay, plus a soft-start time.

Ignore FLAG_N = logic low if the load switch is in the fault/OVP states.



USB_SNS	OUT	FLAG_N	CHGOK	LOAD SWITCH BEHAVIOR (EN_N = HIGH)
< UVLO	> UVLO	High	Hi-Z	Load switch = off, and OTG mode can be enabled. The on/off-state of WRx is determined by the SMB charger.
= UVLO	= VOUT	Low	Low	Load switch = on, and OTG mode is enabled. The on/off-state of WRx is determined by the SMB charger.
> UVLO	Low	Low	X	Load switch = on (EN_N = high), and OTG mode is not allowed.

Figure 4. FLAG_N Block Diagram and Functionality

OPERATION (continued)

Input OVP and Reverse Current Blocking

In the off-state (non-conducting), the load switch USBIN to ground withstand voltage is at least 28V DC with a reverse blocking voltage of at least 16V DC. In the on-state (conducting), the load switch maximum V_{USBIN}/V_{OUT} to ground operating voltage is at least 20V DC.

Soft-Start

Bidirectional peak current limiting is provided with a soft-start that occurs during load switch activation. In slave mode, soft-start occurs when a valid EN_N pin is toggled and after the debounce delay is satisfied. In autonomous mode, soft-start occurs when a valid FLAG_N pin is toggled and after the debounce delay and break-before-make plus discharge delay is satisfied.

Input Surge Protection

The device must withstand up to 130V surge voltage applied from the USBIN pin to ground pins. The surge may be applied to the load switch in the on/off-state. The surge waveform is compatible with the IEC 61000-4-5 specification, R_{SOURCE} = 2.0Ω, 1.2/50μs waveform.

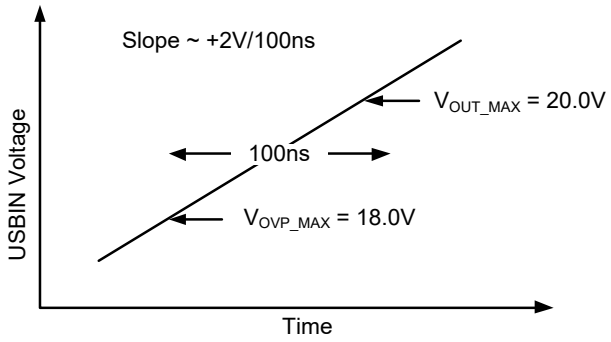


Figure 5. Surge Voltage Waveform with C_{USBIN} = 1μF Capacitive Loading

OTG Modes

OTG modes occur after the charger detects an OTG plug-in event, ~5V is applied to the OUT pin, and the USBIN pin is tied to an OTG load. The USB_SNS and EN_N pins are used in slave mode, while the FLAG_N pin is used in autonomous mode as shown in Figure 6.

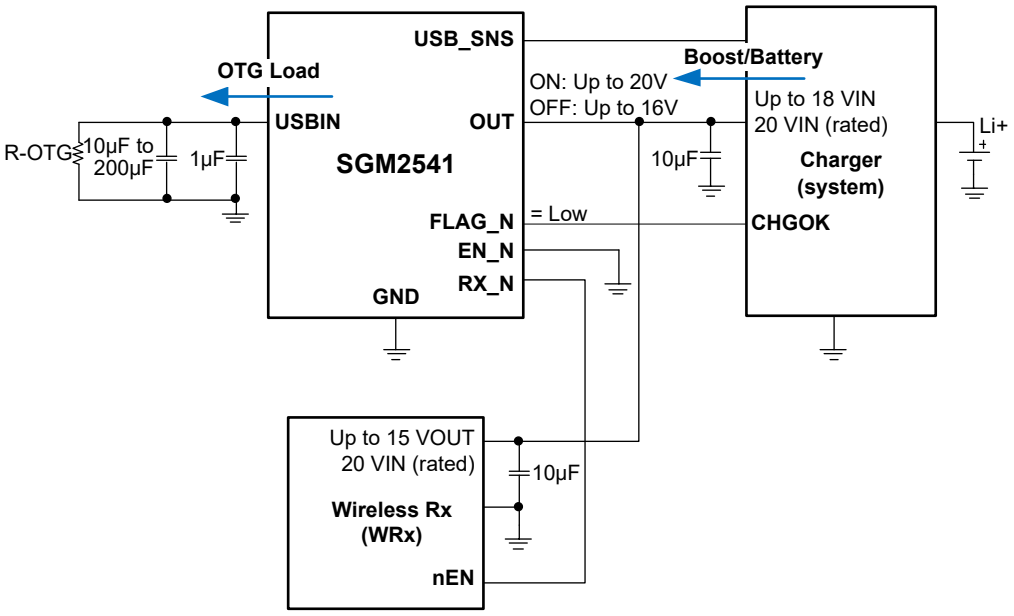


Figure 6. OTG Mode (R-OTG Load Applied to USBIN, Autonomous Mode)

OPERATION (continued)

OTG mode must support C_{USBIN} = 1μF (static), plus C_{OTG} = 200μF that can occur during a hot plug event; see Figure 7.

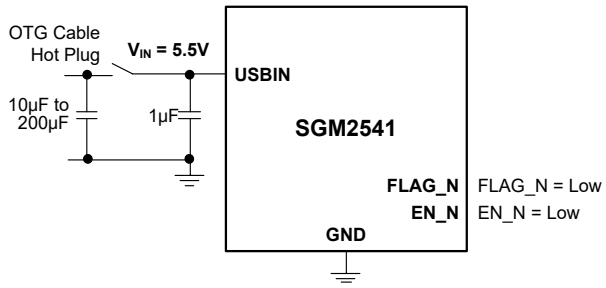


Figure 7. OTG Cable Capacitive Hot Plug Event (C-Load Applied)

Debounce Period

The valid USBIN detection occurs after a 50ms input debounce period. There is no OUT debounce.

Turn-On Delay and Discharge

In autonomous mode, the USBIN 50ms debounce period is followed by a 50ms break-before-make delay that allows time to disable the device while discharging the wireless Rx output. The break-before-make delay is also triggered in autonomous mode when RX_N = high. These delays are followed by a soft-start to limit peak inrush currents.

A 10mA (or 500kΩ) pull-down at OUT is active during the 50ms break-before-make delay, ensuring that no voltage appears at the output when the on-state is activated.

The break-before-make delay is inactive when the V_{USBIN} is removed because UVLO is active and the load switch is not powered; see Figure 9.

Timing Diagrams

Figure 8 to Figure 11 show slave and autonomous mode timing diagrams.

In slave mode, the on/off-state of the load switch is determined by the EN_N logic input pin that is tied to the system logic. A soft-start delay is applied when the EN_N pin is toggled low, and the USBIN 50ms debounce period has expired.

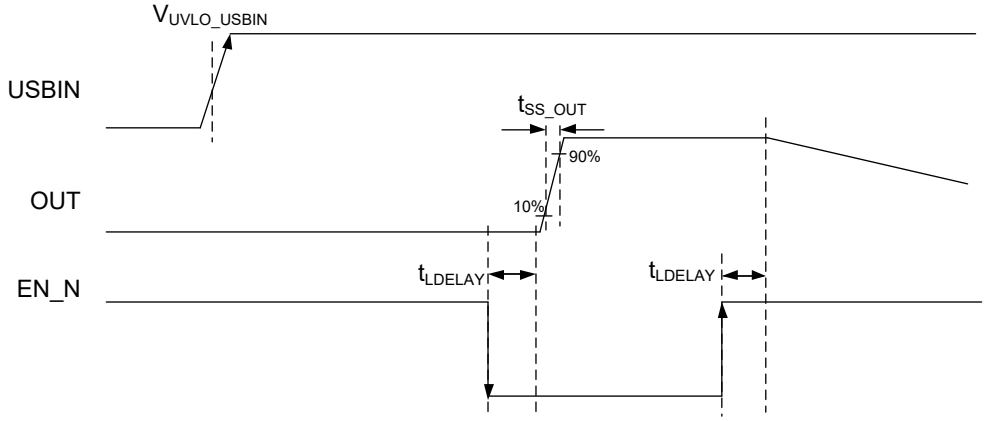


Figure 8. Slave Configuration. Application of V_{USBIN} with System Turned Off, Enabling, Disabling

OPERATION (continued)

In autonomous mode, a 50ms debounce delay, a 50ms break-before-make/discharge period and a soft-start delay are applied when the USB_SNS input rising threshold is detected. The FLAG_N pin provides the USBIN voltage status prior to entering OTG mode. The discharge feature is enabled during the 50ms break-before-make period.

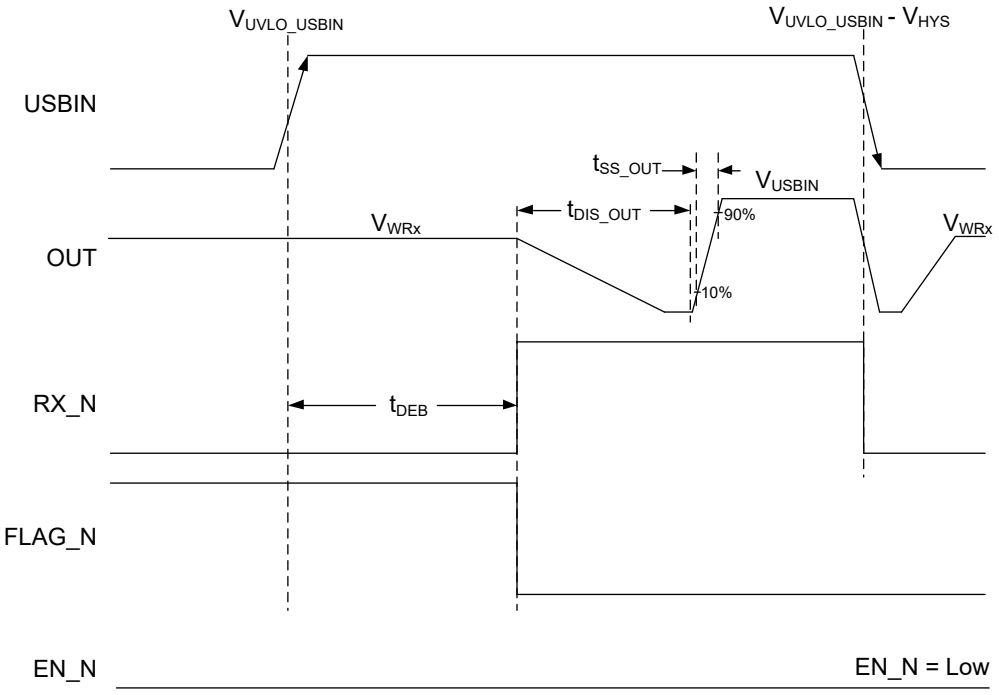


Figure 9. Autonomous Configuration. Application of V_{USBIN} with V_{OUT} Present, Removal of V_{USBIN}

OPERATION (continued)

In OTG modes, a load is applied to the USBIN and current flows from OUT to USBIN.

In slave mode, OTG occurs when a valid OUT voltage is applied, no voltage is detected at the USB_SNS and the logic turn-on delay time is satisfied. OTG mode is triggered by pulling the EN_N pin low, as shown in Figure 10.

In autonomous mode, the FLAG_N is a logic output and toggles high to indicate USBIN invalid, and OTG can be enabled immediately. The FLAG_N pin is bidirectional, and autonomous OTG mode is triggered by pulling the FLAG_N input pin low, which triggers a soft-start.

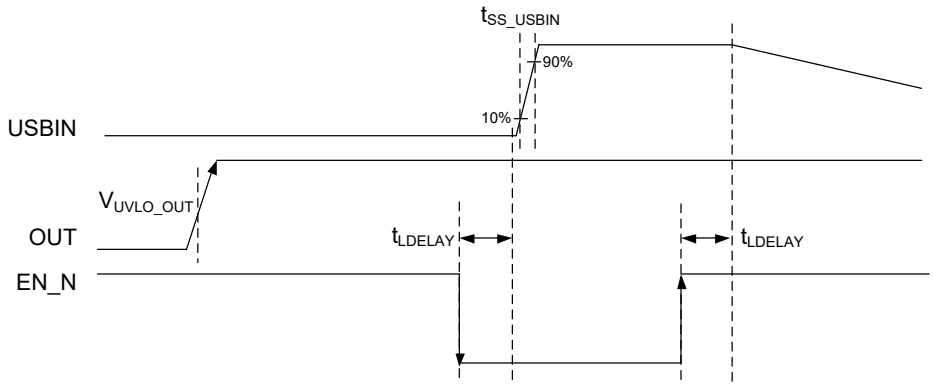


Figure 10. Slave Configuration. Application of V_{OUT}, Enabling (OTG), Disabling

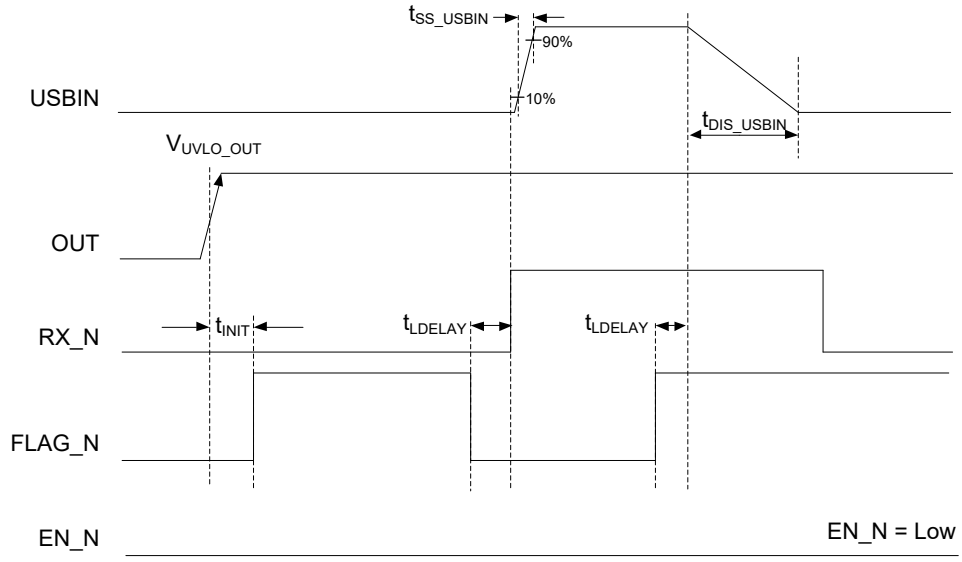


Figure 11. Autonomous Configuration. Application of V_{OUT}, Enabling (OTG), Disabling

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

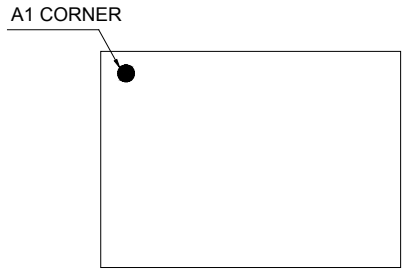
FEBRUARY 2019 – REV.A.1 to REV.A.2	Page
Updated Absolute Maximum Ratings section	2
Changed Electrical Characteristics section	4

SEPTEMBER 2018 – REV.A to REV.A.1	Page
Changed Electrical Characteristics section	4, 5

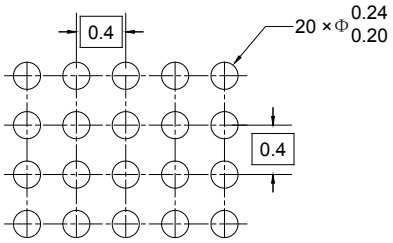
Changes from Original (JUNE 2018) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

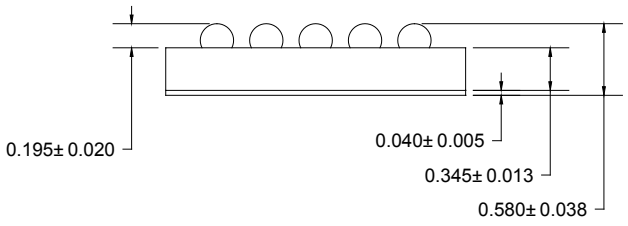
WLCSP-2.43×1.75-20B



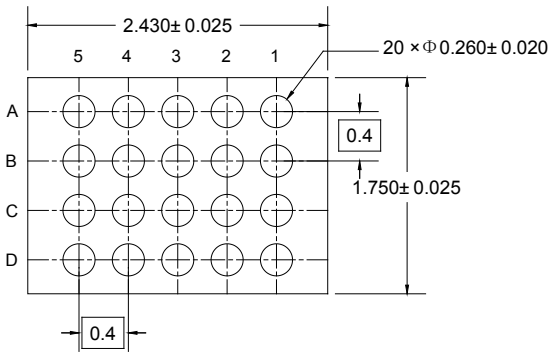
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

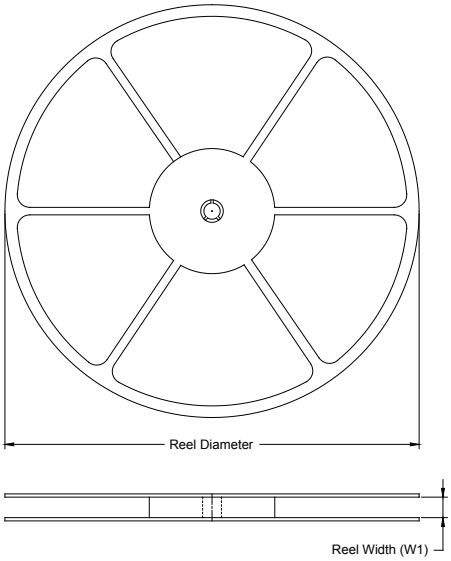


BOTTOM VIEW

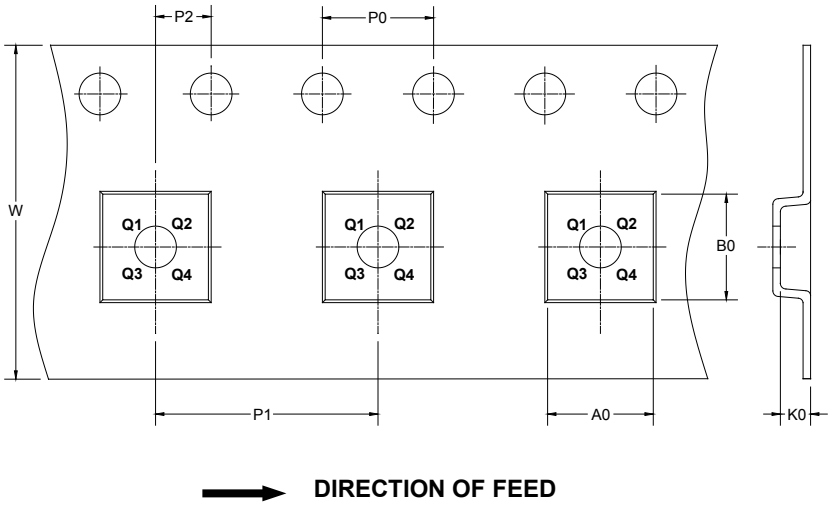
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



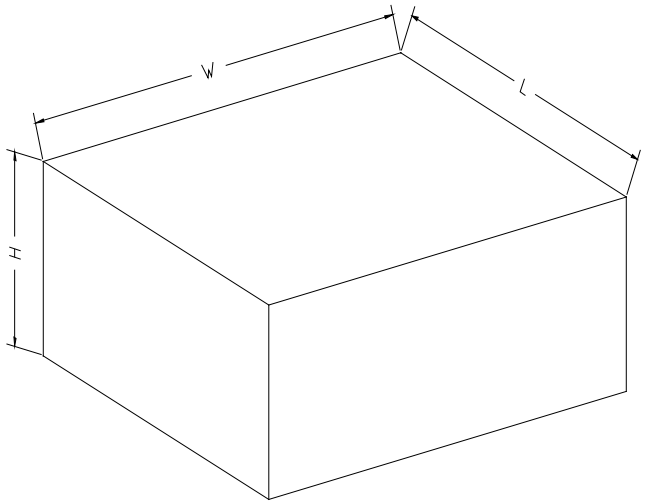
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.43×1.75-20B	7″	9.2	1.90	2.71	0.81	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002