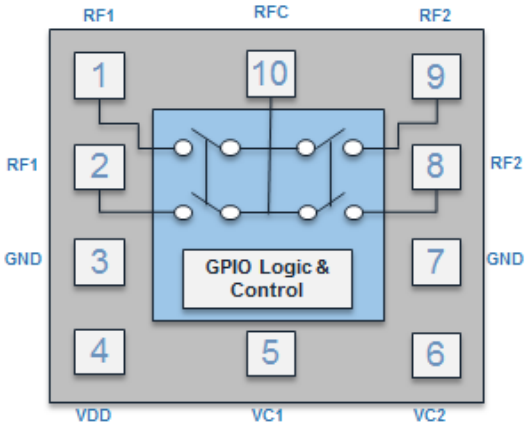
RF1694B

Single Pole Double Throw Switch

The RF1694B is very low loss SPDT specifically designed for high performance antenna tuning applications. All RF path performance is enhanced with ultra-low on state resistance and off state capacitance. RF1694B allows the creation of advanced tuning topologies to maximize TRP & TIS performance in space constrained applications.



Functional Block Diagram

Package: Laminate Package
10-pin, 1.1mm x 1.5mm x 0.44mm

Features

- Ultra-Low On-resistance, 0.6Ω
- Very Linear Performance, 75dBm IP3
- Off Ports, 'Open Type'
- Two pin GPIO control Interface for standard SP4T operation
- Very Small 1.1mm x 1.5mm, Laminate Package
- Very low profile, 0.44mm
- 2.4V to 5.8V Supply Range (V_{BATT} Connect)

Applications

- Antenna Tuning
- Band Switching
- Impedance Tuning

Ordering Information

RF1694BSB	5-pc Sample Bag
RF1694BSR	100-pc 7" Reel
RF1694BTR13-5K	5000-pc, 13" Tape and Reel
RF1694BPCK-410	Fully Assembled EVB

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS20160119

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage, V_{DD}	+6.0	V
Control Voltage, V_{CTL}	+3.3	V
Max voltage between any combination of RF ports or ground V_{RF}, V_{DD} = 2.85VDC, $V_{CTL1/2}$=0/1.8VDC, Temp=25C	36	V_P
Operating Case Temperature	-30 to +90	°C
Storage Temperature	-55 to +150	°C
ESD All Pins, HBM, JESD22-A114	2.0	kV

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Electrical Specifications: Temp = 25°C, 50Ω, Active Mode. V_{DD} = 2.85V, CTL = 0/+1.8V.
Operating Frequency	700		2700	MHz	
Supply Voltage V_{DD}	2.4	2.85	5.8	V	
Supply Current I_{DD}		50		µA	
Control Voltage High V_{CTL1}, V_{CTL2}	1.3	1.8	2.7	V	
Control Voltage Low V_{CTL1}, V_{CTL2}	0		0.45	V	
Control Current I_{CTL}		0.1		µA	V_{CTL} = 1.8V

Electrical Specifications

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Electrical Specifications: Temp = 25°C, 50Ω, Active Mode. V_{DD} = 2.85V, CTL = 0/+1.8V.
Insertion Loss (RFC to RF1 & RF2) LS2 & LS3		0.15	0.30	dB	700 – 915 MHz
		0.25	0.60	dB	915 – 1910 MHz
		0.50	0.85	dB	1910 – 2700 MHz
Isolation (RFC to RF1 & RF2) LS2 & LS3		23		dB	700 – 915 MHz
		20		dB	915 – 1910 MHz
		15		dB	1910 – 2700 MHz
Isolation (RFC to RF1 & RF2) LS4, All Off Mode		17		dB	700 – 915 MHz
		13		dB	915 – 1910 MHz
		11		dB	1910 – 2700 MHz
Return Loss		22		dB	915 MHz
		16		dB	1910 MHz

Electrical Specifications

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Electrical Specifications: Temp = 25°C, 50Ω, Active Mode. V_{DD} = 2.85V, CTL = 0/+1.8V.
R_{ON} (RFC to RF1/RF2)		0.6		Ω	100MHz
Start Up Time		9		µs	10% VDD ramp up to 90% of final RF amplitude
ON switching speed		5		µs	90% of final RF amplitude
OFF Switching Speed		5		µs	90% of final RF amplitude
Second Harmonics		-80		dBm	700 MHz, Pin = 23 dBm
Third Harmonics		-92		dBm	
Second Harmonics		-55		dBm	915 MHz, Pin = 35 dBm
Third Harmonics		-65		dBm	
Second Harmonics		-55		dBm	1910 MHz, Pin = 33 dBm
Third Harmonics		-65		dBm	
Second Harmonics		-65		dBm	2570 MHz, Pin = 23 dBm
Third Harmonics		-75		dBm	
IIP2, Low		115		dBm	Refer to IIP2 conditions table
IIP2, High		115		dBm	Refer to IIP2 conditions table
IIP3, Cell		75		dBm	Refer to IIP3 conditions table
IIP3, IMT		72		dBm	Refer to IIP3 conditions table
SVE-LTE Test 1		75		dBm	Refer to IIP3 conditions table
SVE-LTE Test 2		80		dBm	Refer to IIP3 conditions table
Receive Spurious 700 – 2700 MHz		-117		dBm	No RF Signal
		-112		dBm	RF – 915 MHz at 35dBm
		-112		dBm	RF – 1910 MHz at 33dBm

Control Logic

Logic State	Mode	CTL1	CTL2	State Description	RF Applied
1	Low Power	V_{LOW}	V_{LOW}	Low Power Mode	No
2	Active	V_{LOW}	V_{HIGH_CTL}	RFC to RF2 ON	Yes
3	Active	V_{HIGH_CTL}	V_{LOW}	RFC to RF1 ON	Yes
4	Active	V_{HIGH_CTL}	V_{HIGH_CTL}	All Off Mode	Yes

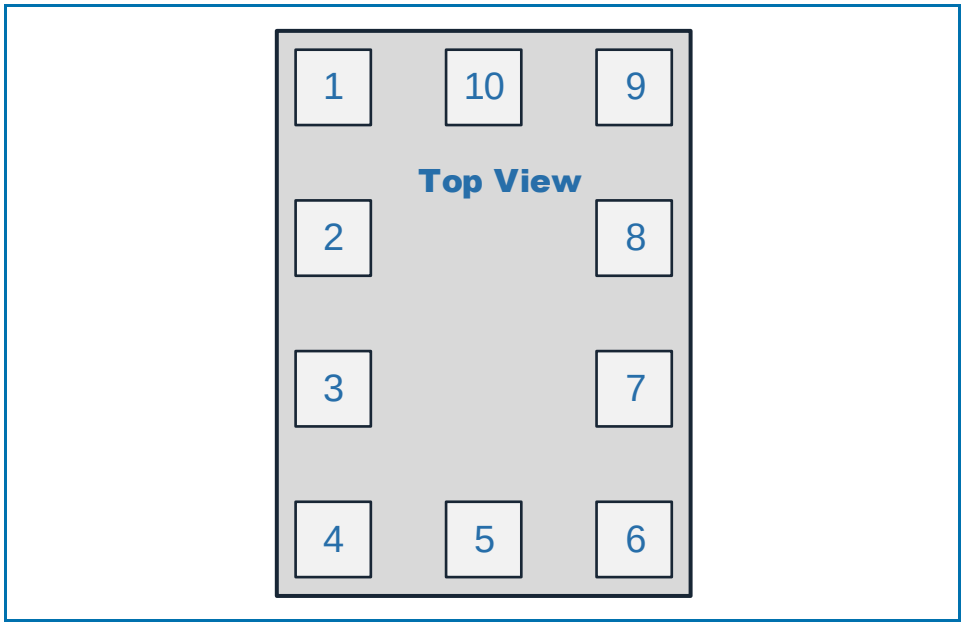
IIP2 Test Conditions

Band	In-band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band I Low (IMT)	2140	1950	+20	190	-15
Band I High (IMT)	2140	1950	+26	4090	-20
Band II Low (PCS)	1960	1880	+20	80	-15
Band II High (PCS)	1960	1880	+26	3840	-20
Band V Low (Cell)	881.5	836.5	+20	45	-15
Band V High (Cell)	881.5	836.5	+26	1718	-20
Band VIII Low	942.5	897.5	+20	45	-15
Band VIII High	942.5	897.5	+26	1840	-20

IIP3 Test Conditions

Band	In-band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band I High (IMT)	2140	1950	+20	1760	-15
Band V High (Cell)	881.5	836.5	+20	791.5	-15
SVE LTE Test 1	747	825	+14	786	+23
SVE LTE Test 2	872	827	+23	782	+14

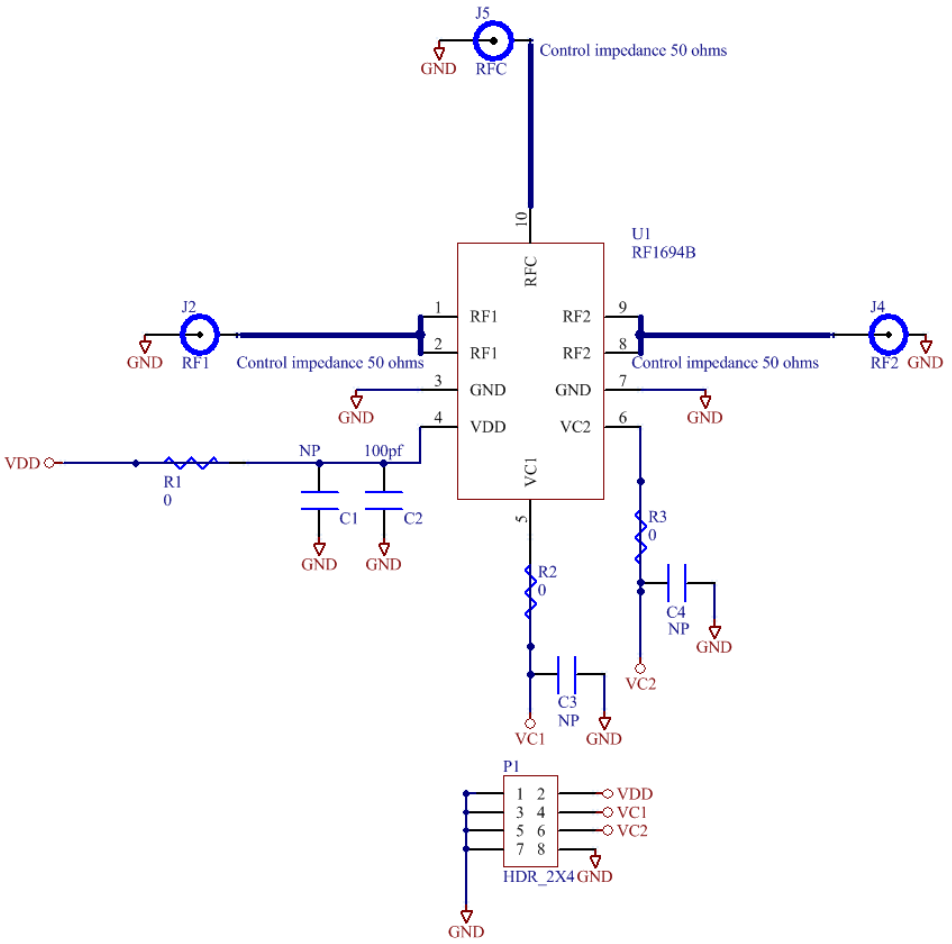
Pin Out



Pin Names and Descriptions

Pin	Name	Details
1	RF1	RF port 1.
2	RF1	RF port 1.
3	GND	Ground.
4	VDD	Voltage Supply.
5	CTL1	Control Voltage 1.
6	CTL2	Control Voltage 2.
7	GND	Ground.
8	RF2	RF port 2.
9	RF2	RF port 2.
10	RFC	RF Common port.

Evaluation Board Schematic

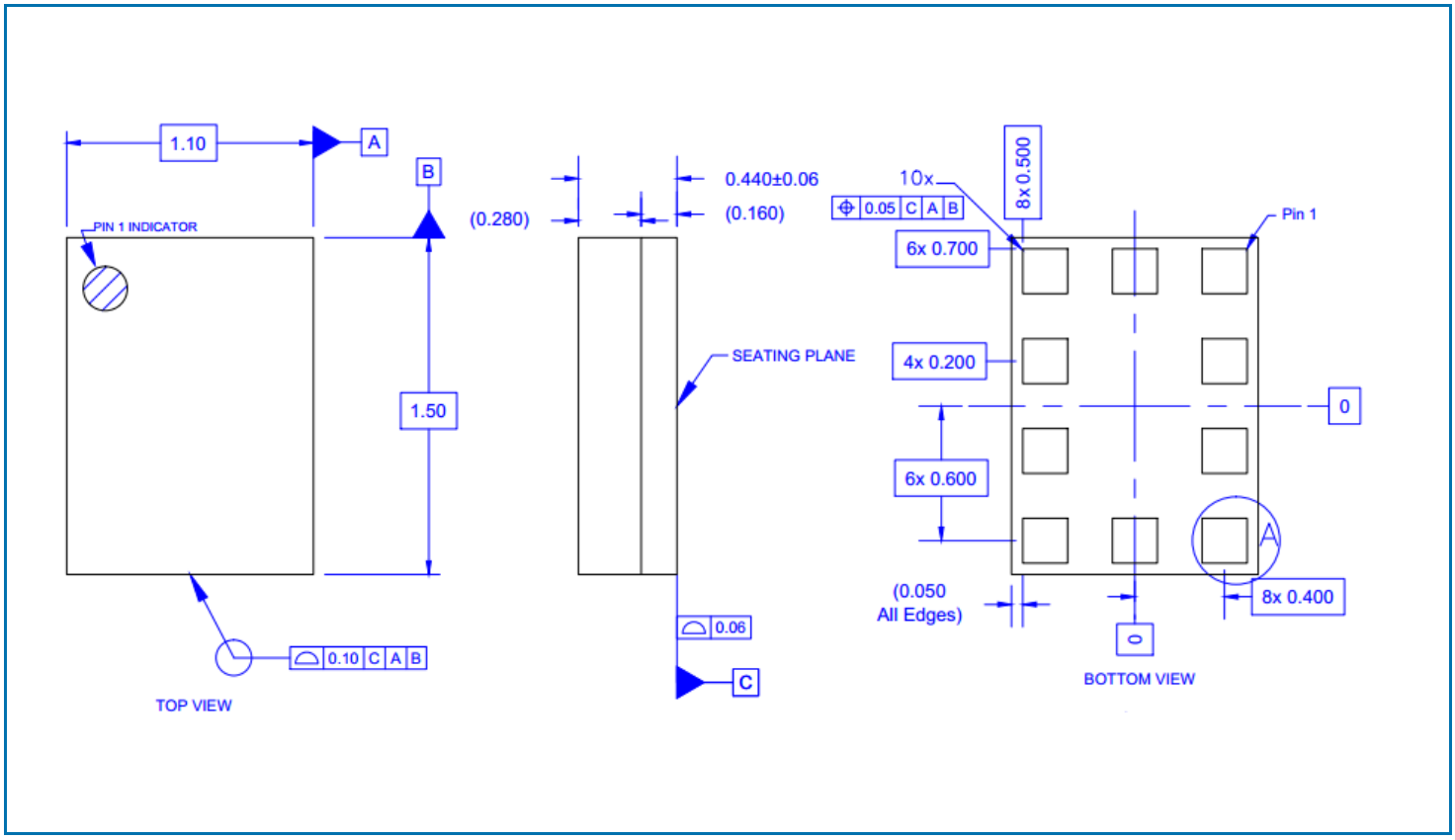


1) Pins 1 and 2 are shorted together on the evaluation board and must be done at the board level in an application to meet specifications (i.e. Ron = 0.6Ω).

2) Pins 8 and 9 are shorted together on the evaluation board and must be done at the board level in an application to meet specifications (i.e. Ron = 0.6Ω).

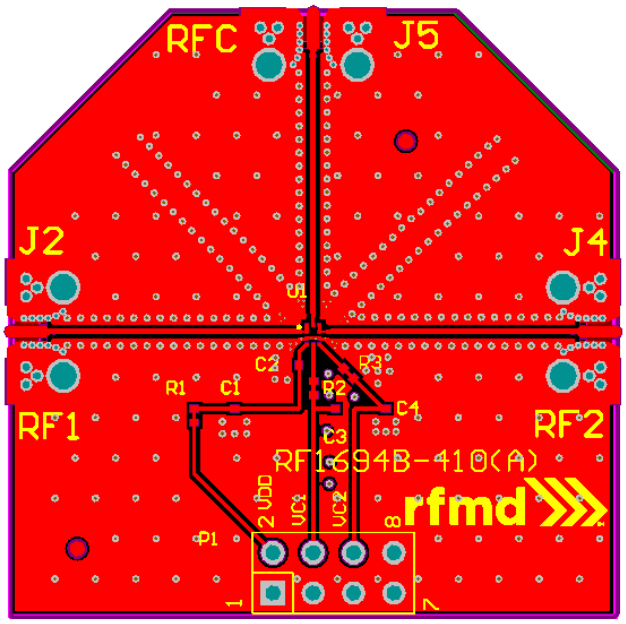
Part Number	Part	Part Description
U1	RF1694B	RF1694B, SPDT Switch
J2, J4 & J5	SMA connector	Edge mount 0.068” SMA connector
C2	100 pF capacitor	(0402) 100 pF de-coupling capacitor
C1, C3 & C4	NP	Not populated.
R1, R2 & R3	NP	Not populated.
P1	2X4 RA header	2X4 right angled header with 0.1” spacing

Package Outline and Branding Drawing (Dimensions in millimeters)

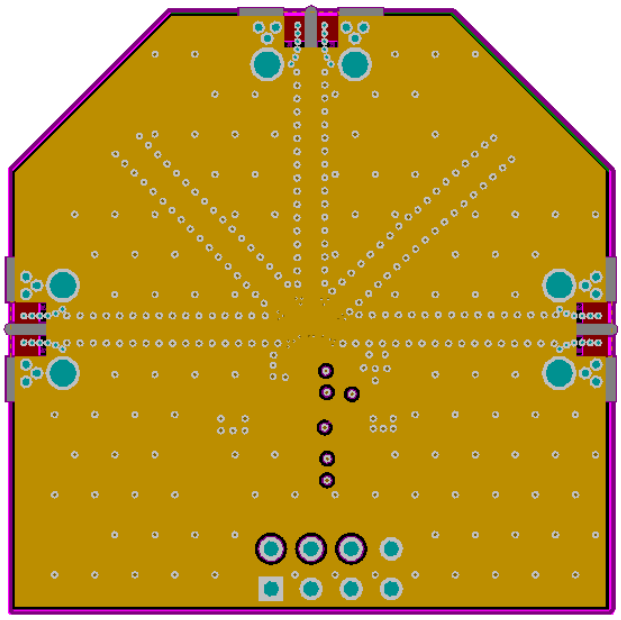


Evaluation Board Layout

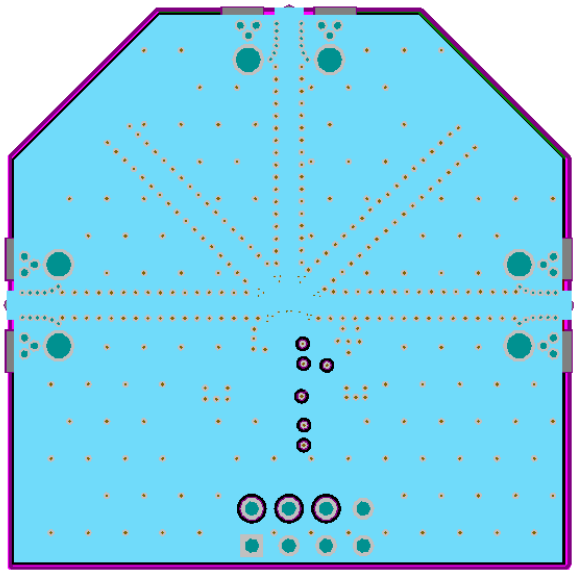
Top – Layer 1



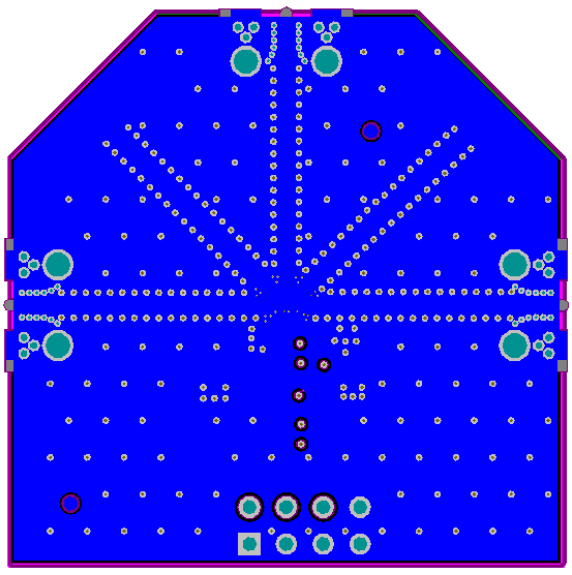
Layer 2



Layer 3

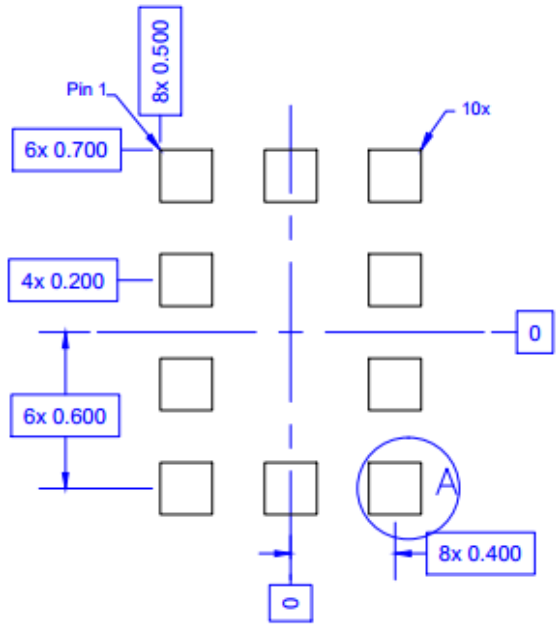


Bottom – Layer 4



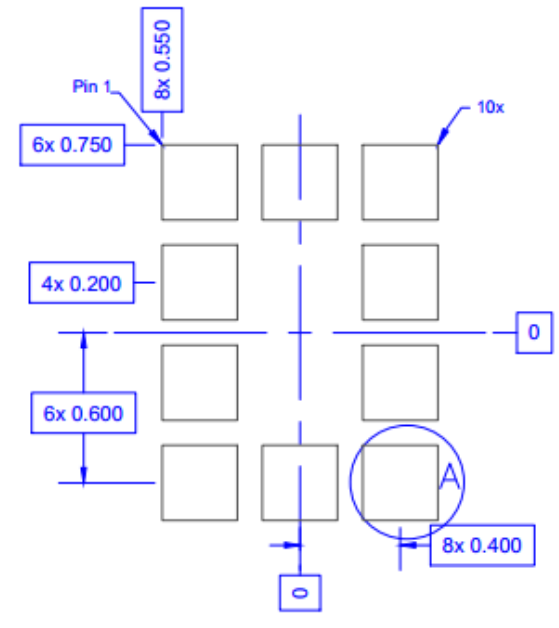
PCB Design Requirements

PCB Metal Land Pattern



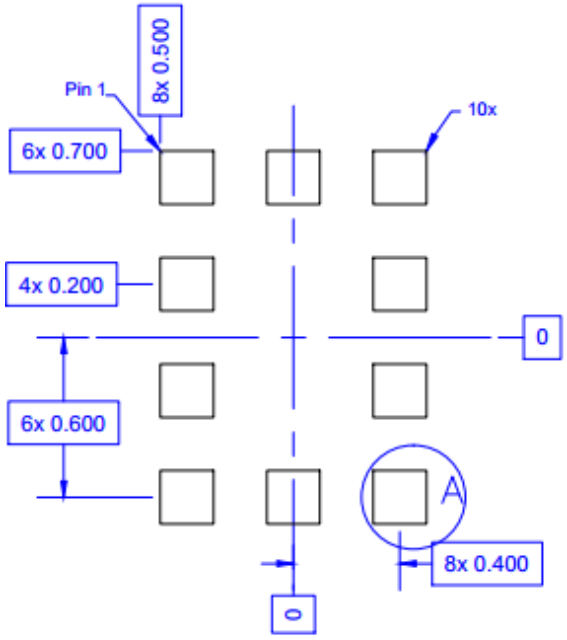
PCB METAL TOP VIEW

PCB Soldermask Pattern



SOLDER MASK PATTERN TOP VIEW

PCB Stencil Pattern



STENCIL PATTERN TOP VIEW

Timing Diagram

Power ON and OFF sequence

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signals CTL1 and CTL2 should be set to 0V unless V_{DD} is set in the operating voltage range.

Power ON –

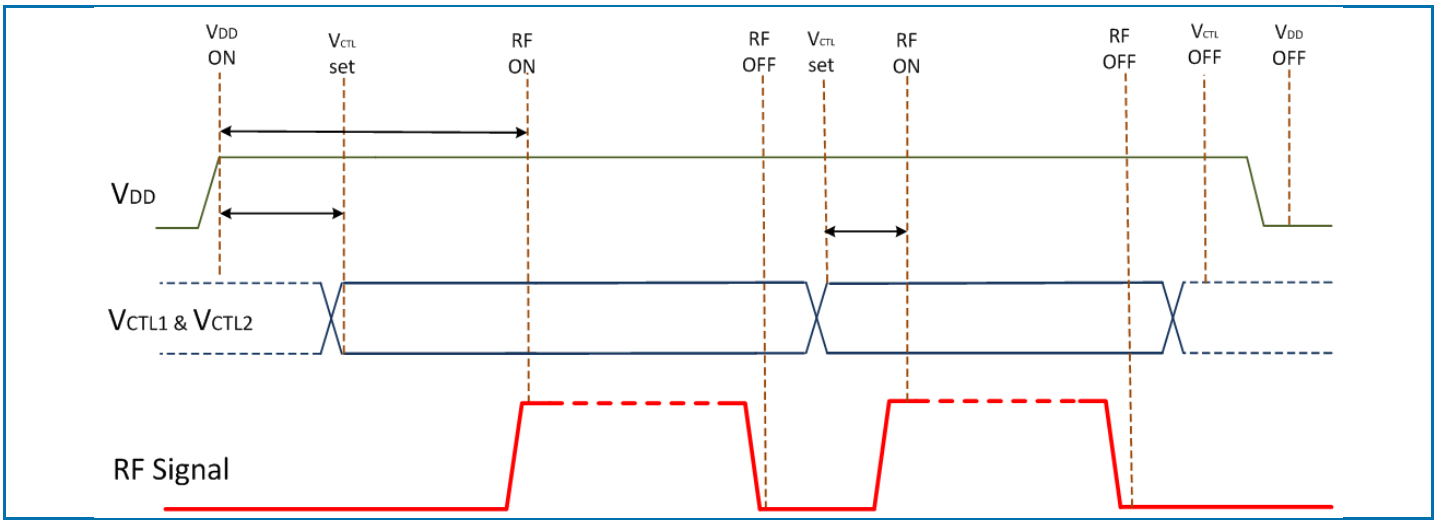
1) Apply voltage supply - V_{DD}
2) Set Controls - V_{CTL1} & V_{CTL2}
3) Wait 20µs or greater and then apply RF

Change switch position from one RF port to another –

1) Remove RF
2) Change control voltages V_{CTL1} & V_{CTL2} to set the switch to desired RF port
4) Wait 5µs or greater and then apply RF

Power OFF –

1) Remove RF
2) Remove control voltages - V_{CTL1} & V_{CTL2}
3) Remove V_{DD}



Revision History

Revision Code	Comments
DS20141013	First Draft
DS20141203	Updated Electrical Specifications Chart and included some of the TBD items
DS20141204	Minor correction to Z-height on page 1 and application note addition on page 7.
DS20141208	Minor formatting corrections.
DS20150318	Updating of Electrical specifications tables and formatting corrections.
DS20150326	Updated Ordering Info
DS20150911	Updated Abs Max Table information
DS20160119	Added Insertion Loss Max Limits