QM11024

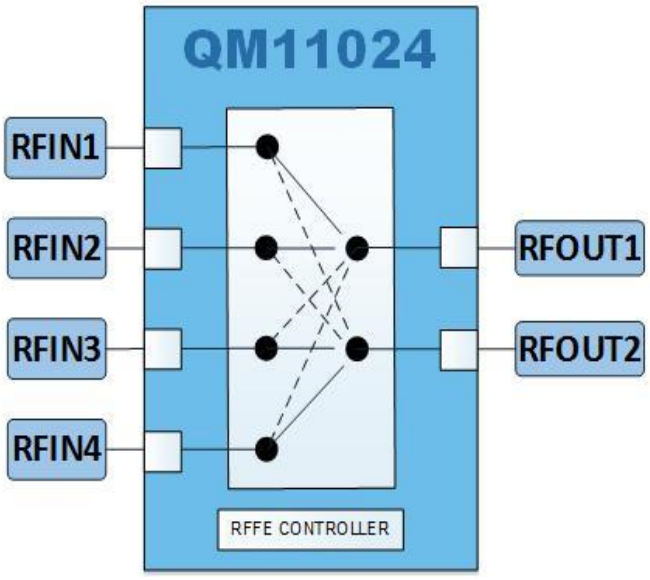
BROADBAND HIGH LINEARITY DP4T ROUTING SWITCH

Product Overview

The QM11024 is a low loss, high linearity dual-pole four-throw addressable switch with performance optimized for transfer routing applications. The QM11024 integrates a serial control system compatible with the RFFE standard. The select lines (SID) provide USID addressability and up to two placements of the QM11024 on the same RFFE Bus. The QM11024 runs off a single VIO voltage supply and is packaged in a 16 pin compact 2.0mm x 2.0mm x 0.5mm size device.This offers mobile handset designers a compact, easy-to-use, switch component for quick integration into multimode, multi-band systems.

16 Pin 2.0 x 2.0 X 0.5 mm³ Module

Functional Block Diagram



Key Features

- Excellent Insertion Loss and Isolation performance
- High Linearity
- RFFE 2.1 Control Interface
  - UDR Mask write capable (R/WM)
- Broadband Performance Suitable for Multiple Air Interfaces including 5G applications.
- Slave ID for Multiple Placements on the Same Board
- Very Low Current Consumption
- DC blocking capacitors are not required in typical applications
- Single VIO supply

Applications

- Cellular Handset Applications
- Cellular Modems and USB Devices
- Multi-Mode GSM, CDMA, WCDMA,LTE and NR including n77, n79 frequency bands.

Ordering Information

Part Number	Description
QM11024DK	Design Kit
QM11024SB	Sample Bag with 5 pcs
QM11024SR	Sample Reel with 100 pcs
QM11024TR13	Standard 13” Reel with 10,000 pcs

Absolute Maximum Ratings

Parameter	Conditions	Rating
Storage Temperature		-40 to +125 °C
Operating Temperature		-30 to +90°C
V_{IO}, SDATA, SCLK, & SID		2.15 V
Absolute Max Power	All ports 10:1 VSWR, +25°C	38dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
V_{IO} Interface Supply Voltage High	1.65	1.8	1.95	V
V_{IO} Interface Supply Voltage Low	0	0	0.45	V
SDATA, SCLK – Voltage High	0.8 x V_{IO}	1.8	V_{IO}	V
SDATA, SCLK – Voltage Low	0.00	0.00	0.2 x V_{IO}	V
Switching Time -- Switch RF path from 10% to 90% (see Figure.2/3)		3	4	µs

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C,

V_{IO}/SDATA/SCLK/SID = 1.8 V / 0 V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RFOUT1/2-RFIN1/2/3/4	617 MHz to 960 MHz		0.4		dB
RFOUT1/2-RFIN1/2/3/4	1425 MHz to 2200 MHz		0.5		dB
RFOUT1/2-RFIN1/2/3/4	2300 MHz to 2690 MHz		0.65		dB
RFOUT1/2-RFIN1/2/3/4	3300 MHz to 3800 MHz		0.8		dB
RFOUT1/2-RFIN1/2/3/4	3800 MHz to 5000 MHz*		0.9		dB
Isolation**					
Active RFIN1/2/3/4 to RFOUT1, measure RFIN1/2/3/4 to RFOUT2	617 MHz to 960 MHz		40		dB
	1427 MHz to 2200 MHz		35		dB
	2300 MHz to 2690 MHz		35		dB
Active RFIN1/2/3/4 to RFOUT2 , measure RFIN1/2/3/4 to RFOUT1	3300 MHz to 3800 MHz		30		dB
	3800 MHz to 5000 MHz		30		dB
Harmonics					
2nd Harmonic	Freq = 824 MHz to 915 MHz ; P_{IN} = 36dBm		-50		dBm
3rd Harmonic			-50		dBm
2nd Harmonic	Freq = 1710 MHz to 1785 MHz ; P_{IN} = 33dBm		-58		dBm
3rd Harmonic			-55		dBm
2nd Harmonic	Freq = 1850 MHz to 1910 MHz ; P_{IN} = 33dBm		-58		dBm
3rd Harmonic			-55		dBm
2nd Harmonic	Freq = 617 MHz to 960 MHz ; P_{IN} = 26dBm		-78		dBm
3rd Harmonic			-80		dBm
2nd Harmonic	Freq = 1427 MHz to 2200 MHz ; P_{IN} = 26dBm		-72		dBm
3rd Harmonic			-79		dBm
2nd Harmonic	Freq = 2300-2690MHz; P_{IN} = 26dBm		-70		dBm
3rd Harmonic			-80		dBm
2nd Harmonic	Freq = 3300 MHz to 3800 MHz ; P_{IN} = 26dBm		-65		dBm
3rd Harmonic			-80		dBm
2nd Harmonic	Freq = 3800 MHz to 5000 MHz ; P_{IN} = 26dBm***		-55		dBm
3rd Harmonic			-75		dBm
Linearity					
IIP2	f1=20dBm f2=-15dBm: f1=1950MHz f2=4090MHz		118	120	dBm
IIP3	f1=20dBm f2=-15dBm: f1=1950MHz f2=1760MHz		76	78	dBm
VSWR					
Input/Output VSWR	699 MHz to 960 MHz		1.2		:1

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
	1427 MHz to 2200 MHz		1.2		:1
	2300 MHz to 2690 MHz		1.4		:1
	3300 MHz to 3800 MHz		1.5		:1
	3800 MHz to 5000 MHz		2.0		:1

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS

Notes

* Insertion loss averaged over band. See separate application note for improvement of matching at 5GHz/6GHz and recommended ports.

** See Table 1

*** The performance between 3300MHz to 5000MHz is based on the use of RFOUT2 for optimum harmonic performance.

Isolation Frequency Range: 617MHz to 960MHz														
Active Path		Measured Port					Active Path		Measured Port					
	Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT2		Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT1	units
RFIN1 to RFOUT1 (RFOUT2 isolation)	RFIN1	x	40	62	61	44	RFIN1 to RFOUT2 (RFOUT1 isolation)	RFIN1	x	40	38	45	45	dB
	RFOUT1	x	40	63	61	43		RFOUT2	x	40	37	45	45	
RFIN2 to RFOUT1 (RFOUT2 isolation)	RFIN2	39	x	47	62	38	RFIN2 to RFOUT2 (RFOUT1 isolation)	RFIN2	53	x	38	37	47	
	RFOUT1	40	x	48	62	38		RFOUT2	53	x	38	37	46	
RFIN3 to RFOUT1 (RFOUT2 isolation)	RFIN3	51	46	x	40	36	RFIN3 to RFOUT2 (RFOUT1 isolation)	RFIN3	53	41	x	34	47	
	RFOUT1	50	46	x	41	37		RFOUT2	52	41	x	34	46	
RFIN4 to RFOUT1 (RFOUT2 isolation)	RFIN4	51	57	40	x	38	RFIN4 to RFOUT2 (RFOUT1 isolation)	RFIN4	35	41	45	x	43	
	RFOUT1	50	56	41	x	39		RFOUT2	35	39	45	x	43	

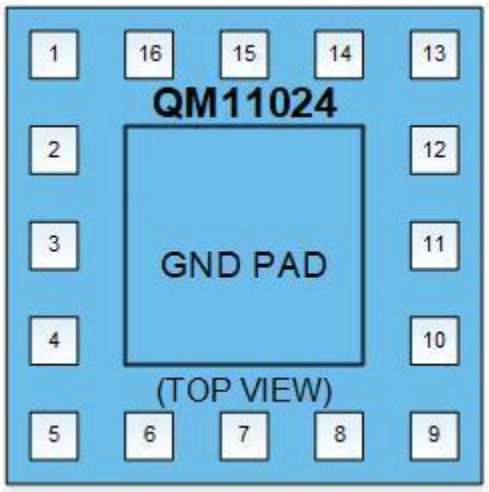
Isolation Frequency Range: 1425MHz to 2200MHz														
Active Path		Measured Port					Active Path		Measured Port					
	Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT2		Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT1	units
RFIN1 to RFOUT1 (RFOUT2 isolation)	RFIN1	x	34	54	55	37	RFIN1 to RFOUT2 (RFOUT1 isolation)	RFIN1	x	33	32	40	39	dB
	RFOUT1	x	33	57	55	37		RFOUT2	x	33	31	39	38	
RFIN2 to RFOUT1 (RFOUT2 isolation)	RFIN2	34	x	41	54	31	RFIN2 to RFOUT2 (RFOUT1 isolation)	RFIN2	47	x	32	31	40	
	RFOUT1	34	x	41	56	31		RFOUT2	46	x	31	31	39	
RFIN3 to RFOUT1 (RFOUT2 isolation)	RFIN3	45	41	x	34	30	RFIN3 to RFOUT2 (RFOUT1 isolation)	RFIN3	46	35	x	28	40	
	RFOUT1	45	41	x	34	30		RFOUT2	46	34	x	28	39	
RFIN4 to RFOUT1 (RFOUT2 isolation)	RFIN4	44	53	34	x	32	RFIN4 to RFOUT2 (RFOUT1 isolation)	RFIN4	28	34	39	x	36	
	RFOUT1	44	50	34	x	32		RFOUT2	28	33	39	x	35	

Isolation Frequency Range: 2300MHz to 2700MHz														
Active Path		Measured Port					Active Path		Measured Port					
	Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT2		Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT1	units
RFIN1 to RFOUT1 (RFOUT2 isolation)	RFIN1	x	31	50	53	35	RFIN1 to RFOUT2 (RFOUT1 isolation)	RFIN1	x	31	30	38	36	dB
	RFOUT1	x	31	57	54	34		RFOUT2	x	31	29	38	35	
RFIN2 to RFOUT1 (RFOUT2 isolation)	RFIN2	33	x	39	51	29	RFIN2 to RFOUT2 (RFOUT1 isolation)	RFIN2	45	x	30	30	38	
	RFOUT1	33	x	39	54	29		RFOUT2	44	x	29	30	37	
RFIN3 to RFOUT1 (RFOUT2 isolation)	RFIN3	44	39	x	31	28	RFIN3 to RFOUT2 (RFOUT1 isolation)	RFIN3	44	32	x	26	37	
	RFOUT1	42	40	x	31	27		RFOUT2	43	32	x	26	37	
RFIN4 to RFOUT1 (RFOUT2 isolation)	RFIN4	42	56	31	x	29	RFIN4 to RFOUT2 (RFOUT1 isolation)	RFIN4	26	32	37	x	33	
	RFOUT1	41	49	31	x	29		RFOUT2	26	32	37	x	32	

Isolation Frequency Range: 3300MHz to 3800MHz														
Active Path		Measured Port					Active Path		Measured Port					
	Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT2		Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT1	units
RFIN1 to RFOUT1 (RFOUT2 isolation)	RFIN1	x	29	44	48	32	RFIN1 to RFOUT2 (RFOUT1 isolation)	RFIN1	x	29	29	37	32	dB
	RFOUT1	x	29	53	54	31		RFOUT2	x	28	28	36	31	
RFIN2 to RFOUT1 (RFOUT2 isolation)	RFIN2	33	x	35	45	26	RFIN2 to RFOUT2 (RFOUT1 isolation)	RFIN2	43	x	29	29	35	
	RFOUT1	35	x	38	52	26		RFOUT2	43	x	28	29	34	
RFIN3 to RFOUT1 (RFOUT2 isolation)	RFIN3	41	37	x	28	25	RFIN3 to RFOUT2 (RFOUT1 isolation)	RFIN3	42	30	x	25	34	
	RFOUT1	37	41	x	28	25		RFOUT2	42	30	x	24	34	
RFIN4 to RFOUT1 (RFOUT2 isolation)	RFIN4	39	54	28	x	26	RFIN4 to RFOUT2 (RFOUT1 isolation)	RFIN4	24	30	36	x	29	
	RFOUT1	37	47	29	x	26		RFOUT2	24	30	35	x	29	

Isolation Frequency Range: 3800MHz to 500MHz														
Active Path		Measured Port					Active Path		Measured Port					
	Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT2		Input Ports	RFIN1	RFIN2	RFIN3	RFIN4	RF OUT1	units
RFIN1 to RFOUT1 (RFOUT2 isolation)	RFIN1	x	26	38	43	30	RFIN1 to RFOUT2 (RFOUT1 isolation)	RFIN1	x	27	29	38	30	dB
	RFOUT1	x	27	45	51	29		RFOUT2	x	27	28	34	29	
RFIN2 to RFOUT1 (RFOUT2 isolation)	RFIN2	31	x	32	41	25	RFIN2 to RFOUT2 (RFOUT1 isolation)	RFIN2	43	x	28	30	33	
	RFOUT1	35	x	36	48	24		RFOUT2	43	x	27	31	32	
RFIN3 to RFOUT1 (RFOUT2 isolation)	RFIN3	36	33	x	25	24	RFIN3 to RFOUT2 (RFOUT1 isolation)	RFIN3	42	29	x	24	33	
	RFOUT1	32	40	x	26	23		RFOUT2	42	29	x	23	32	
RFIN4 to RFOUT1 (RFOUT2 isolation)	RFIN4	36	41	25	x	24	RFIN4 to RFOUT2 (RFOUT1 isolation)	RFIN4	24	29	36	x	26	
	RFOUT1	32	42	26	x	23		RFOUT2	23	30	33	x	26	

Table 1. Port to port typical Isolation



Pin Description

PIN	LABEL	DESCRIPTION
1	RFIN1	RF I/O
2	GND	Ground
3	RFOUT1	RF I/O
4	GND	Ground
5	USID	USID configurable Address input
6	VIO	RFFE Power Supply
7	SCLK	RFFE Clock Signal
8	SDATA	RFFE Data Signal
9	N/C	N/C. (Can be grounded.)
10	GND	Ground
11	RFOUT2	RF I/O
12	GND	Ground
13	RFIN4	RF I/O
14	RFIN3	RF I/O
15	GND	Ground
16	RFIN2	RF I/O
GND PAD	GND PAD	Ground

Register Configuration

Register 0x0000 – Output_Cross_CTRL

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:1	SPARE	Reserved for future use	0x00	No	0	R/WM
0	Output_Cross	Enable DPDT output Switch to cross mode, 0x0: DPDT Direct operating mode 0x1: DPDT output cross operating mode	0x0	No	0	R/WM
		Note: See Truth Table for example of operation				

Register 0x0001 – SW_CTRL

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:6	SPARE	Reserved for future use	0x0	No	0	R/WM
5:4	SW_Connect_Ind[1:0]	Indicate switch connect sequence from bit0 to bit 3 00: one port connect to output1,ouput2 isolation 01: Lower bit in bit0 to bit3 connect to output1 10: Higher bit in bit0 to bit3 connect to output1 11: one port connect to output2,ouput1 isolation	0x0	No	0	R/WM
3:0	Input_Sel[3:0]	Input Ports Select Enables DP4T input Port. Each bit is a dedicated input port. Bit0 <->input1 Bit1 <->input2 Bit2 <->input3 Bit3 <->input4 0000: Isolation 0001: Input 1 Select 0010: Input 2 Select 0100: Input 3 Select 1000: Input 4 Select etc	0x0	No	0	R/WM
		Note: See Truth Table for example of operation				

Register 0x001A – RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B – GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C – PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	1	B/G	No	R/W
6	PWR_MODE[0]	0: ACTIVE 1: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D – PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x1E	No	No	R

Register 0x001E – MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0xC6	No	No	R

Register 0x001F – MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x3	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID The default value at reset is selected via pin SID0. SID0 / USID: 0 → 0x6; 1 → 0x7 *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x6	No	No	R/W

Register 0x0020 – EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Register 0x0022 – GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 – ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x002C – TEST_PATT

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Register 0x002D — EXT_TRIG_MASK

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TriggerMask[10:3]	Setting bit TriggerMask[N] disables Trigger[N] If using an Extended Write to update both TriggerMask and Trigger, than TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0x00	No	No	R/W

Register 0x002E — EXT_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.*	0x00	B/G	No	W

Truth Table

Reg_00	Reg_01						RFOUT1	RFOUT2
0	5	4	3	2	1	0		
0	0	0	0	0	0	0	Isolation	Isolation
0	0	0	0	0	0	1	RFIN1	Isolation
0	0	0	0	0	1	0	RFIN2	Isolation
0	0	0	0	1	0	0	RFIN3	Isolation
0	0	0	1	0	0	0	RFIN4	Isolation
0	0	1	0	0	1	1	RFIN1	RFIN2
0	0	1	0	1	0	1	RFIN1	RFIN3
0	0	1	0	1	1	0	RFIN2	RFIN3
0	0	1	1	0	0	1	RFIN1	RFIN4
0	0	1	1	0	1	0	RFIN2	RFIN4
0	0	1	1	1	0	0	RFIN3	RFIN4
0	1	0	0	0	1	1	RFIN2	RFIN1
0	1	0	0	1	0	1	RFIN3	RFIN1
0	1	0	0	1	1	0	RFIN3	RFIN2
0	1	0	1	0	0	1	RFIN4	RFIN1
0	1	0	1	0	1	0	RFIN4	RFIN2
0	1	0	1	1	0	0	RFIN4	RFIN3
0	1	1	0	0	0	1	Isolation	RFIN1
0	1	1	0	0	1	0	Isolation	RFIN2
0	1	1	0	1	0	0	Isolation	RFIN3
0	1	1	1	0	0	0	Isolation	RFIN4

Reg_00	Reg_01						RFOUT1	RFOUT2
0	5	4	3	2	1	0		
1	0	0	0	0	0	0	Isolation	Isolation
1	0	0	0	0	0	1	Isolation	RFIN1
1	0	0	0	0	1	0	Isolation	RFIN2
1	0	0	0	1	0	0	Isolation	RFIN3
1	0	0	1	0	0	0	Isolation	RFIN4
1	0	1	0	0	1	1	RFIN2	RFIN1
1	0	1	0	1	0	1	RFIN3	RFIN1
1	0	1	0	1	1	0	RFIN3	RFIN2
1	0	1	1	0	0	1	RFIN4	RFIN1
1	0	1	1	0	1	0	RFIN4	RFIN2
1	0	1	1	1	0	0	RFIN4	RFIN3
1	1	0	0	0	1	1	RFIN1	RFIN2
1	1	0	0	1	0	1	RFIN1	RFIN3
1	1	0	0	1	1	0	RFIN2	RFIN3
1	1	0	1	0	0	1	RFIN1	RFIN4
1	1	0	1	0	1	0	RFIN2	RFIN4
1	1	0	1	1	0	0	RFIN3	RFIN4
1	1	1	0	0	0	1	RFIN1	Isolation
1	1	1	0	0	1	0	RFIN2	Isolation
1	1	1	0	1	0	0	RFIN3	Isolation
1	1	1	1	0	0	0	RFIN4	Isolation

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see Figure: Digital Supply Detail)

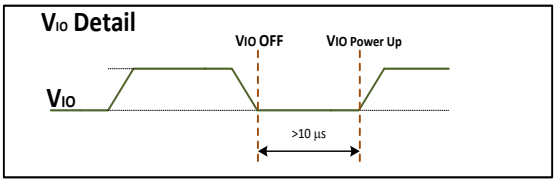


Figure.1 : Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission.
3. VIO must be applied for a minimum of 15 µs before applying RF power.
4. Wait a minimum of typically 3 µs after RFFE bus is idle to apply an RF signal. (see Figure: Digital Signal / RF Power-On Detail)

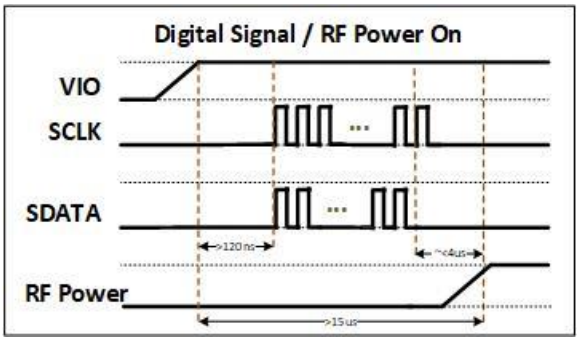


Figure.2: Digital Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see Figure: Switch Event Timing)

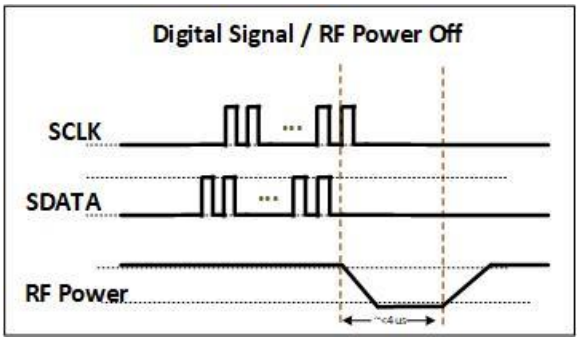


Figure.3: Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 µs before exiting “Low Power Mode”. (see Figure: Low-Power Mode Exit Timimg)

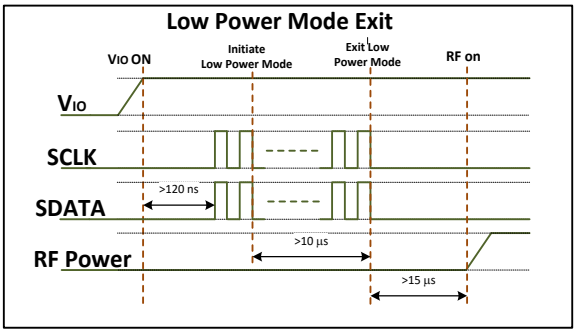
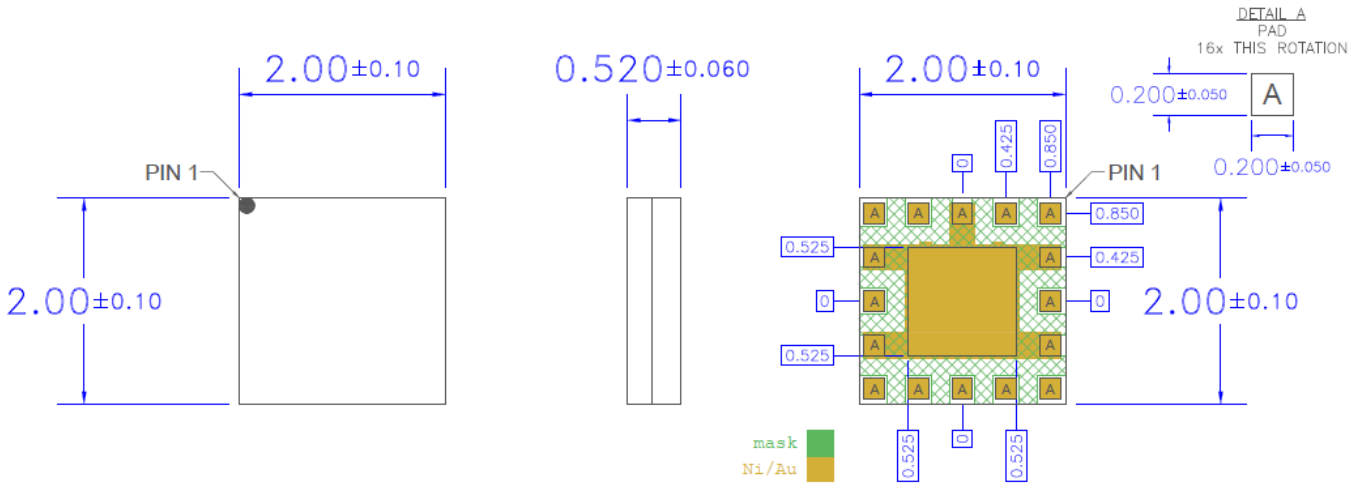


Figure.4: Low-Power Mode Exit Timing

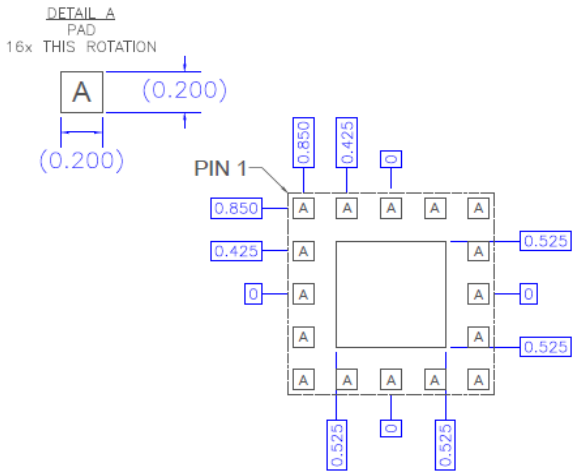
Mechanical Drawing



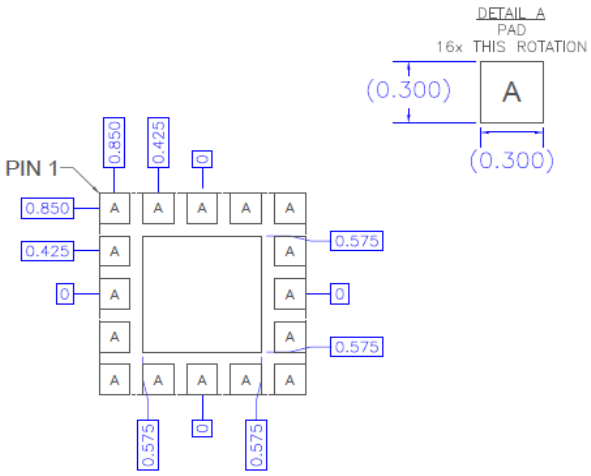
TOP VIEW

SIDE VIEW

BOTTOM VIEW

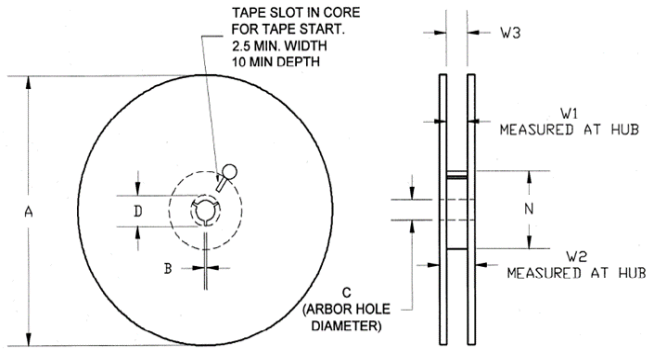


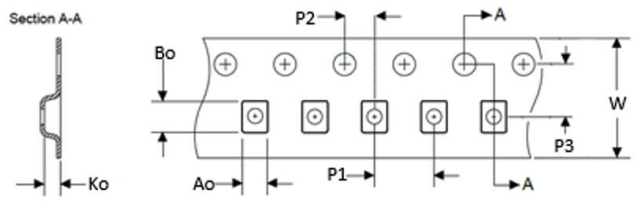
RECOMMENDED LAND PATTERN



RECOMMENDED LAND PATTERN MASK

Tape and Reel Info



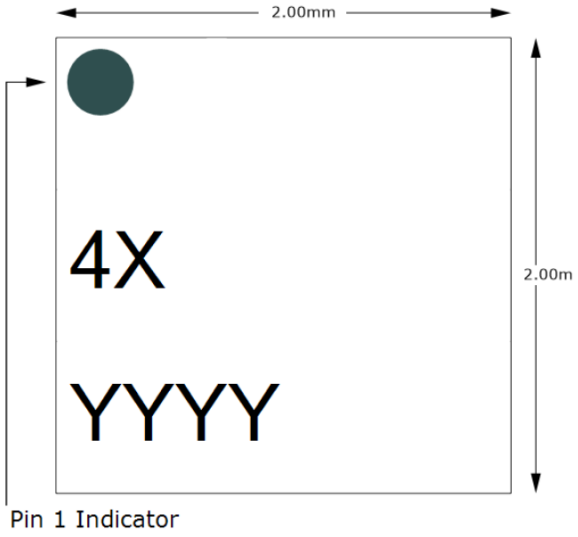


Feature	Measure	Symbol	Size (mm)
Flange	Diameter	D1	330.0
	Thickness	W2	18.2
	Space Between Flange	W1	12.8
Hub	Outer Diameter	D2	102.0
	Arbor Hole Diameter	D3	13.0
	Key Slit Width	B	2.0
	Key Slit Diameter	D4	20.2

Feature	Measure	Symbol	Size (mm)
Cavity	Length	Ao	2.2
	Width	Bo	2.2
	Depth	Ko	0.95
	Pitch	P1	4
Centerline Distance	Cavity to Perforation (Length)	P2	2.0
	Cavity to Perforation (Width)	P3	5.5
Carrier Tape	Width	W	9.2

(Unless otherwise specified, all dimension tolerances per EIA-481)

Marking Diagram



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Revision History

Revision	Description
Rev. G	Production Release Version
Rev.H	Isolation Table, Absolute Max Power simplified, Absolute Max voltage set to 2.15V, Harmonics to 5GHz, Minor editing to Figure 2/3.
Rev.I	Update to Absolute Max table at 25deg C

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice