SGM8480-2
15V Single-Supply, Dual Operational Amplifier with ±10V Output Range

GENERAL DESCRIPTION

The SGM8480-2 precision, low-noise, low-drift dual operational amplifier offers true-zero output that allows the output to cross zero maximizing the dynamic range of an ADC and increasing resolution. In addition, the input common mode range extends from ($+V_S$) - 1.5V down to ($-V_S$) + 3V. The SGM8480-2 integrates charge pump circuitry that generates the negative voltage rail in conjunction with external capacitors. This allows the amplifier to operate from a single 4.5V to 18V power supply, but it is as effective as a normal dual-rail ±4.5V to ±18V amplifier. The architecture eliminates the need for a negative power-supply rail, saving system cost and size.

The SGM8480-2 is unity-gain stable with a gain-bandwidth product of 7.5MHz. The device features low offset voltage of 25μV (MAX), and 200nV_{P-P} noise from 0.1Hz to 10Hz. The low offset and noise specifications and wide input common mode range make the device ideal for sensor transmitters and interfaces. Varying the external charge pump capacitors enables the charge pump noise to be minimized.

The SGM8480-2 is available in Green TSSOP-14 package. It is specified over the -40℃ to +125℃ temperature range.

FEATURES

- **True Bipolar Output Greater than ±10V from a Single 15V Supply Eliminates Space and Cost of Negative Power Supply**
- **Integrated Negative LDO to Cancel Charge Pump Noise**
- **Low Input Offset Voltage: 25μV (MAX)**
- **10nV/$\sqrt{Hz}$ Low Input Noise at 1kHz Provides Wide ADC Dynamic Range**
- **Slew Rate: 6V/μs (TYP)**
- **7.5MHz Gain-Bandwidth Product Provides Wide Frequency Input Range**
- **Quiescent Current: 4.2mA (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-14 Package**

APPLICATIONS

PLC Analog I/O Modules
Sensor Interfaces
Pressure Sensors
Bridge Sensors
Analog Level Shifting/Conditioning

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8480-2	TSSOP-14	-40℃ to +125℃	SGM8480-2XTS14G/TR	SGM84802 XTS14 XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to 20V
CPVDD to GND ..... -0.3V to 20V
CP, CN, CPVSS, V_{SS} Input Current..... ±20mA
Input Common Mode Voltage Range.....
.....$(-V_{DD})$ - 0.3V to $(+V_{DD})$ + 0.3V
Differential Input Current..... ±20mA
Differential Input Voltage [1] ..... ±1V
OUTA, OUTB to GND .....$(-V_{DD})$ - 0.3V to $(+V_{DD})$ + 0.3V
Short-Circuit Duration, OUTA, OUTB to either Supply Rail
.....1s
Junction Temperature .....+150℃
Storage Temperature Range.....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM.....8000V
MM.....300V
CDM 1000V

NOTE: 1. The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding ±1V are applied, limit input current to ±20mA.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .....4.5V to 18V
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

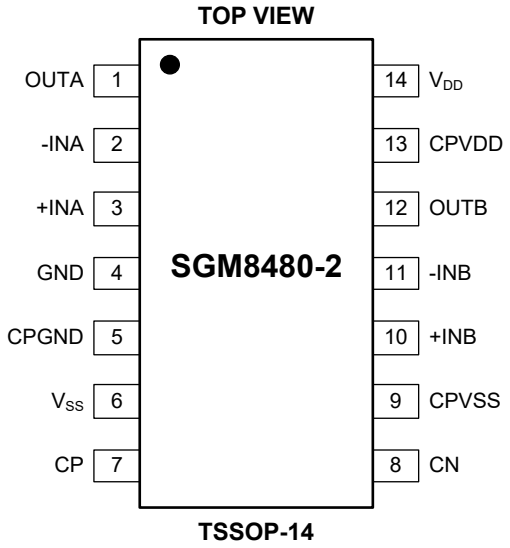
ESD SENSITIVITY CAUTION

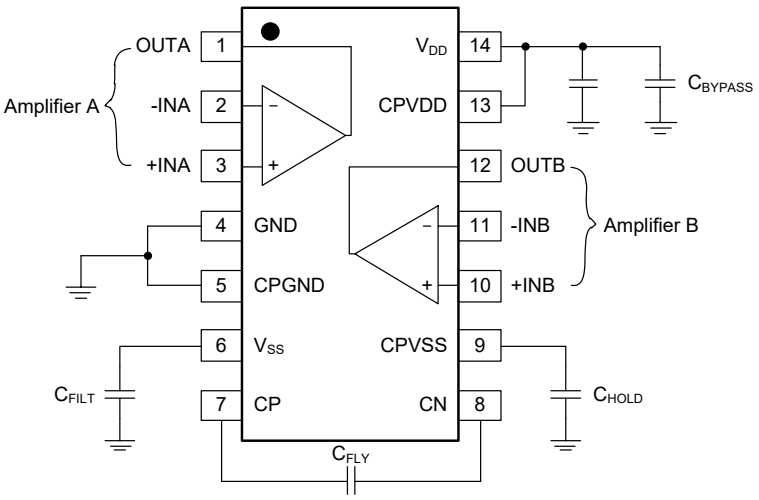
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION





PIN DESCRIPTION

PIN	NAME	FUNCTION
1	OUTA	Channel A Output.
2	-INA	Channel A Negative Input.
3	+INA	Channel A Positive Input.
4	GND	Ground. Connect GND to a solid ground plane.
5	CPGND	Charge Pump Ground. Connect CPGND to GND.
6	V_{SS}	Filtered Negative Power Supply Output. Bypass V_{SS} with a low-ESR capacitor (C_{FILT} = 1μF) to GND.
7	CP	Charge Pump Positive Capacitor Connection. Capacitor connection only to CN. Do not connect any voltage on CP or CN. Connect a low-ESR capacitor (C_{FLY} = 1μF) between CP and CN.
8	CN	Charge Pump Negative Capacitor Connection. Capacitor connection only to CP. Do not connect any voltage on CN or CP. Connect a low-ESR capacitor (C_{FLY} = 1μF) between CP and CN.
9	CPVSS	Charge Pump Negative Supply Output. Bypass CPVSS with a 1μF capacitor to CPGND.
10	+INB	Channel B Positive Input.
11	-INB	Channel B Negative Input.
12	OUTB	Channel B Output.
13	CPVDD	Charge Pump Supply Voltage Input. Connect CPVDD to V_{DD}. Bypass CPVDD with a 0.1μF capacitor to GND.
14	V_{DD}	Device Supply Voltage Input. Bypass V_{DD} with a 0.1μF capacitor to GND.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CPVDD} = 5V to 15V, V_{GND} = 0V, V_{CM} = GND, R_L = 5kΩ to GND, C_{FLY} = 1μF, C_{HOLD} = 1μF, C_{FILT} = 1μF, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage	V_{OS}		+25℃		5	25	μV
			Full			45	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		0.2		μV/℃
Input Bias Current	I_B		+25℃		0.5	5	nA
			Full			6	
Input Offset Current	I_{OS}		+25℃		1	6	nA
			Full			9	
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ + 3		$(+V_S)$ - 1.5	V
Common Mode Rejection Ratio	CMRR	V_{DD} = 15V, V_{CM} = -12V to 13.5V	+25℃	126	140		dB
			Full	123			
		V_{DD} = 5V, V_{CM} = -2V to 3.5V	+25℃	118	140		
			Full	115			
Open-Loop Voltage Gain	A_{OL}	V_{DD} = 15V, V_{OUT} = -12V to 13.5V	+25℃	122	145		dB
			Full	119			
		V_{DD} = 5V, V_{OUT} = -1.3V to 3.5V	+25℃	114	140		
			Full	111			
OUTPUT CHARACTERISTICS							
Output Voltage Swing High	V_{OH}	V_{DD} = 15V	+25℃		220	300	mV
			Full			385	
		V_{DD} = 5V	+25℃		72	100	
			Full			135	
Output Voltage Swing Low	V_{OL}	V_{DD} = 15V	+25℃		100	130	mV
			Full			185	
		V_{DD} = 5V	+25℃		28	38	
			Full			55	
Output Short-Circuit Current	I_{SC}	V_{DD} = 15V	+25℃	±58	±85		mA
		V_{DD} = 5V	+25℃	±45	±66		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{CPVDD} = 5V to 15V, V_{GND} = 0V, V_{CM} = GND, R_L = 5kΩ to GND, C_{FLY} = 1μF, C_{HOLD} = 1μF, C_{FILT} = 1μF, Full = -40℃ to +125℃, unless otherwise noted.)

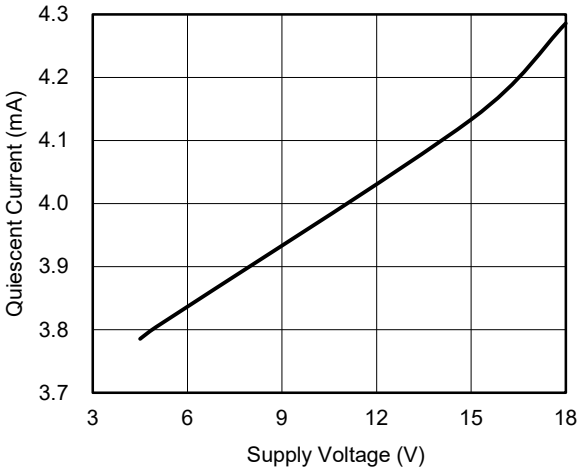
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power Supply Voltage Input Range	V_{DD}	Guaranteed by PSRR	Full	4.5		18	V
Charge Pump Supply Voltage Input Range (1)	V_{CPVDD}		Full	4.5		18	V
Charge Pump Negative Supply Output	V_{CPVSS}	V_{DD} = 15V	+25℃		-14.95		V
		V_{DD} = 5V	+25℃		-4.95		
Filtered Negative Supply Output	V_{SS}	V_{DD} = 15V	+25℃		-14		V
		V_{DD} = 5V	+25℃		-4		
Total Quiescent Current	I_{DD}	V_{DD} = 15V, I_{OUT} = 0	+25℃		4.2	5.5	mA
			Full			6.7	
		V_{DD} = 5V, I_{OUT} = 0	+25℃		3.8	5	
			Full			6.2	
Power Supply Rejection Ratio	PSRR	V_{DD} = 4.5V to 18V	+25℃	114	134		dB
			Full	111			
DYNAMIC PERFORMANCE							
Gain-Bandwidth Product	GBP	C_L = 10pF	+25℃		7.5		MHz
Slew Rate	SR		+25℃		6		V/μs
Settling Time	t_S	V_{IN} = 1V Step, A_V = +1	+25℃		0.7		μs
Charge Pump Frequency	f_{OSC}		+25℃		440		kHz
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, V_{IN} = $2V_{P-P}$, A_V = +1	+25℃		-110		dB
Crosstalk	X_{talk}	f = 1kHz	+25℃		-95		dB
NOISE							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		200		nV_{P-P}
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		10		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 1kHz	+25℃		280		$pA/\sqrt{Hz}$

NOTE: 1. CPVDD voltage must be equal to V_{DD} voltage. Connect CPVDD to V_{DD}.

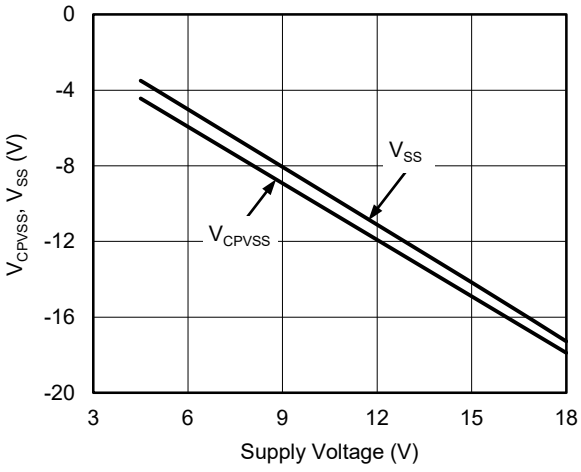
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_{DD} = V_{CPVDD} = 15V, V_{GND} = 0V, V_{CM} = GND, C_{FLY} = 1μF, C_{HOLD} = 1μF, C_{FILT} = 1μF, R_L = 5kΩ and C_L = 10pF to GND, unless otherwise noted.

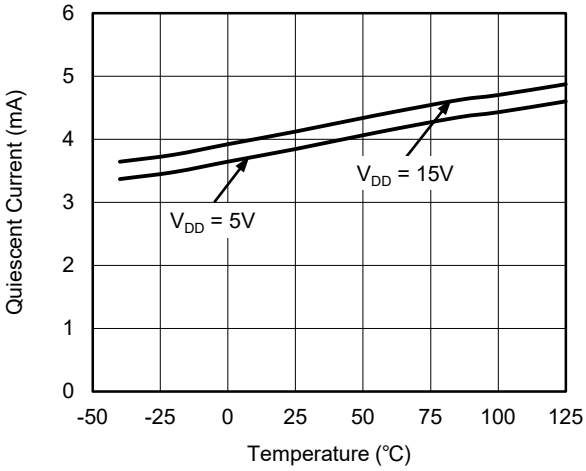
Quiescent Current vs. Supply Voltage



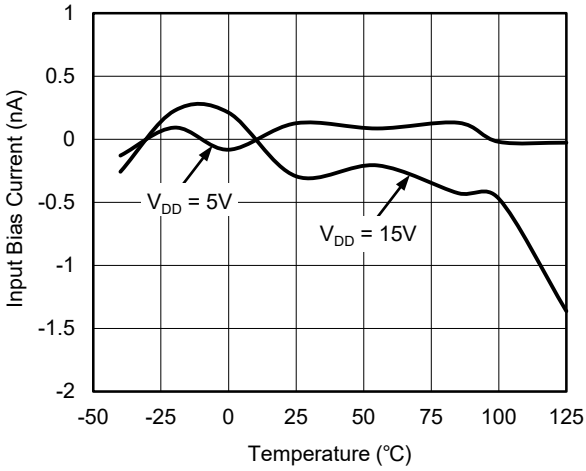
V_{CPVSS} and V_{SS} vs. Supply Voltage



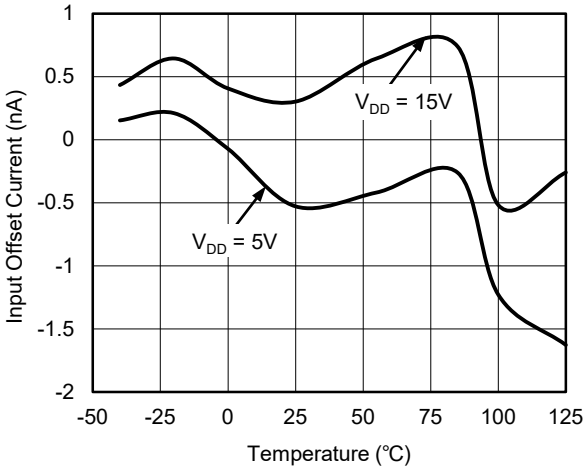
Quiescent Current vs. Temperature



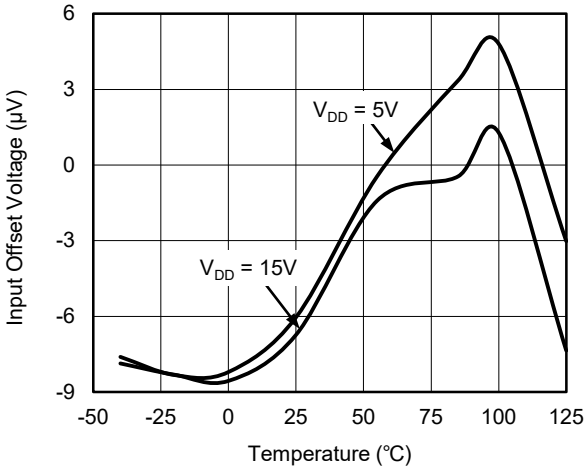
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature



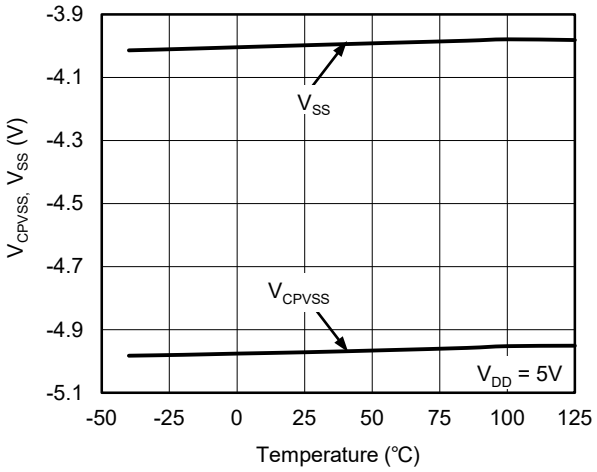
Input Offset Voltage vs. Temperature



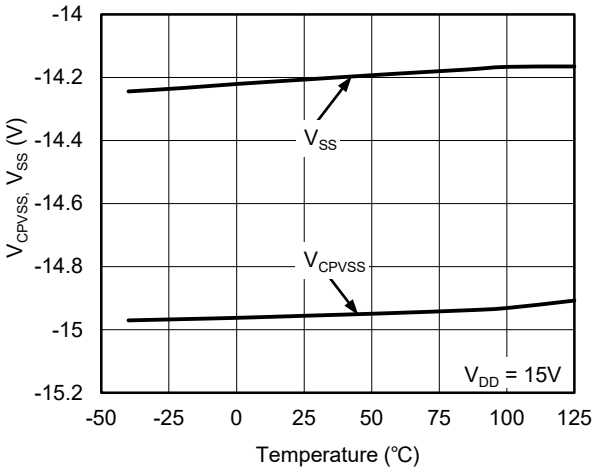
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = V_{CPVDD} = 15V, V_{GND} = 0V, V_{CM} = GND, C_{FLY} = 1μF, C_{HOLD} = 1μF, C_{FILT} = 1μF, R_L = 5kΩ and C_L = 10pF to GND, unless otherwise noted.

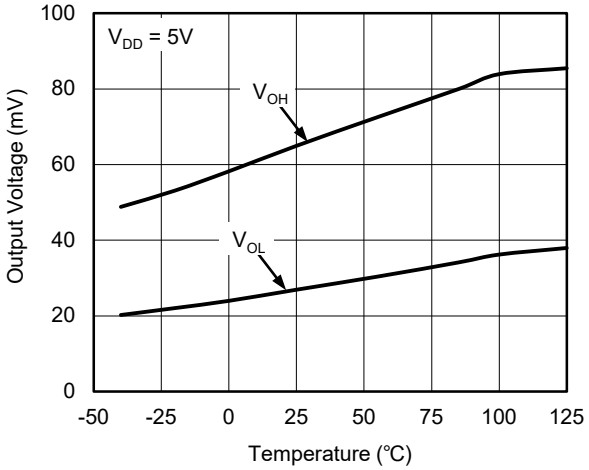
V_{CPVSS} and V_{SS} vs. Temperature



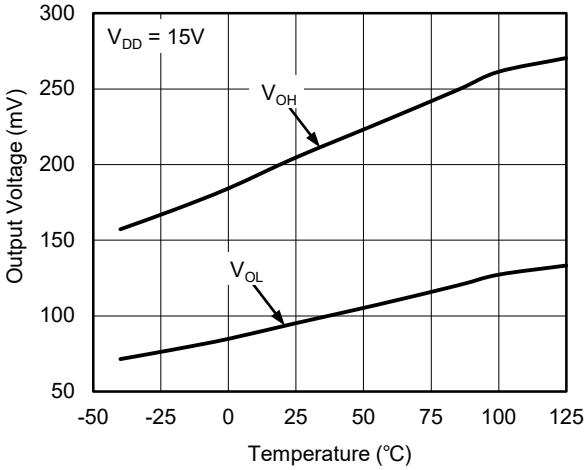
V_{CPVSS} and V_{SS} vs. Temperature



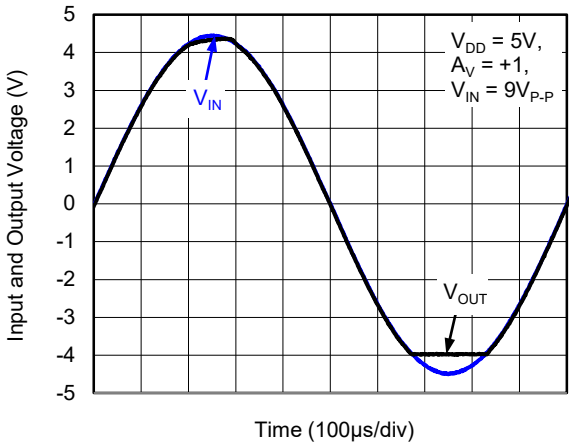
Output Voltage vs. Temperature



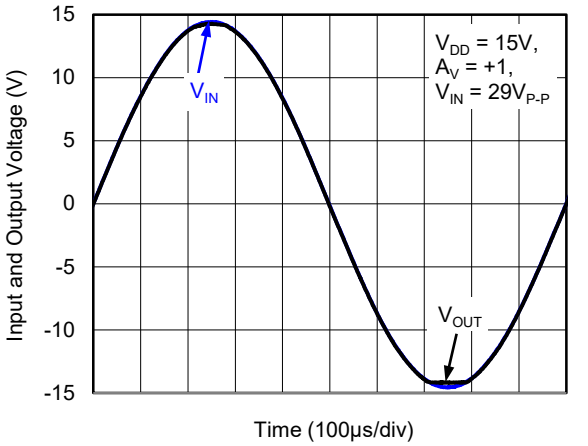
Output Voltage vs. Temperature



No Phase Reversal



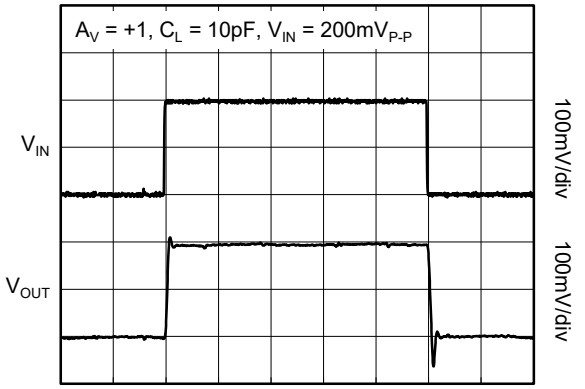
No Phase Reversal



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

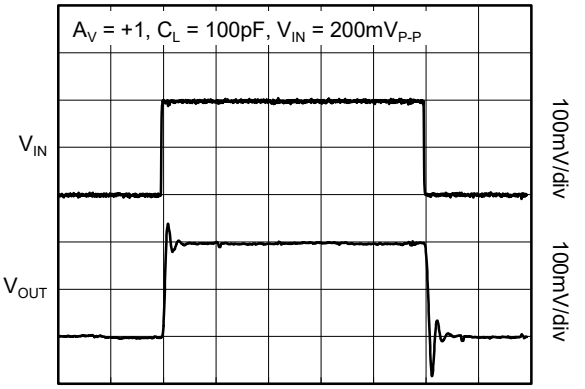
At T_A = +25℃, V_{DD} = V_{CPVDD} = 15V, V_{GND} = 0V, V_{CM} = GND, C_{FLY} = 1μF, C_{HOLD} = 1μF, C_{FILT} = 1μF, R_L = 5kΩ and C_L = 10pF to GND, unless otherwise noted.

Small-Signal Step Response



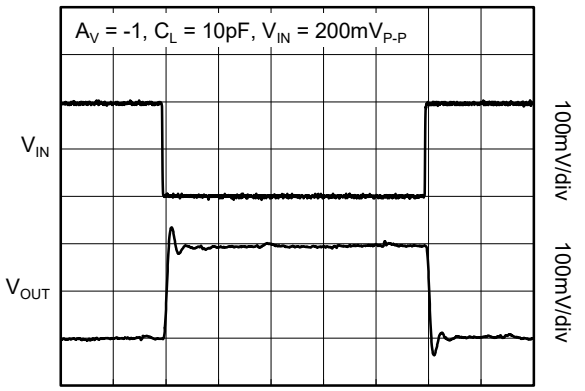
Time (1μs/div)

Small-Signal Step Response



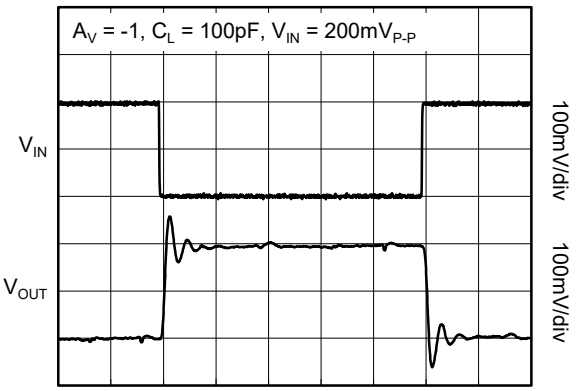
Time (1μs/div)

Small-Signal Step Response



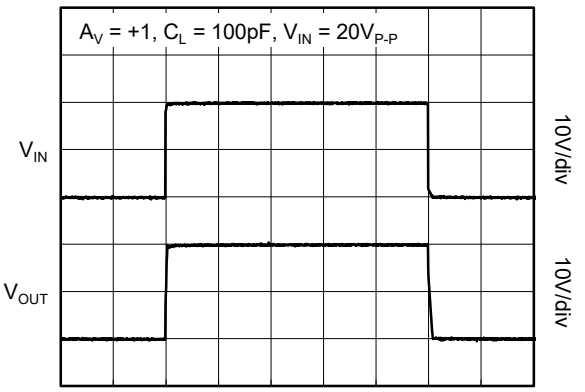
Time (1μs/div)

Small-Signal Step Response



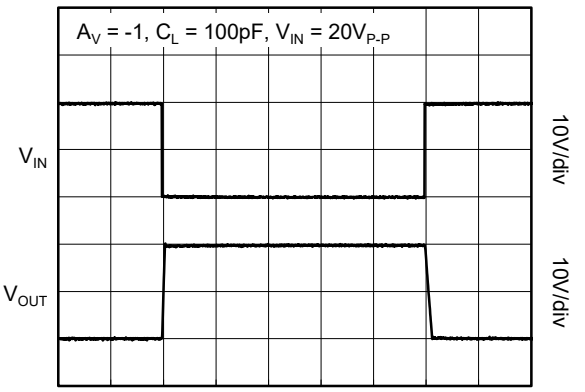
Time (1μs/div)

Large-Signal Step Response



Time (20μs/div)

Large-Signal Step Response

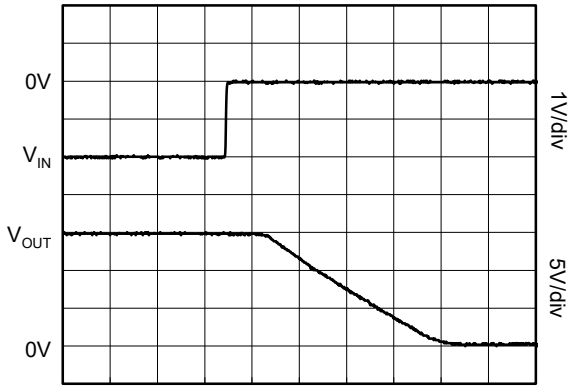


Time (20μs/div)

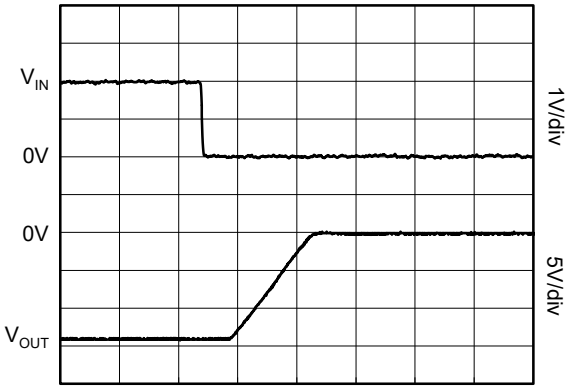
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = V_{CPVDD} = 15V, V_{GND} = 0V, V_{CM} = GND, C_{FLY} = 1μF, C_{HOLD} = 1μF, C_{FILT} = 1μF, R_L = 5kΩ and C_L = 10pF to GND, unless otherwise noted.

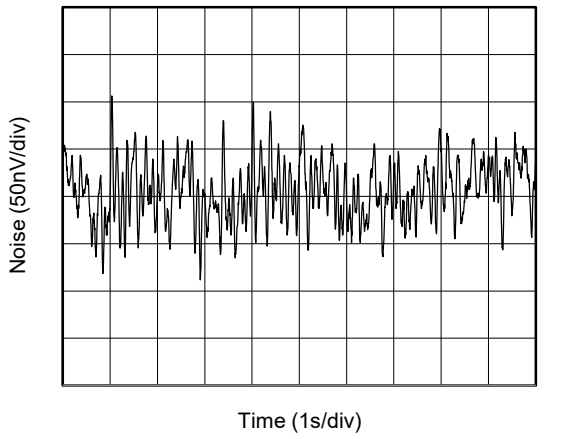
Positive Overload Recovery



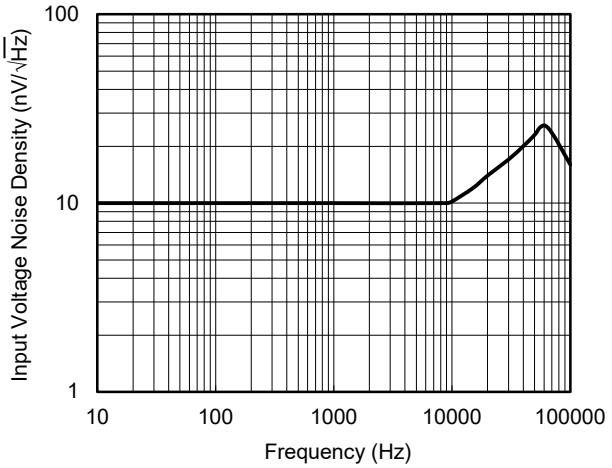
Negative Overload Recovery



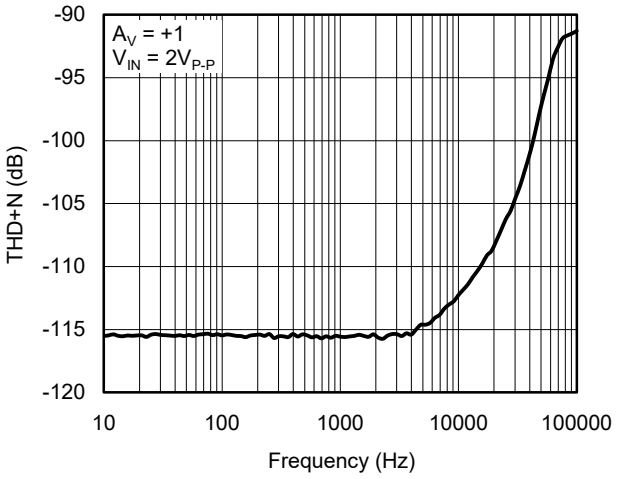
0.1Hz to 10Hz Input Voltage Noise



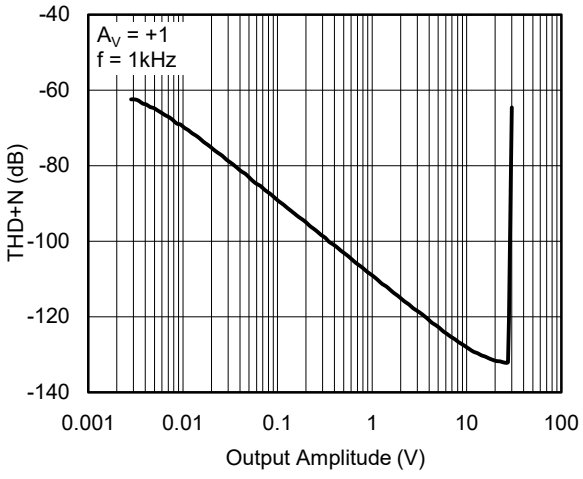
Input Voltage Noise Density vs. Frequency



THD+N vs. Frequency



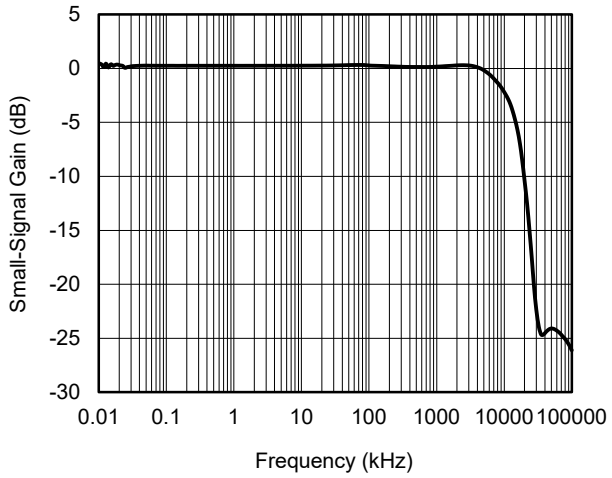
THD+N vs. Output Amplitude



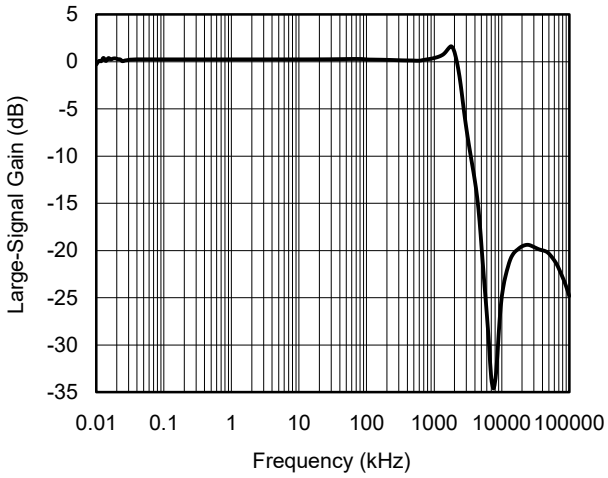
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{DD} = V_{CPVDD} = 15V, V_{GND} = 0V, V_{CM} = GND, C_{FLY} = 1μF, C_{HOLD} = 1μF, C_{FILT} = 1μF, R_L = 5kΩ and C_L = 10pF to GND, unless otherwise noted.

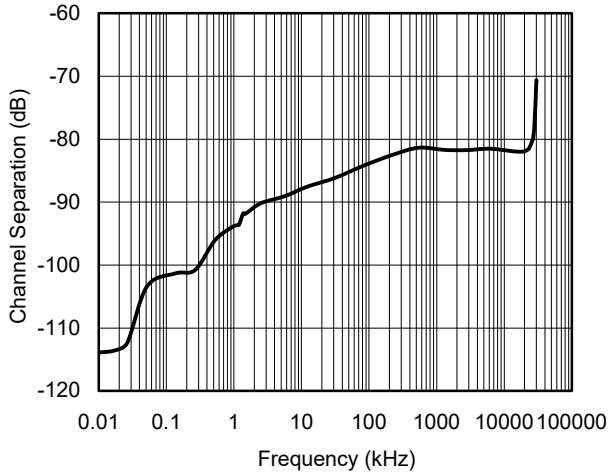
Small-Signal Gain vs. Frequency



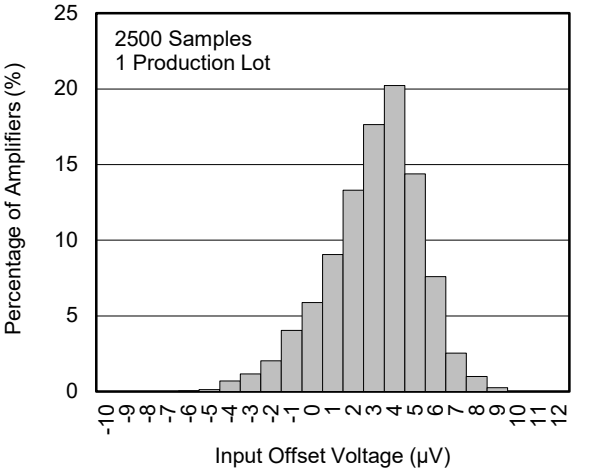
Large-Signal Gain vs. Frequency



Channel Separation vs. Frequency



Input Offset Voltage Production Distribution



TYPICAL APPLICATION CIRCUITS

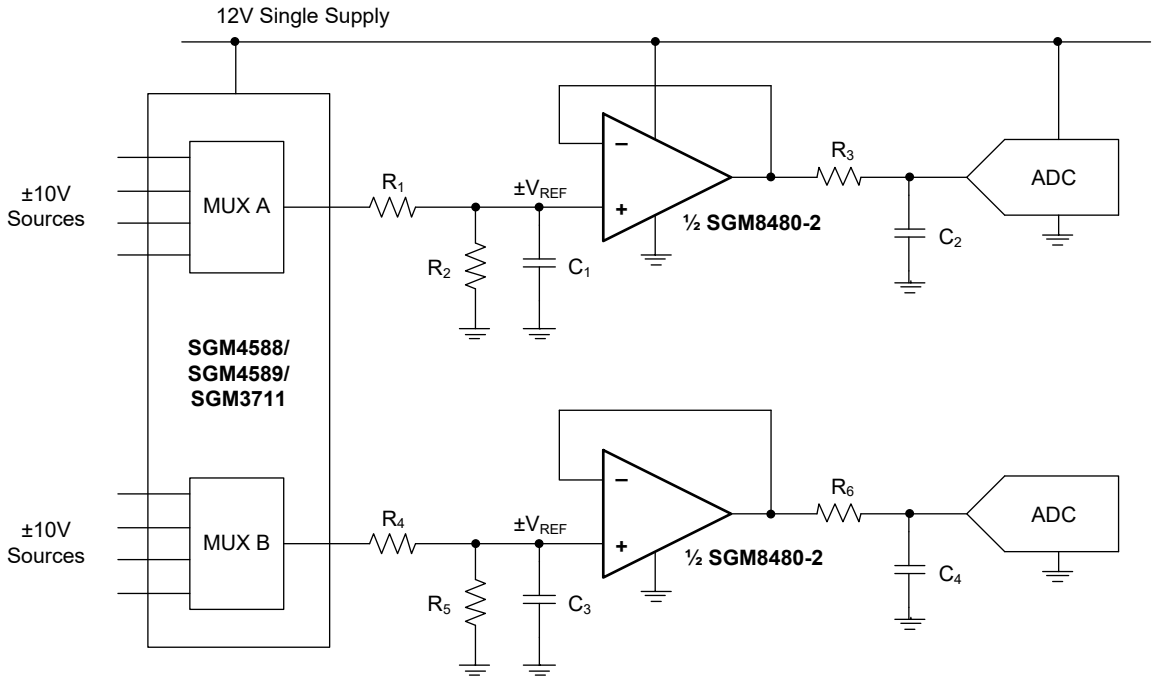


Table 1. Selection Guide for the Typical Operating Circuit

PART NO.	FUNCTION	VOLTAGE SUPPLY RANGE (V)	INPUT VOLTAGE RANGE (V)
SGM8480-2	Precision Amplifier	4.5 to 18	-15 to 16.5
SGM4588	8:1 MUX	±4.5 to ±15	±14
SGM4589	Dual 4:1 MUX	±4.5 to ±15	±14
SGM3711	Dual DPDT Switch	3.3 to 12	±10

DETAILED DESCRIPTION

The SGM8480-2 is a high-precision amplifier that provides less than 25μV of maximum input-referred offset and low 1/f noise. These characteristics are achieved by using chopper-stabilized techniques.

Common Internal Charge Pump

The SGM8480-2's integrated charge pump produces a negative voltage rail (V_{SS}) that is common to both amplifiers (see Figure 1 for external capacitor connections). The device consumes a total of 4.2mA (TYP) of quiescent current (including both the operational amplifiers and the charge pump operation).

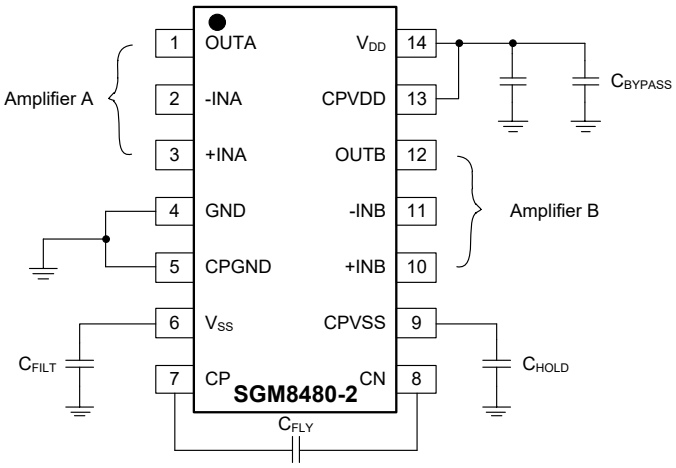


Figure 1. External Capacitor Connections

The V_{SS} generator acts as a negative supply for the SGM8480-2, and has 85mA limited sink current capability. Attempting to load more than its capability will reduce the negative supply voltage, affecting its driving capability when sinking current. If both amplifiers sink a total current beyond typically 85mA, it will result in reduced swing in the negative direction and increased ripple affecting both outputs and degrading output accuracy and performance of both amplifiers.

In order to prevent both amplifiers from being affected by over-current on negative power supply, each amplifier has output current limit function, and the current limit value is 42.5mA for each amplifier. This guarantees the total output current will not exceed 85mA, and the V_{SS} negative supply doesn't rise due to overloading.

ESD Networks

The SGM8480-2 output swing can be well below 0V while all the other circuitry on the board may have 0V as its most negative terminal. Since almost all modern integrated circuits protect their inputs with a network of diode clamps to their power rails, it is possible to discover the driven circuit is clamping the SGM8480-2's output (Figure 2).

Correct circuit should be designed such that the SGM8480-2's output will not be clamped by another circuit's ESD network. A common solution to this problem is to arrange that the output is level-shifted as well as amplified or conditioned by the SGM8480-2. Be sure not to exceed the absolute maximum ratings on any devices surrounding the SGM8480-2 amplifier.

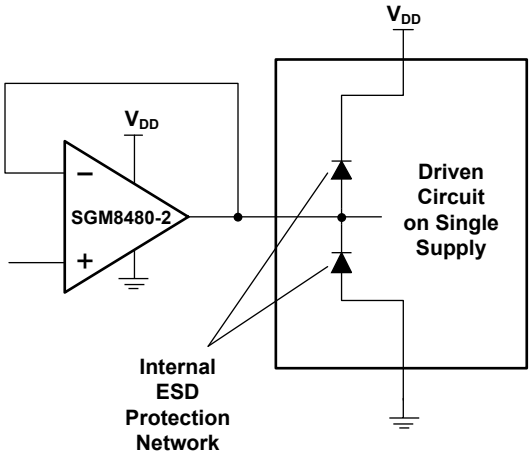


Figure 2. Possibility of Clamping the SGM8480-2 Output via Another Circuit's ESD Network

DETAILED DESCRIPTION (continued)

Capacitor Selection

The SGM8480-2 requires three external capacitors (C_{FLY}, C_{HOLD} and C_{FILT}) to generate the V_{SS} negative supply rail. The charge pump output resistance is a function of the ESR of C_{FLY}, C_{HOLD} and C_{FILT}. To maintain the lowest output resistance, use capacitors with low ESR.

Flying Capacitor (C_{FLY})

Increasing the flying capacitor's value reduces the output resistance. Above 0.1μF, increasing C_{FLY}'s capacitance has negligible effect because internal switch resistance and capacitor ESR then dominate the output resistance.

Output Capacitor (C_{HOLD})

Increasing the output capacitor's value reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Lower capacitance values can be used with light loads if higher output ripple can be tolerated. Refer to the following graphs to estimate the peak-to-peak ripple for certain sinking current value.

V_{SS} Bypass Capacitor (C_{FILT})

Bypass the incoming supply (V_{SS}) to reduce its AC impedance and the impact of the charge pump's switching noise. Connect a minimum of a 0.1μF low-ESR capacitor from V_{SS} to GND as close as possible to the IC.

Noise Suppression

Low-frequency noise, inherent in all active devices, is inversely proportional to frequency. Charges at the oxide-silicon interface that are trapped-and-released by oxide and PN junction occur at low frequency more often. The SGM8480-2 eliminates the 1/f noise internally, thus making it an ideal choice for DC or low frequency, high-precision applications. The 1/f noise appears as a slow varying offset voltage and is eliminated by the chopping technique used.

Electromagnetic interference (EMI) noise occurs at higher frequency that results in malfunction or degradation of electrical equipment. The ICs have an input EMI filter to avoid the output being affected by radio frequency interference. The EMI filter composed of passive devices presents significant higher impedance to higher frequency.

Near-Zero Source Impedances

The negative voltage generator has a finite current sink capability (typically around 85mA for C_{FLY} = 1μF, C_{HOLD} = C_{FILT} = 1μF). If the device is overloaded by the output sink current of one or both amplifiers combined, it will lose regulation, limiting output swing in the negative direction. Additionally, if regulation is lost, and the input is forced towards the negative rail, the SGM8480-2 may enter a latch-up condition. This latch-up is non-destructive, and the device will recover when the fault conditions are removed.

The SGM8480-2 is specified with a 5kΩ load on each output channel. This results in a maximum output load current that is well below an overload of the generator, and so the device will not latch up. It is possible to drive even heavier loads, although the total output sink current (of both channels combined) should not be allowed to exceed 85mA peak. When driving loads that may approach the output's limit, it is recommended that the inputs should be high-impedance sources or add a protective 5kΩ series resistor.

DETAILED DESCRIPTION (continued)

True Zero Output Architecture

The SGM8480-2 is unique compared to the majority of operational amplifiers. The SGM8480-2 contains an internal charge pump and a negative low dropout regulator that generates a low noise negative voltage rail (V_{SS}), shared by both amplifiers. This allows the amplifier input and output ranges to extend substantially below 0V, while powered from only a single positive supply. V_{SS} output supplies both amplifiers and its output load current. V_{SS} can be used to power external circuitry but the additional load current is seen as additional load by the charge pump. This internally generated negative supply can cause currents to flow in unexpected paths especially through the electrostatic discharge protection networks found in almost all modern integrated circuits (Figure 3).

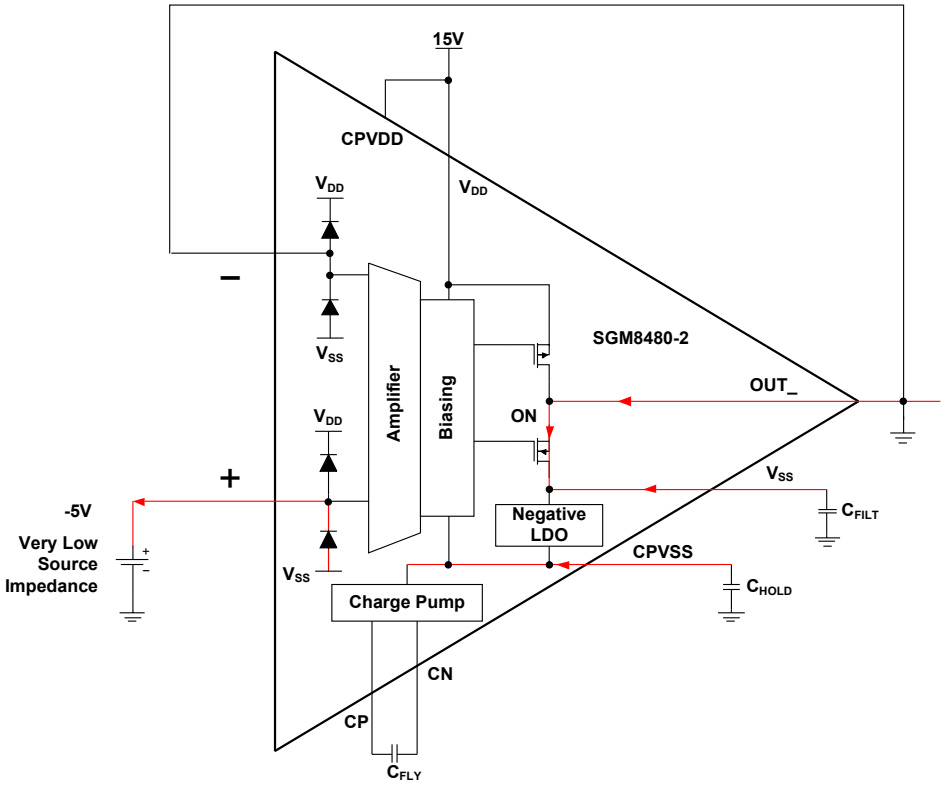


Figure 3. Possible Latch-up Due to Overloading the SGM8480-2

APPLICATION INFORMATION

Layout Guidelines

The SGM8480-2 features ultra-low offset voltage and noise, causing the Seebeck effect error to become significant. Therefore, to get optimum performance follow the following layout guidelines:

Avoid temperature gradients at the junction of two dissimilar metals. The most common dissimilar metals used on a PCB are solder to component lead and solder to board trace. Dissimilar metals create a local thermocouple. A variation in temperature across the board can cause an additional offset due to the Seebeck effect at the solder junctions. To minimize the Seebeck effect, place the amplifier away from potential heat sources on the board, if possible. Orient the resistors such that both the ends are heated equally. It is good practice to match the input signal path to ensure that the type and number of thermoelectric junctions remain the same. For example, consider using dummy 0Ω resistors oriented such that the thermoelectric sources due to the real resistors in the signal path is cancelled. It is recommended to flood the PCB with ground plane. The ground plane ensures that heat is distributed uniformly reducing the potential offset voltage degradation due to Seebeck effect.

REVISION HISTORY

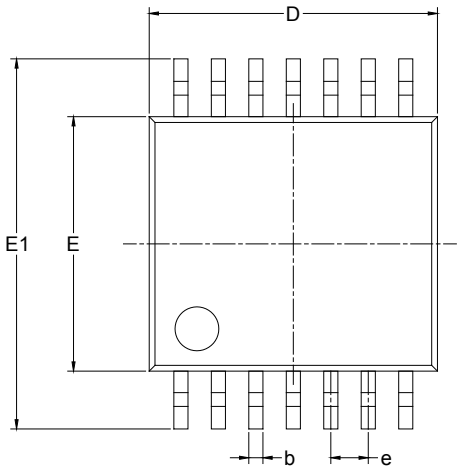
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

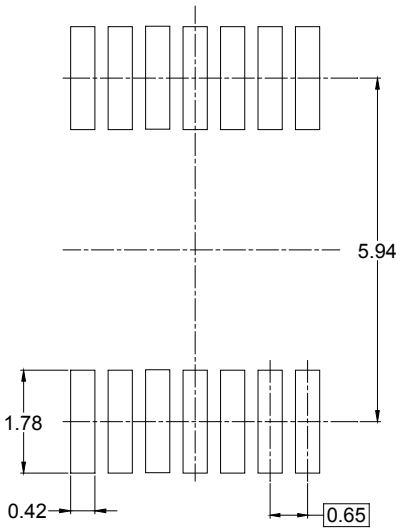
Changes from Original (DECEMBER 2017) to REV.A

Changed from product preview to production data	All

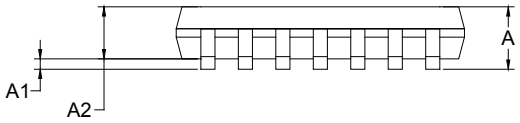
PACKAGE OUTLINE DIMENSIONS

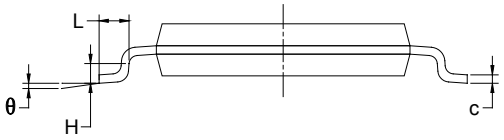
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

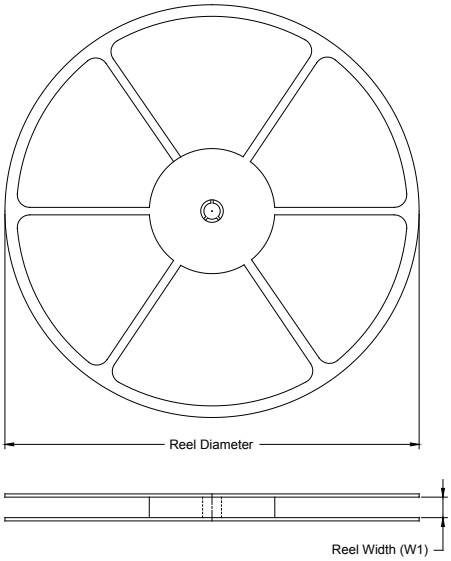




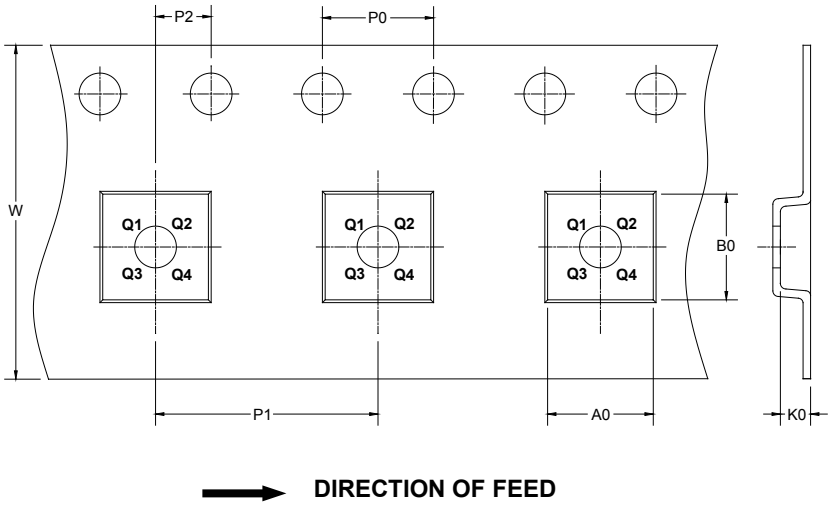
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



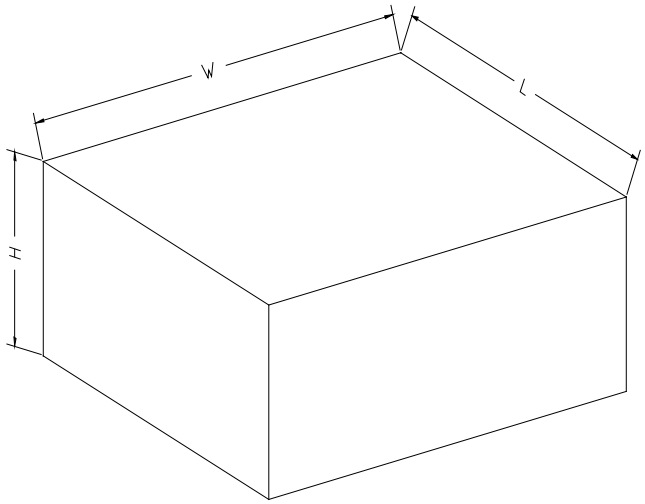
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002