SGM5348-10
8 Channels, 10-Bit Digital-to-Analog Converter with Output Operational Amplifier

GENERAL DESCRIPTION

The SGM5348-10 features 8 channels of digital-to-analog converter (DAC) with output amplifiers. The output amplifier provides high current drive capability. The digital data is sent via SPI interface, and cascaded connections can be used. The SGM5348-10 also offers daisy-chain operation, where an unlimited number of SGM5348-10s can be updated simultaneously using a single serial interface.

There are two references for the SGM5348-10. One reference input serves channels 1 through 4, while the other reference serves channels 5 through 8. Each reference can be set independently between 0.5V and V_{CC}, providing the widest possible output dynamic range. The SGM5348-10 has a 16-bit input shift register that controls the mode of operation, the power-down condition and the register/output value of the DAC channels. All 8 channels DAC outputs can be updated simultaneously or individually.

A power-on reset circuit ensures that the DAC outputs are set to 0V during power-up and remain 0V until there is a valid data written into the device. The power-down feature of the SGM5348-10 allows each DAC to be independently powered with three different termination options. With all the DAC channels powered down, power consumption reduces to less than 1.5μW at 3V and less than 3μW at 5V. The low power consumption and small packages of the SGM5348-10 make it an excellent choice for use in battery powered equipment.

The SGM5348-10 is suitable for normal DAC in industrial applications, and it also can be used as audio signal volumes control or replacement for potentiometers for adjustment.

The SGM5348-10 is available in a Green TSSOP-16 package. It operates over the extended industrial temperature range of -40℃ to +125℃.

FEATURES

- **Low Power Consumption (0.5mW/CH)**
- **Integrating 8 Channels of 10-Bit DAC**
- **Built-in Rail-to-Rail Output Amplifier: Sink/Source Current with Short Current Control**
- **Daisy-Chain Capability**
- **Simultaneous 8 Channels Output Updating**
- **Individual Channel Power-Down Capability**
  - **0.6μA (TYP) I_{CC} for Power-Down Mode**
- **0.1% (TYP) Gain Error for All Channels**
- **Interface Sees No Quiescent Current when $V_{BUS} < V_{CC}$**
- **Power-On Reset: Output Reset to GND**
- **Serial Data Input: Up to 40MHz Operation**
- **TTL Compatible Input Logic Level**
- **Wide Power Supply Range: 2.8V to 5.5V**
- **Dual Reference Voltages with Range of 0.5V to V_{CC}**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-16 Package**

APPLICATIONS

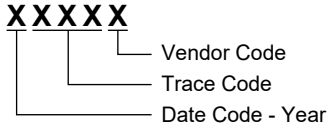
Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators
Voltage Reference for ADCs
Sensor Supply Voltage
Range Detectors

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5348-10	TSSOP-16	-40℃ to +125℃	SGM5348-10XTS16G/TR	SGMME2 XTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{CC} ..... -0.3V to 6.5V
Input Voltage Range, V_{IN} .....-0.3V to V_{CC} + 0.3V
Output Voltage Range, V_{OUT} .....-0.3V to V_{CC} + 0.3V
Input Current at Any Pin..... 10mA
Package Input Current..... 30mA
Package Thermal Resistance
TSSOP-16 ..... 120℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .....-40℃ to +125℃
Power Supply Voltage Range, V_{CC} .....2.8V to 5.5V
Reference Voltage, V_{REF1}, V_{REF2} ..... 0.5V to V_{CC}
Oscillation Limited Output Capacitance, C_{OL} ..... 2nF (MAX)
SCLK Frequency .....40MHz (MAX)

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

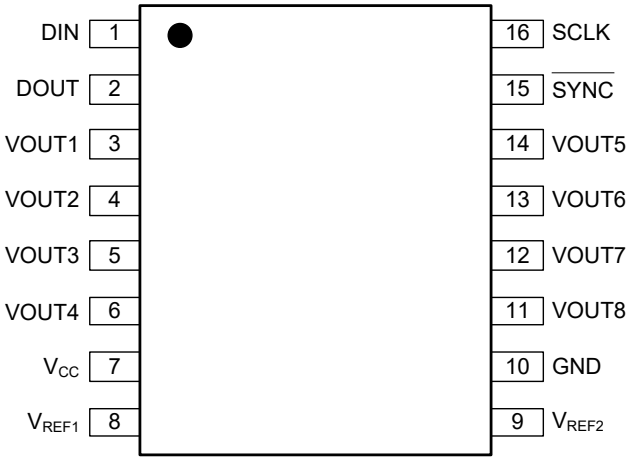
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-16

PIN DESCRIPTION

NAME	PIN	TYPE	DESCRIPTION
DIN	1	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
DOUT	2	Digital Output	Serial Data Output. DOUT is used in daisy-chain operation and is connected directly to a DIN pin on another SGM5348-10. Data is not available at DOUT unless $\overline{SYNC}$ remains low for more than 16 SCLK cycles.
GND	10	Ground	Ground Reference for All On-chip Circuitry.
SCLK	16	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
$\overline{SYNC}$	15	Digital Input	Frame Synchronization Input. When this pin goes low, data is written into the DAC's input shift register on the falling edges of SCLK. After the 16th falling edge of SCLK, a rising edge of $\overline{SYNC}$ causes the DAC to be updated. If $\overline{SYNC}$ is brought high before the 15th falling edge of SCLK, the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
V_{CC}	7	Power Supply	Power Supply Input. Must be decoupled to GND.
VOUT1	3	Analog Output	CH1 Analog Output Voltage.
VOUT2	4	Analog Output	CH2 Analog Output Voltage.
VOUT3	5	Analog Output	CH3 Analog Output Voltage.
VOUT4	6	Analog Output	CH4 Analog Output Voltage.
VOUT5	14	Analog Output	CH5 Analog Output Voltage.
VOUT6	13	Analog Output	CH6 Analog Output Voltage.
VOUT7	12	Analog Output	CH7 Analog Output Voltage.
VOUT8	11	Analog Output	CH8 Analog Output Voltage.
V_{REF1}	8	Analog Input	Un-Buffered Reference Voltage Shared by Channels 1, 2, 3 and 4. Must be decoupled to GND.
V_{REF2}	9	Analog Input	Un-Buffered Reference Voltage Shared by Channels 5, 6, 7 and 8. Must be decoupled to GND.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 5.5V, T_A = -40℃ to +125℃, V_{REF1} = V_{REF2} = V_{CC}, C_L = 200pF to GND, input code range from 12 to 1011. Typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Analog DC Performance					
Resolution		10			Bit
INL (1)			0.8	2.8	LSB
DNL (2)	Monotonicity guaranteed by design	-0.25		0.3	LSB
Offset			3	15	mV
Gain Error			0.1	0.45	%FSR
Offset Drift			10		μV/℃
Gain Drift			2		ppmFS/℃
Zero Code Error	0μA current load		3	15	mV
	200μA current load		5		
	1mA current load		8		
Full Scale Error	0μA current load		3	25	mV
	200μA current load		6		
	1mA current load		20		
Zero Code Drift			5		μV/℃
Full Scale Error Drift			5		μV/℃
Analog AC Performance					
Output Settling Time	To 1LSB		7		μs
Slew Rate	C_{LOAD} = 200pF		0.9		V/μs
Noise Density	Code = 0x200, f = 1kHz		30		nV/$\sqrt{Hz}$
Noise	30kHz LPF		17		μV_{RMS}
Multiplying Bandwidth			300		kHz
Wake-Up Time	C_{LOAD} = 200pF		8		μs
Output Characteristics					
Output Resistance			0.3		Ω
Short Current	Sink		37		mA
	Source		37		
Continuous Current (3)	V_{CC} = 2.8V		5		mA
	V_{CC} = 5.5V		10		
Maximum Capacitance Load			2		nF
Reference Characteristics					
V_{REF1}/V_{REF2}		0.5		V_{CC}	V
Input Impedance			50		kΩ
Digital Input Characteristics					
Input Current			0.1	1	μA
Input Low Voltage	V_{CC} = 2.8V to 3.6V			0.6	V
	V_{CC} = 4.5V to 5.5V			0.8	
Input High Voltage	V_{CC} = 2.8V to 3.6V	2.3			V
	V_{CC} = 4.5V to 5.5V	3.5			
Input Hysteresis			0.2		V

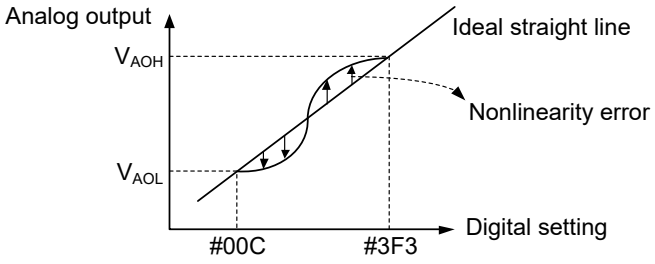
ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 5.5V, T_A = -40℃ to +125℃, V_{REF1} = V_{REF2} = V_{CC}, C_L = 200pF to GND, input code range from 12 to 1011. Typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power-On Reset					
Reset Level	MIN for minimum entry level, MAX for maximum release level	2.42	2.6	2.78	V
Hysteresis	Difference between reset release level and entry level		40		mV
Power Consumption					
Normal Operation Mode	V_{CC} = 5V		0.5	0.8	mA
	V_{REF1} = V_{REF2} = 5V		0.1	0.2	
Power-Down Mode	V_{CC} = 5V		0.6	7	μA
	V_{REF1} = V_{REF2} = 5V		0.01	1	

NOTES:

1. Nonlinearity error: The error of the I/O curve deviated from the ideal straight line between output voltages at "#00C" and "#3F3".
2. Differential nonlinearity error: The error deviated from the ideal increment given when the digital value is incremented by one bit.
3. At +125℃, please limit the output current of each channel to 5mA for maximum operating life time.



TIMING CHARACTERISTICS

(V_{CC} = 2.8V to 5.5V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}				40	MHz
SCLK Cycle Time	$1/f_{SCLK}$		25	33		ns
SCLK High Time	t_{CH}		10			ns
SCLK Low Time	t_{CL}		10			ns
$\overline{SYNC}$ Setup Time before SCLK Falling Edge	t_{SS}		3	10	$1/f_{SCLK}$ - 3	ns
Data Setup Time before SCLK Falling Edge	t_{DS} (1)		2.5			ns
Data Hold Time after SCLK Falling Edge	t_{DH} (1)		2.5			ns
$\overline{SYNC}$ Hold Time after the 16th Falling Edge of SCLK	t_{SH}	T_A = +25℃	0	3	$1/f_{SCLK}$ - 3	ns
$\overline{SYNC}$ High Time	t_{SYNC}		5			ns

NOTE: 1. When the internal LDO is enabled and V_{BUS} = V_{CC}, the minimum setup and hold times should be 4ns.

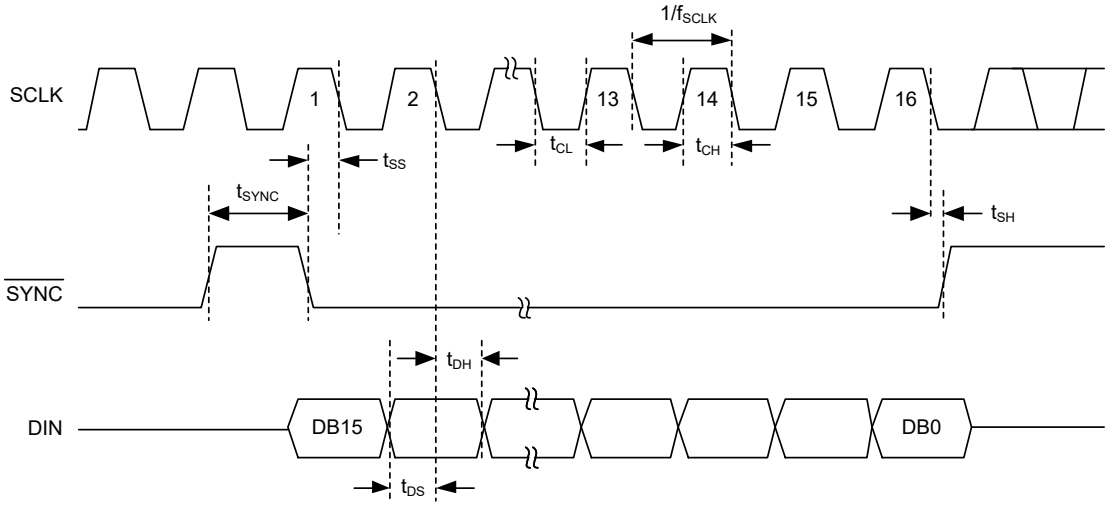
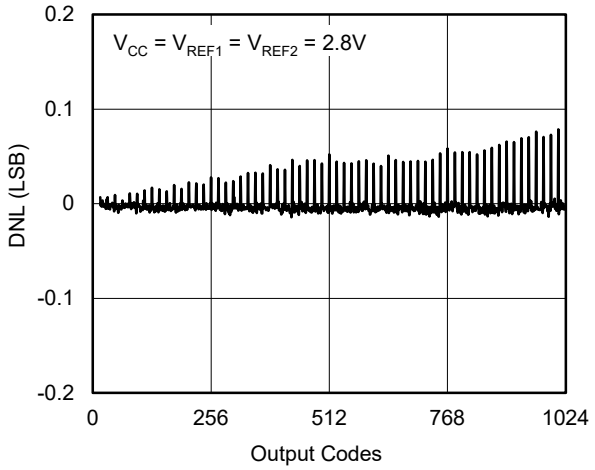


Figure 1. Input/Output Timing Definition

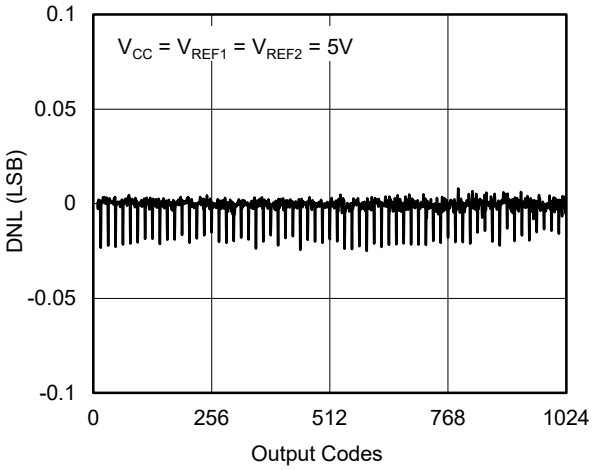
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

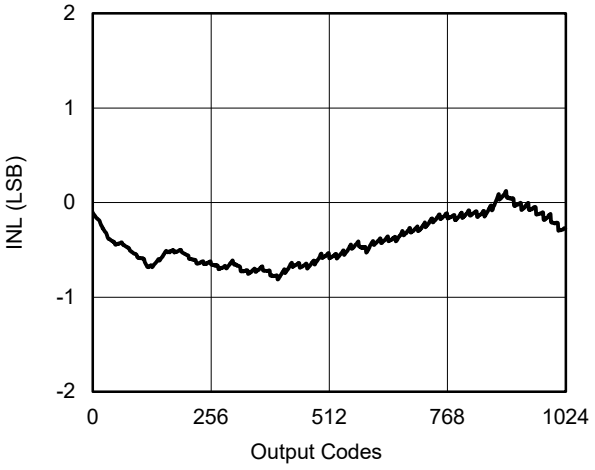
DNL vs. Output Codes



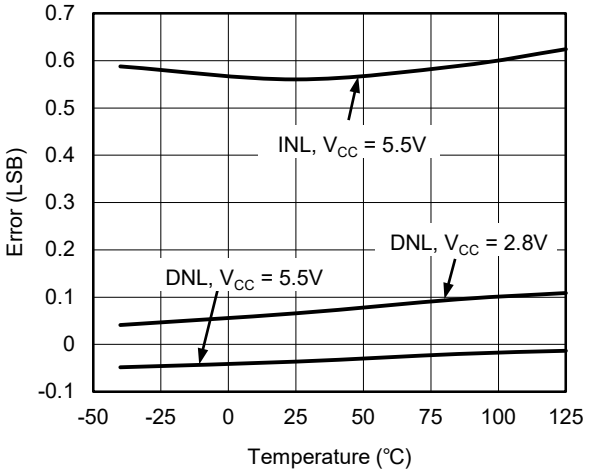
DNL vs. Output Codes



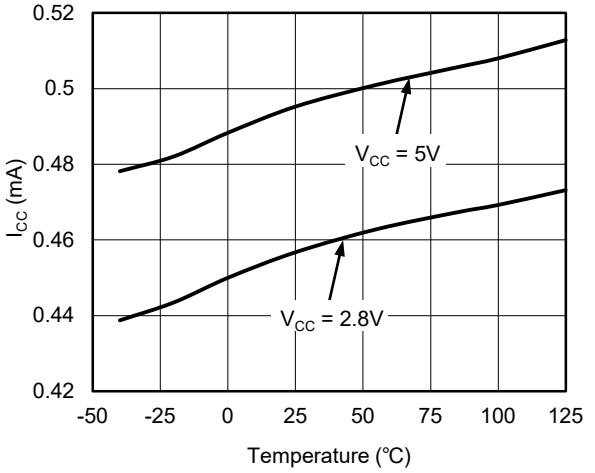
INL vs. Output Codes



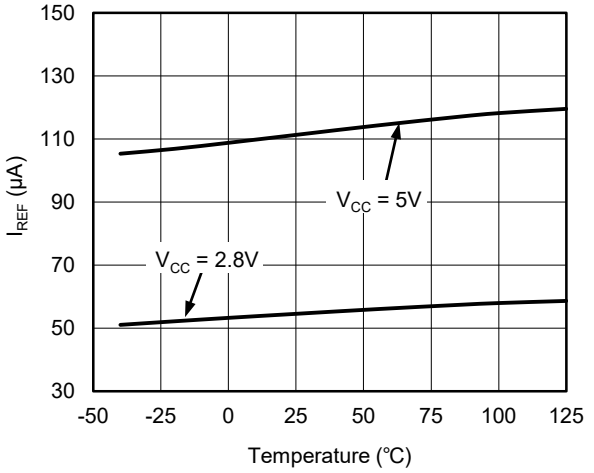
INL and DNL vs. Temperature



I_{CC} vs. Temperature



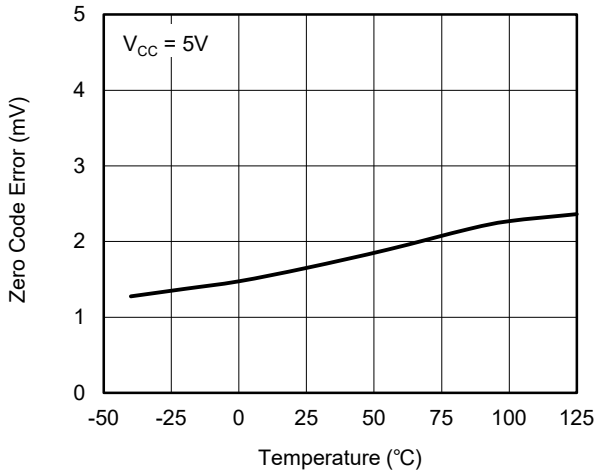
I_{REF} vs. Temperature



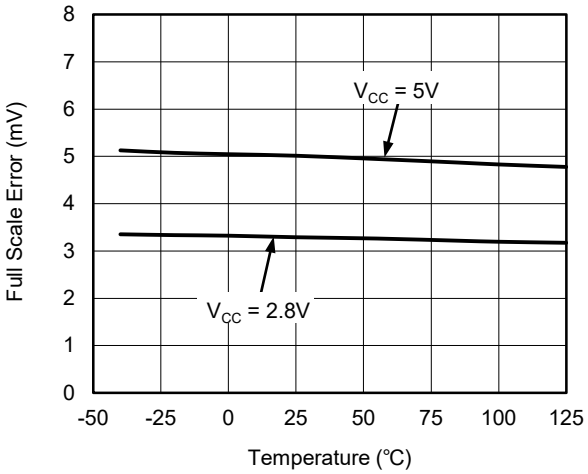
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

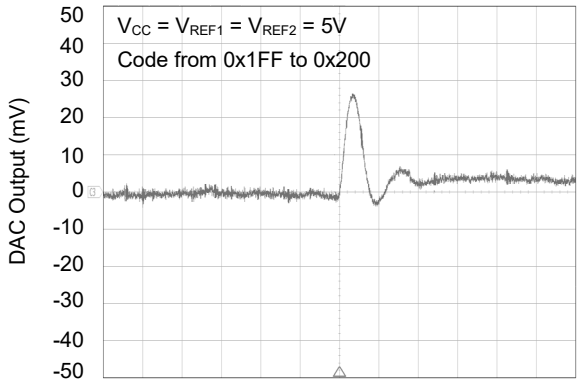
Zero Code Error vs. Temperature



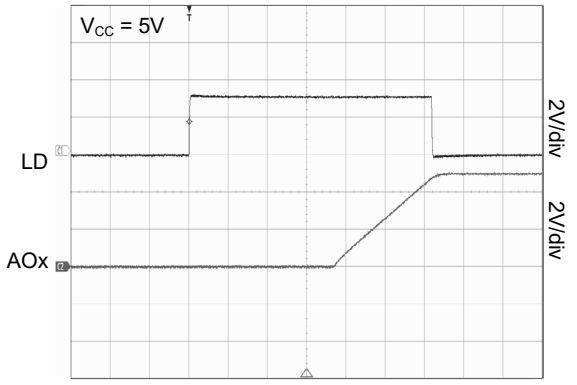
Full Scale Error vs. Temperature



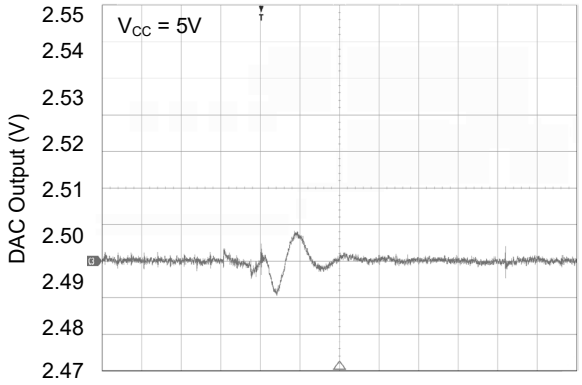
Glitch Response



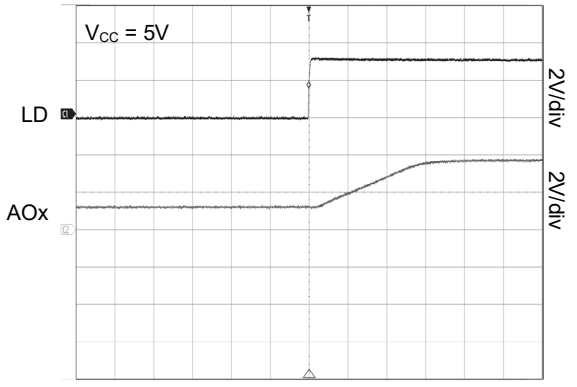
Wake-Up Time



DAC-to-DAC Crosstalk



Settling Time



FUNCTIONAL BLOCK DIAGRAM

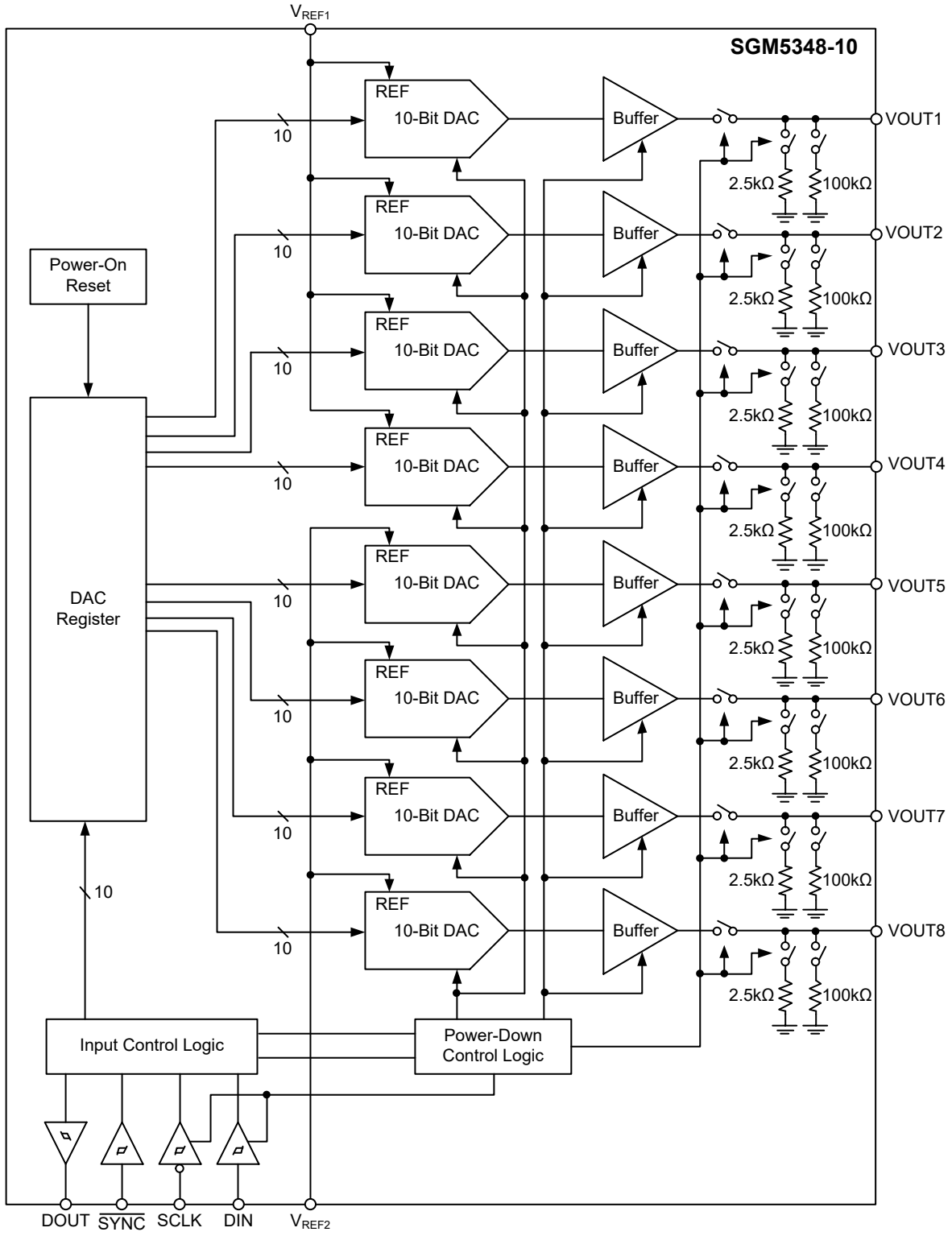


Figure 2. Block Diagram

DETAILED DESCRIPTION

DAC Architecture and Output Amplifiers

The SGM5348-10 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings followed by an output buffer. The reference voltages are externally applied at V_{REF1} for DAC channels 1 through 4, and V_{REF2} for DAC channels 5 through 8.

For simplicity, a single resistor string is shown in Figure 3. This string consists of 1024 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT1, 2, 3, 4} = V_{REF1} \times (D/1024) \quad (1)$$

$$V_{OUT5, 6, 7, 8} = V_{REF2} \times (D/1024) \quad (2)$$

where

D is the decimal equivalent of the binary code that is loaded into the DAC register.

D can take on any value between 0 and 1023. This configuration ensures that the DAC is monotonic.

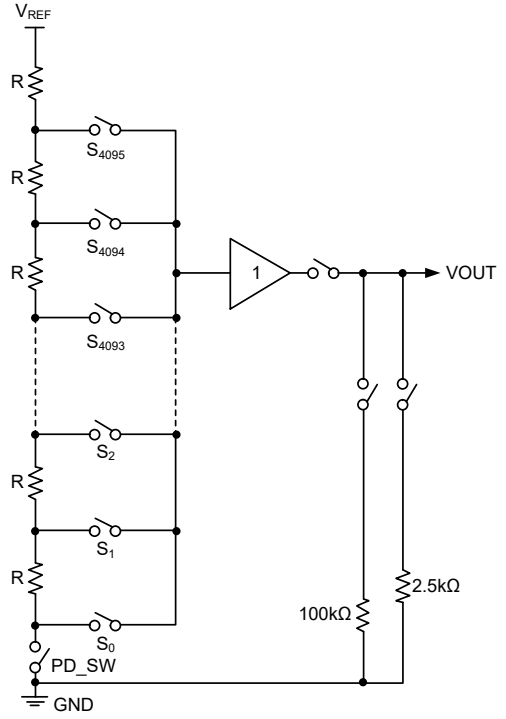


Figure 3. DAC Resistor String

Because all 8 DAC channels of the SGM5348-10 can be controlled independently, each channel consists of a DAC register and a 10-bit DAC. Figure 4 is a simple block diagram of an individual channel in the SGM5348-10. Depending on the mode of operation, data written into a DAC register causes the 10-bit DAC output to be updated, or an additional command is required to update the DAC output. Further description of the modes of operation can be found in Serial Interface section.

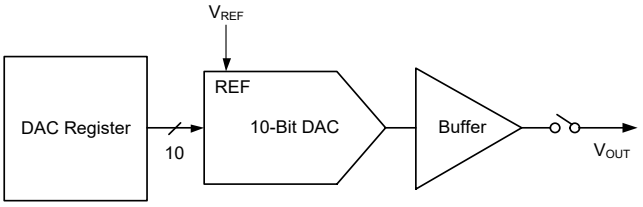


Figure 4. Single-Channel Block Diagram

The output amplifiers are rail-to-rail output, providing an output voltage range of 0V to V_{CC} when the reference is V_{CC}. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_{CC}, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_{CC}, there is only a loss in linearity in the lowest codes.

The output amplifiers are capable of driving a load of 2kΩ in parallel with 1500pF to ground or to V_{CC}. The zero code and full-scale outputs for given load currents are available in the Electrical Characteristics.

DAC string and amplifier can be powered down to kill DC current. The user will see three modes of R_{OUT} at analog output when powering down. (More detailed information will be descripted in Power-Down Mode section.) In the power-down mode, all the DIN/DATA registers are kept unchanged but they may be loaded with new values by the serial port. When power-down is finished, the DAC buffer has a delay to allow internal circuits to recover and the output is slewing back to the value in DATA register in a controlled manner.

DETAILED DESCRIPTION (continued)

Reference Voltage

SGM5348-10 uses dual external references, V_{REF1} and V_{REF2}, which are shared by channels 1 to 4 and channels 5 to 8, respectively. The reference voltage range is 0.5V to V_{CC}, providing the widest possible output dynamic range.

Serial Interface

The three-wire interface is compatible with SPI, QSPI, and MICROWIRE buses, and operates at clock rates up to 40MHz. The interface is made up of SCLK, DIN, DOUT and $\overline{SYNC}$ pins. A valid serial frame contains 16 falling edges of SCLK. See Figure 1 for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the DIN line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid mis-clocking data into the shift register, it is critical that $\overline{SYNC}$ not be brought low on a falling edge of SCLK (see minimum and maximum setup times for $\overline{SYNC}$ in Figure 5). On the 16th falling edge of SCLK, the last data bit is clocked into the register. The write sequence is concluded by bringing the $\overline{SYNC}$ line high. Once $\overline{SYNC}$ is high, the programmed function (a change in the DAC channel address, mode of operation, or register contents) is executed. To avoid mis-clocking data into the shift register, it is critical that $\overline{SYNC}$ be brought high between the 16th and 17th falling edges of SCLK.

If $\overline{SYNC}$ is brought high before the 15th falling edge of SCLK, the write sequence is aborted and the data that has been shifted into the input register is discarded. If $\overline{SYNC}$ is held low beyond the 17th falling edge of SCLK, the serial data presented at DIN will begin to be output on DOUT. In either case, $\overline{SYNC}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{SYNC}$.

$\overline{SYNC}$ should be idled high to avoid the activation of daisy-chain operation where DOUT is active.

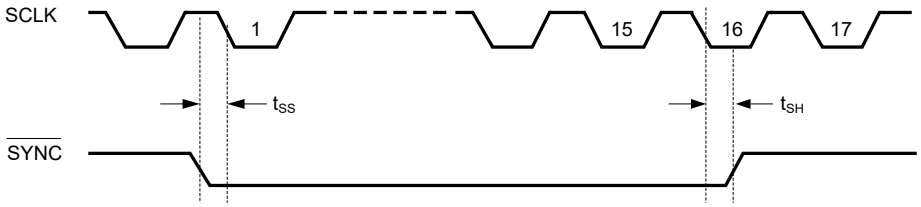


Figure 5. $\overline{SYNC}$ Setup and Hold Times

DETAILED DESCRIPTION (continued)

Daisy-Chain Operation

Daisy-chain operation allows communication with any number of SGM5348-10s using a single serial interface. As long as the correct number of data bits are input in a write sequence (multiple of 16 bits), a rising edge of $\overline{SYNC}$ properly updates all DACs in the system.

To support multiple devices in a daisy-chain configuration, SCLK and $\overline{SYNC}$ are shared across all SGM5348-10s and DOUT of the first DAC in the chain is connected to DIN of the second. Figure 6 shows three SGM5348-10s connected in daisy-chain fashion. Similar to a single-channel write sequence, the conversion for a daisy-chain operation begins on a falling edge of $\overline{SYNC}$ and ends on a rising edge of $\overline{SYNC}$. A valid write sequence for n devices in a chain requires n times 16 falling edges to shift the entire input data stream through the chain. Daisy-chain operation is specified for a maximum SCLK speed of 40MHz.

The serial data output pin, DOUT, is available on the SGM5348-10 to allow daisy-chaining of multiple SGM5348-10 devices in a system. In a write sequence, DOUT remains low for the first 14 falling edges of SCLK before going high on the 15th falling edge. Subsequently, the next 16 falling edges of SCLK output the first 16 data bits entered into DIN. Figure 7 shows the timing of three SGM5348-10s in Figure 6. In this instance, it takes 48 falling edges of SCLK followed by a rising edge of SYNC to load all three SGM5348-10s with the appropriate register data. On the rising edge of $\overline{SYNC}$, the programmed function is executed in each SGM5348-10 simultaneously.

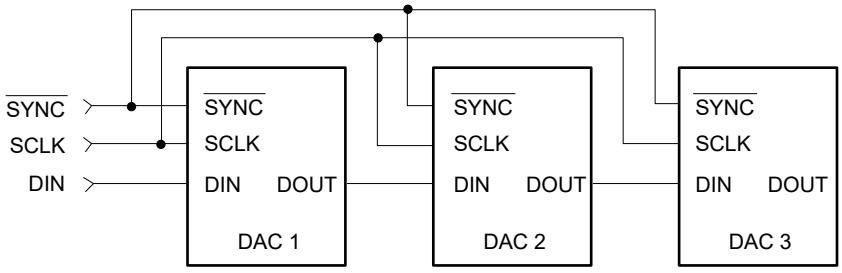


Figure 6. Daisy-Chain Configuration

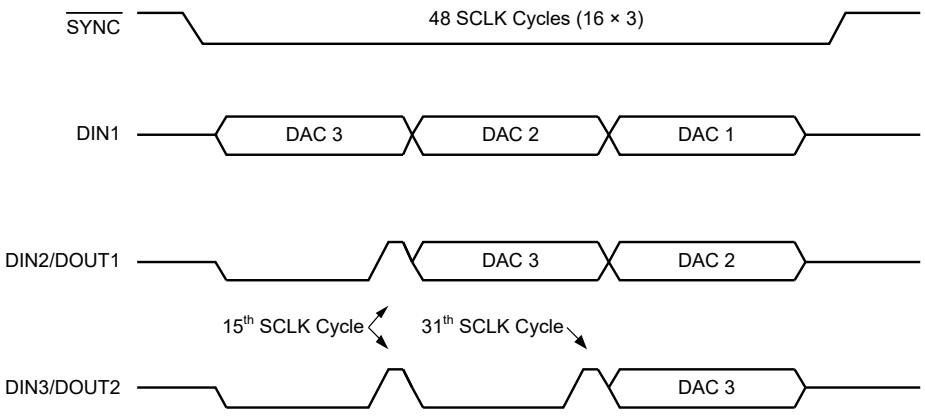


Figure 7. Daisy-Chain Timing Diagram

REGISTER DEFINITION

Shifter Register Format

The DIN is sampled by the falling edge of SCLK and shifted to a shift register. DOUT is connected to serial output of the shift register and is updated at falling edge of SCLK. The format of shifter register is shown below as an example. The lower 2 bits DB[1:0] will be added by 0 or 1 (X) code.

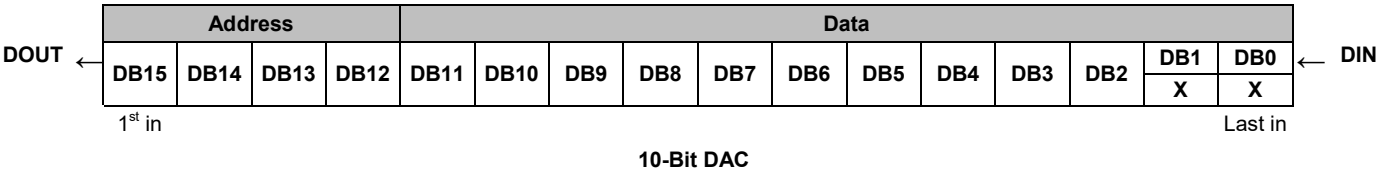


Figure 8. Serial Data

The upper 4 bits are always for address. The next 10 bits are for data respectively. MSB is streamed in first. The lower 2 bits will be ignored by SGM5348-10.

Register Address

Address				Address Selected
DB15	DB14	DB13	DB12	
0	0	0	0	Channel 1 Data Register.
0	0	0	1	Channel 2 Data Register.
0	0	1	0	Channel 3 Data Register.
0	0	1	1	Channel 4 Data Register.
0	1	0	0	Channel 5 Data Register.
0	1	0	1	Channel 6 Data Register.
0	1	1	0	Channel 7 Data Register.
0	1	1	1	Channel 8 Data Register.
1	0	0	0	Write Register Mode (WRM).
1	0	0	1	Write Through Mode (WTM).
1	0	1	0	Update Select or LDO Select.
1	0	1	1	CH1 Write Mode.
1	1	0	0	Broadcast Mode.
1	1	0	1	Hi-Z Outputs.
1	1	1	0	100kΩ Outputs.
1	1	1	1	2.5kΩ Outputs.

REGISTER DESCRIPTION

DAC Input Data Update Mechanism

The SGM5348-10 has two modes of operation plus a few special command operations. The two modes of operation are Write Register Mode (WRM) and Write Through Mode (WTM). For the rest of this document, these modes are referred to as WRM and WTM. The special command operations are separate from WRM and WTM because they can be called upon regardless of the current mode of operation. The mode of operation is controlled by the first 4 bits of the control register, DB15 through DB12. See Table 1 for a detailed summary.

After the SGM5348-10 powers up, the DAC is in WRM. In WRM, the registers of each individual DAC channel can be written to without causing the DAC outputs to be updated. This is accomplished by setting DB[15] to 0, specifying the DAC register to be written to in DB[14:12], and entering the new DAC register setting in DB[11:0] (see Table 2). The SGM5348-10 remains in WRM until the mode of operation is changed to WTM. The mode of operation is changed from WRM to WTM by setting DB[15:12] to 1001. The DB[11:0] should all be 0 when writing 1001 to DB[15:12]. Once in WTM, writing data to a DAC channel's register causes the DAC's output to be updated as well. Changing a DAC channel's register in WTM is accomplished in the same manner as it is done in WRM. However, in WTM the DAC's register and output are updated at the completion of the command (see Table 2). Similarly, the SGM5348-10 remains in WTM until the mode of operation is changed to WRM by setting DB[15:12] to 1000.

Table 1. Write Register and Write Through Modes

DB[15:12]	DB[11:0]												Description of Mode
1000	0	0	0	0	0	0	0	0	0	0	0	0	WRM: The registers of each DAC channel can be written to without causing their outputs to change.
1001	0	0	0	0	0	0	0	0	0	0	0	0	WTM: Writing data to a channel's register causes the DAC output to change.

Table 2. Commands Impacted by WRM and WTM

DB[15]	DB[14:12]	DB[11:0]												Description of Mode
0	000	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH1's data register only. WTM: CH1's output is updated by data in D[11:0].
0	001	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH2's data register only. WTM: CH2's output is updated by data in D[11:0].
0	010	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH3's data register only. WTM: CH3's output is updated by data in D[11:0].
0	011	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH4's data register only. WTM: CH4's output is updated by data in D[11:0].
0	100	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH5's data register only. WTM: CH5's output is updated by data in D[11:0].
0	101	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH6's data register only. WTM: CH6's output is updated by data in D[11:0].
0	110	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH7's data register only. WTM: CH7's output is updated by data in D[11:0].
0	111	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	WRM: D[11:0] written to CH8's data register only. WTM: CH8's output is updated by data in D[11:0].

REGISTER DESCRIPTION (continued)

As mentioned previously, the special command operations can be exercised at any time regardless of the mode of operation. There are three special command operations. The first command is exercised by setting data bits DB[15:12] to 1010. This allows user to update multiple DAC outputs simultaneously to the values currently loaded in their respective control registers, and it also controls internal LDO that allows bus voltage to be lower than V_{CC} without causing leakage. Update select feature is valuable if user wants each DAC output to be at a different output voltage but still has all the DAC outputs change to their appropriate values simultaneously. Internal LDO helps when this part is powered at 5V and is directly controlled by a 3V MCU. The details will be introduced in Table 3.

The second special command allows the user to alter the DAC output of CH1 with a single write frame. This command is exercised by setting data bits DB[15:12] to 1011 and data bits DB[11:0] to the desired control register value. It also has the added benefit of causing the DAC outputs of the other channels to update to their current control register values as well. A user may choose to exercise this command to save a write sequence. For example, the user may wish to update several DAC outputs simultaneously, including CH1. To accomplish this task in the minimum number of write frames, the user would alter the control register values of all the DAC channels except CH1 while operating in WRM. The last write frame would be used to exercise the special command CH1 Write Mode. In addition to updating CH1's control register and output to a new value, all of the other channels would be updated as well. At the end of this sequence of write frames, the SGM5348-10 would still be operating in WRM (see Table 3).

The third special command allows the user to set all the DAC control registers and outputs to the same level. This command is commonly referred to as Broadcast Mode because the same data bits are being broadcast to all of the channels simultaneously. This command is exercised by setting data bits DB[15:12] to 1100 and data bits DB[11:0] to the value that the user wishes to broadcast to all the DAC control registers. Once the command is exercised, each DAC output is updated by the new control register value. This command is frequently used to set all the DAC outputs to some known voltage such as 0V, $V_{REF}/2$, or Full Scale. A summary of the commands can be found in following Table 3.

Table 3. Special Command Operations

DB[15:12]	DB[11:0]												Description of Mode
1010	LDO1	LDO0	X	X	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	Update Select: The DAC outputs of the channels selected with a 1 in DB[7:0] are updated simultaneously to the values in their respective control registers. LDO Select: LDO[1:0] = 00 (default): Internal LDO is disabled. LDO[1:0] = 10: The internal LDO will be enabled. LDO output voltage is 2.5V, in order to access the bus signal of 2.7V, and then V_{BUS} can be lower than V_{CC} without leakage.
1011	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	CH1 Write Mode: The control register of CH1 and DAC output is updated to the data in DB[11:0]. The outputs of the other seven channels are also updated according to their respective control register values.
1100	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	X	X	Broadcast Mode: The data in DB[11:0] is written to all channels' control register and DAC output simultaneously.

REGISTER DESCRIPTION (continued)

Device Functional Modes

Power-On Reset

At power-up, an internal POR monitors the V_{CC} and gives a reset. The DIN/DATA are reset to 0 so that DAC output starts from a known value before the user loads value to the DAC register. When V_{CC} is less than the minimum working voltage of the POR, the amplifier only has very weak drive capability and the feedback resistor pulls the output low. During the whole power-up process, the DAC outputs remain at 0V.

Power-Down Modes

SGM5348-10 has three power-down modes where different output terminations can be selected (see Table 4). When all channels are in power-down state, the supply current drops to 0.5μA at 3V and 0.6μA at 5V. By selecting the channels to be powered down in DB[7:0] with a 1, individual channels can be powered down separately, or multiple channels can be powered down simultaneously. The three different output terminations include high output impedance, 100kΩ to ground, and 2.5kΩ to ground.

When one channel is powered down, the power-down switch of DAC core and buffer is OFF so that no current is consumed by DAC and buffer. The bias generator, however, is only shut down if all the channels are placed in power-down mode. The contents of the DAC registers are unaffected when in power-down. Therefore, each DAC register maintains its value before the SGM5348-10 is powered down unless it is changed during the write sequence which instructs it to recover from power-down. Minimum power consumption is achieved in the power-down mode with $\overline{SYNC}$ idled high, DIN idled low, and SCLK disabled.

The serial interface is not affected by the power-down. If DIN and DATA of a powered down channel are not programmed, then the value before power-down is kept unchanged. But user can also choose to write new value for the powered down channel.

There is maximum 20μs for the channel to recover. The output of DAC buffer will slew from GND to the value in DAC_REG with a controlled manner.

When all the 8 channels are powered down, the only block that consumes current is the POR.

Table 4. Power-Down Modes

DB[15:12]	DB[11:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Output Impedance
1101	XXXX	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	Hi-Z Outputs
1110	XXXX	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	100kΩ Outputs
1111	XXXX	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	2.5kΩ Outputs

APPLICATION INFORMATION

Bipolar Operation

The SGM5348-10 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be achieved with the circuit in Figure 9. This circuit will provide an output voltage range of ±5V. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5V.

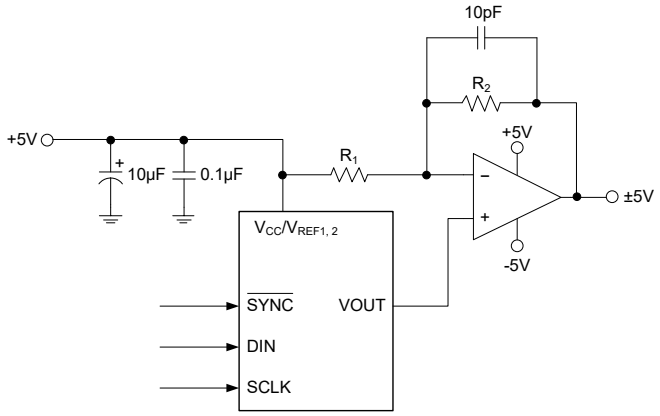


Figure 9. Bipolar Operation

The output voltage of this circuit for any code is found to be

$V_{OUT} = V_{CC} \times (D/1024) \times ((R_1 + R_2)/R_1) - V_{CC} \times R_2/R_1$ (3)

where D is the input code in decimal form.

With V_{CC} = 5V and $R_1 = R_2$

$$V_{OUT} = (10 \times D/1024) - 5V \quad (4)$$

Programmable Attenuator

Figure 10 shows one of the channels of the SGM5348-10 being used as a single-quadrant multiplier. In this configuration, an AC or DC signal can be driven into one of the reference pins. The SPI interface of the DAC can be used to digitally attenuate the signal to any level from 0dB (full scale) to 0V. This is accomplished without adding any noticeable level of noise to the signal. An amplifier stage is shown as a reference for applications where the input signal requires amplification. Note how the AC signal in this application is AC-coupled to the amplifier before being amplified. A separate bias voltage is used to set the common-mode voltage for the SGM5348-10's reference input to $V_{CC}/2$, allowing the largest possible input swing. The multiplying bandwidth of V_{REF1}/V_{REF2} is 300kHz with a V_{CM} of 2.5V and a peak-to-peak signal swing of 2V.

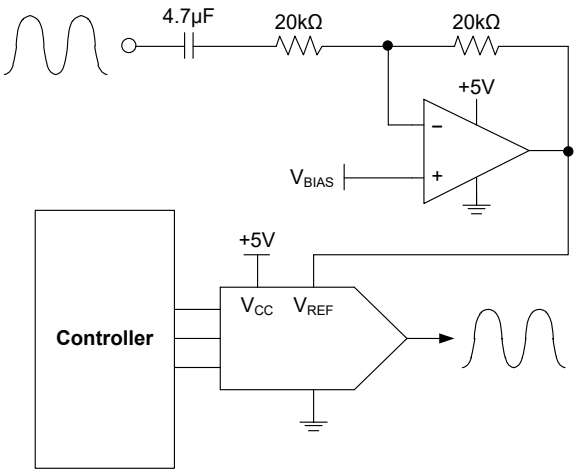


Figure 10. Programmable Attenuator

INDUSTRIAL APPLICATION

Figure 11 shows the SGM5348-10 controlling several different circuits in an industrial setting. Channel 1 is shown providing the reference voltage to the ADC. The reference may be set to any voltage from 0.2V to 5.5V, providing the widest dynamic range possible. Typically, the ADC will be monitoring a sensor and would benefit from the ADC's reference voltage being adjustable. Channel 2 is providing the drive or supply voltage for a sensor. By having the sensor supply voltage adjustable, the output of the sensor can be optimized to the input level of the ADC monitoring it. Channel 3 is defined to adjust the offset or gain of an amplifier stage in the system. Channel 4 is configured with an operational amplifier to provide an adjustable current source. Being able to convert one of the 8 channels of the SGM5348-10 to a current output eliminates the need for a separate current output DAC to be added to the circuit. Channel 5, in conjunction with an operational amplifier, provides a bipolar output swing for devices requiring control voltages that are centered on ground. Channel 6 and 7 are used to set the upper and lower limits for a range detector. Channel 8 is reserved for providing voltage control or acting as a voltage setpoint.

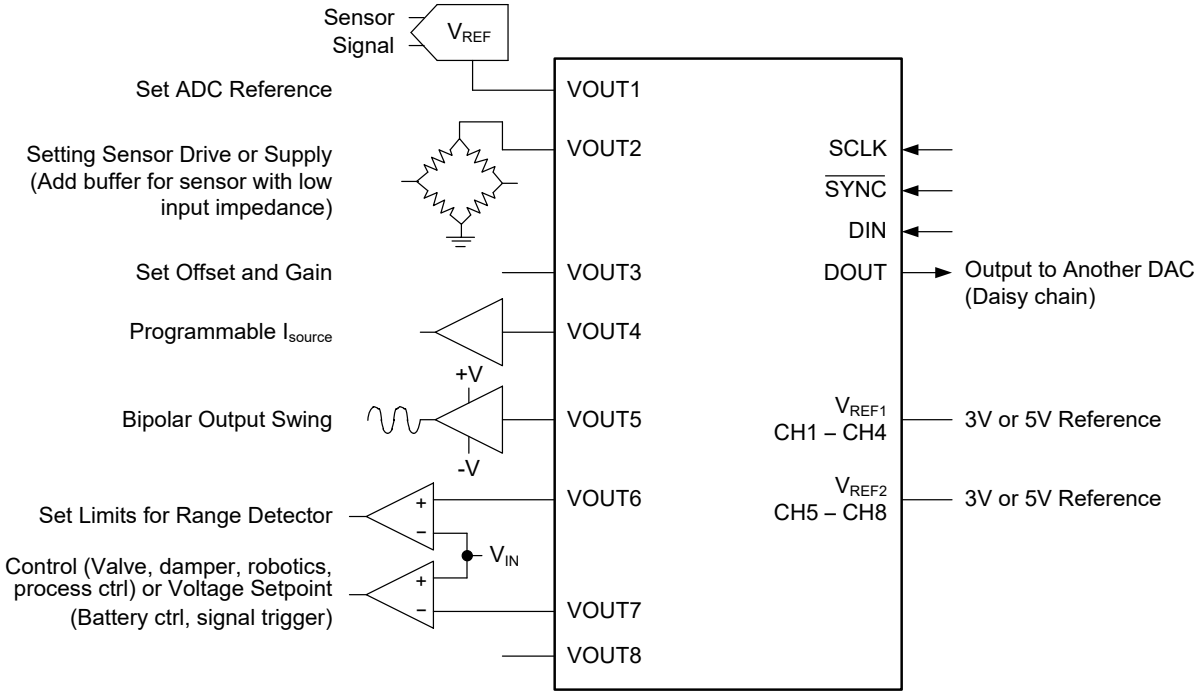


Figure 11. Industrial Application

LAYOUT GUIDELINES

For best accuracy and minimum noise, the printed-circuit board containing the SGM5348-10 must have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes must be located in the same board layer. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design uses a fencing technique to prevent the mixing of analog and digital ground currents. Separate ground planes must only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the SGM5348-10. Take special care to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

For best performance, the SGM5348-10 power supply must be bypassed with at least a 1μF and a 0.1μF capacitors. The 0.1μF capacitor must be placed right at the device supply pin. The 1μF or larger valued capacitor can be a tantalum capacitor while the 0.1μF capacitor must be a ceramic capacitor with low ESL and low ESR. If a ceramic capacitor with low ESL and low ESR is used for the 1μF value and it can be placed right at the supply pin, the 0.1μF capacitor can be eliminated. Capacitors of this nature typically span the same frequency spectrum as the 0.1μF capacitor and thus eliminate the need for the extra capacitor. The power supply for the SGM5348-10 must only be used for analog circuits.

It is also advisable to avoid the crossover of analog and digital signals. This helps minimize the amount of noise from the transitions of the digital signals from coupling onto the sensitive analog signals such as the reference pins and the DAC outputs.

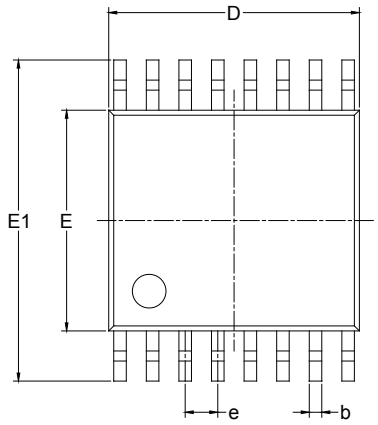
REVISION HISTORY

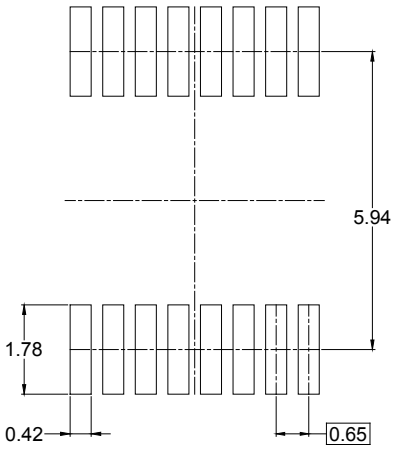
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2019) to REV.A	Page
Changed from product preview to production data	All

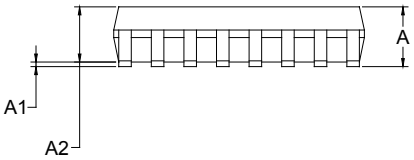
PACKAGE OUTLINE DIMENSIONS

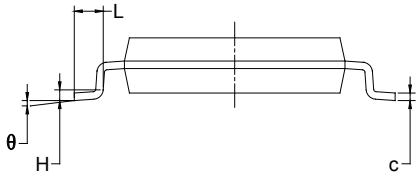
TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

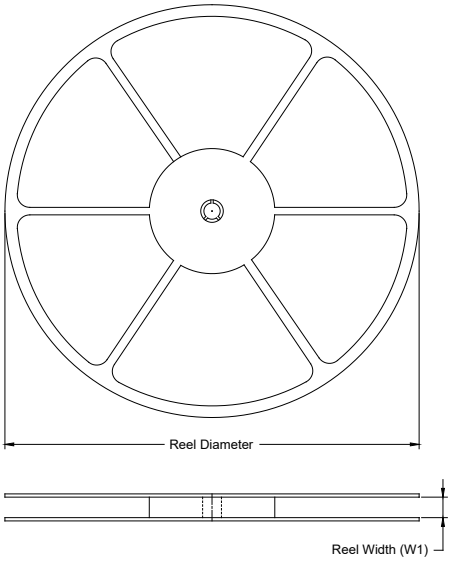




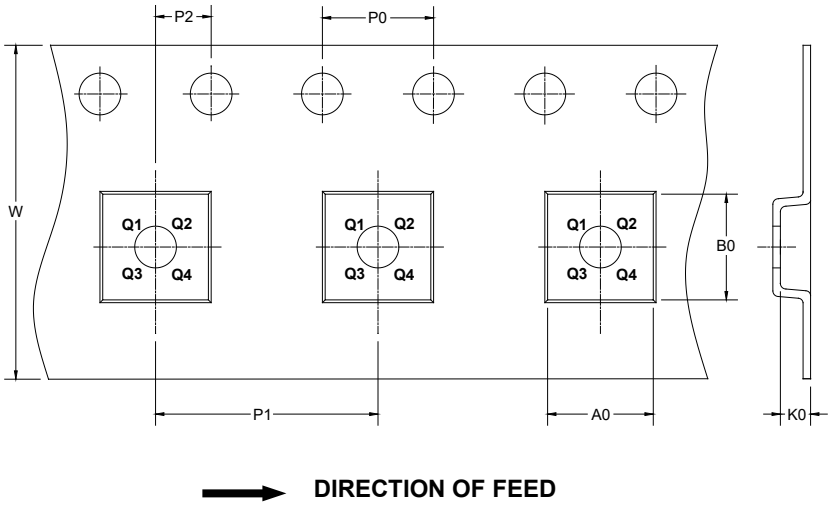
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



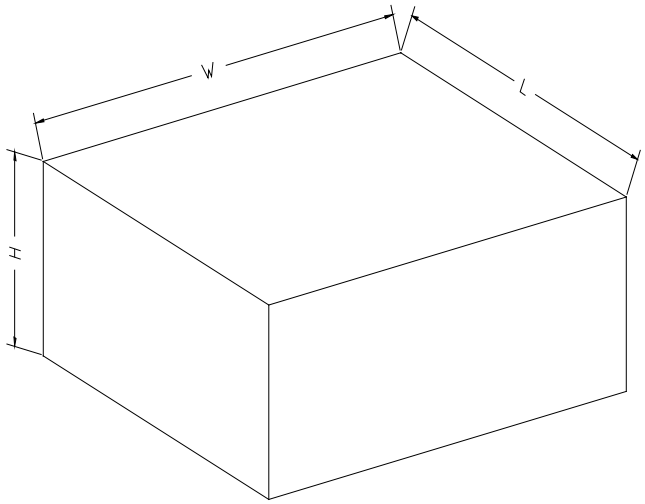
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002