SGM5349A-16
8-CH, 16-Bit, SPI Interface, Voltage-Output DAC

GENERAL DESCRIPTION

The SGM5349A-16 is a low power, 8 channels, 16-bit, buffered voltage-output DAC. It operates from a single 2.7V to 5.5V supply and the monotonicity is guaranteed by design. The SGM5349A-16 has no internal voltage reference, and the full-scale output range is V_{REF}.

The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0V and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 1μA at 5.5V and provides software-selectable output loads while in power-down mode for any or all DAC channels. The outputs can be updated simultaneously using the $\overline{\text{LDAC}}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{\text{CLR}}$ that updates DAC to a user-programmable code: zero scale, midscale, or full scale.

The SGM5349A-16 utilizes a versatile 3-wire serial interface that operates at clock rates of up to 50MHz and is compatible with standard SPI, QSPI, DSP and MICROWIRE interface standards. The on-chip precision output amplifier enables rail-to-rail output swing.

The SGM5349A-16 is available in Green TSSOP-16 and TQFN-4×4-16L packages.

FEATURES

- **Low Power, Small Footprint, Pin-Compatible, 8 Channels, 16-Bit DAC**
- **Power Down to 1μA at 5.5V**
- **2.7V to 5.5V Power Supply**
- **Monotonicity Guaranteed by Design**
- **Power-On Reset to Zero Scale**
- **3 Power-Down Functions**
- **Hardware $\overline{\text{LDAC}}$ and $\overline{\text{LDAC}}$ Override Function**
- **$\overline{\text{CLR}}$ Function to Programmable Code**
- **Rail-to-Rail Buffered Voltage-Output Operation**
- **Selectable 1.8V Bus Voltage Support Version can be Provided by Request**
- **Available in Green TSSOP-16 and TQFN-4×4-16L Packages**

APPLICATIONS

Process Control
Data Acquisition Systems
Portable Battery-Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

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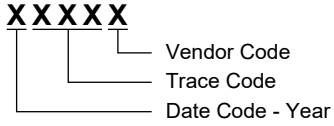
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5349A-16	TSSOP-16	-40℃ to +125℃	SGM5349A-16XTS16G/TR	SGMCEF XTS16 XXXXX	Tape and Reel, 4000
	TQFN-4×4-16L	-40℃ to +125℃	SGM5349A-16XTQE16G/TR	SGMCED XTQE16 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to 6.5V
Digital Input Voltage to GND ..... -0.3V to V_{DD} + 0.3V
V_{OUT} to GND ..... -0.3V to V_{DD} + 0.3V
V_{REFIN}/V_{REFOUT} to GND ..... -0.3V to V_{DD} + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

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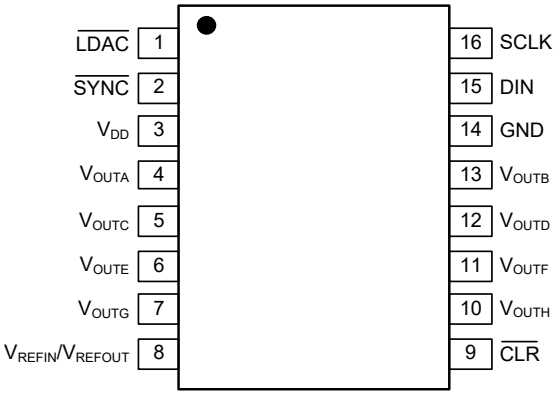
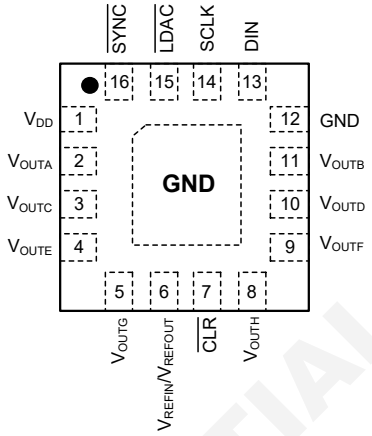
PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-16

(TOP VIEW)



TQFN-4×4-16L

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP-16	TQFN-4×4-16L		
1	15	$\overline{LDAC}$	Pulsing this pin low allows DAC registers to be updated if the input registers have new data. This allows DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
2	16	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{SYNC}$ is taken high before the 32nd falling edge, the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the device.
3	1	V_{DD}	Power Supply Input. This part can be operated from 2.7V to 5.5V, and the supply should be decoupled with a 10μF capacitor in parallel with a 0.1μF capacitor to GND.
4	2	V_{OUTA}	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	3	V_{OUTC}	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	4	V_{OUTE}	Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
7	5	V_{OUTG}	Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
8	6	V_{REFIN}/ V_{REFOUT}	The SGM5349A-16 has a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
9	7	$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{CLR}$ code register: zero, midscale, or full scale. Default setting clears the output to 0V.
10	8	V_{OUTH}	Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
11	9	V_{OUTF}	Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
12	10	V_{OUTD}	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
13	11	V_{OUTB}	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
14	12	GND	Ground Reference Point for All Circuitry on the Part.
15	13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
16	14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50MHz.
–	Exposed Pad	GND	It is recommended that the exposed paddle be soldered to the ground plane.

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ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{DD}, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Static Performance (1)						
Resolution			16			Bits
Relative Accuracy				8		LSB
Differential Nonlinearity		Monotonicity guaranteed by design		±0.4		LSB
Zero-Code Error		All 0s loaded to DAC register		1.5		mV
Zero-Code Error Drift						μV/℃
Full-Scale Error		All 1s loaded to DAC register		0.4		% FSR
Gain Error				0.4		% FSR
Gain Temperature Coefficient		Of FSR/℃				ppm
Offset Error				1.5		mV
DC Power Supply Rejection Ratio		V_{DD} ± 10%		-90		dB
DC Crosstalk		Due to full-scale output change, R_L = 2kΩ to GND or V_{DD}		10		μV
		Due to load current change		25		μV/mA
		Due to powering down (per channel)		10		μV
Output Characteristics (2)						
Output Voltage Range			0		V_{DD}	V
Capacitive Load Stability		R_L = ∞		2		nF
		R_L = 2kΩ		10		
DC Output Impedance				0.1		Ω
Short-Circuit Current		V_{DD} = 5V		35		mA
Power-Up Time		Coming out of power-down mode, V_{DD} = 5V				μs
Reference Inputs						
Reference Current		V_{REF} = V_{DD} = 5.5V (per DAC channel)		24		μA
Reference Input Range			0		V_{DD}	V
Reference Input Impedance				28		kΩ
Logic Inputs (2)						
Input Current		All digital inputs		0.1		μA
Input Low Voltage, V_{IL}					0.7	V
Input High Voltage, V_{IH}			2.5			V
Pin Capacitance				3		pF
Power Requirements						
Power Supply Range, V_{DD}		All digital inputs at 0 or V_{DD}, DAC active, excludes load current	2.7		5.5	V
Normal Mode (3)	I_{DD}			0.8		mA
All Power-Down Modes (4)				1		μA

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NOTES:
1. Linearity calculated using a reduced code range of SGM5349A-16 (Code 512 to 65,024). Output unloaded.
2. Guaranteed by design and characterization; not production tested.
3. Interface inactive. All DACs active. DAC outputs unloaded.
4. All eight DACs powered down.

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{DD}, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Settling Time	¼ to ¾ scale settling to ±2 LSB (16-bit resolution)			TBD		μs
Slew Rate				TBD		V/μs
Digital-to-Analog Glitch Impulse	1 LSB (16-bit resolution) change around major carry			TBD		nV-s
	From code 0xEA00 to code 0xE9FF (16-bit resolution)			TBD		
Digital Feedthrough				TBD		nV-s
Digital Crosstalk				TBD		nV-s
Analog Crosstalk				TBD		nV-s
DAC-to-DAC Crosstalk				TBD		nV-s
Multiplying Bandwidth	V_{REF} = 2V ± 0.2Vp-p			TBD		kHz
Total Harmonic Distortion	V_{REF} = 2V ± 0.1Vp-p, frequency = 10kHz			TBD		dB
Output Noise Spectral Density	DAC code = 0x8400 (16-bit resolution)	1kHz		TBD		nV/√Hz
		10kHz		TBD		nV/√Hz
Output Noise	0.1Hz to 10Hz, DAC code = 0x0000			TBD		μVp-p

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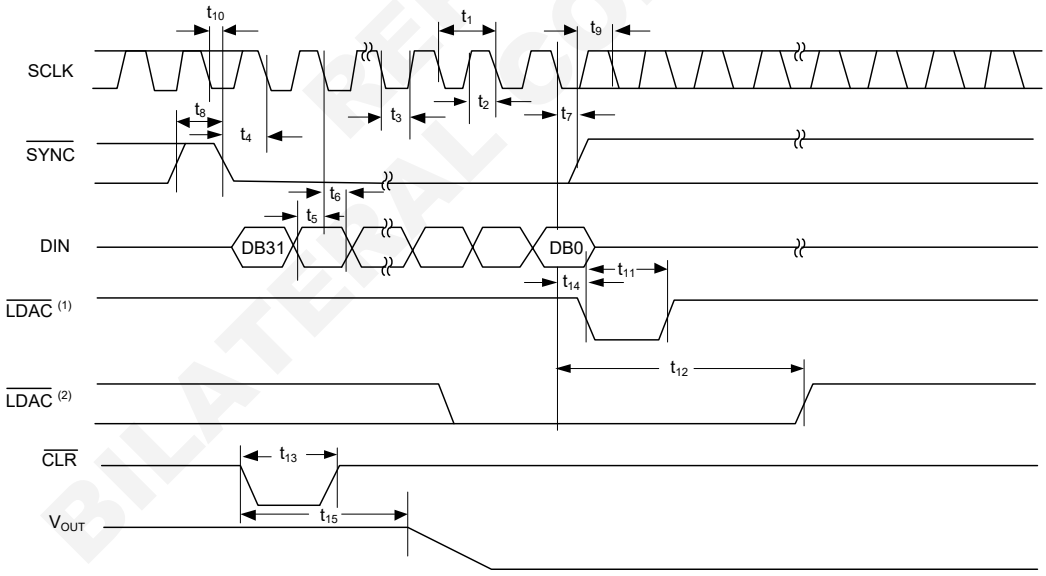
TIMING CHARACTERISTICS

(All input signals are specified with $t_r = t_f$ = 1ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 1. V_{DD} = 2.7V to 5.5V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Cycle Time	t_1 (1)		20			ns
SCLK High Time	t_2		8			ns
SCLK Low Time	t_3		8			ns
$\overline{SYNC}$ to SCLK Falling Edge Setup Time	t_4		13			ns
Data Setup Time	t_5		4			ns
Data Hold Time	t_6		4			ns
SCLK falling Edge to $\overline{SYNC}$ Rising Edge	t_7		0			ns
Minimum $\overline{SYNC}$ High Time	t_8		15			ns
$\overline{SYNC}$ Rising Edge to SCLK Fall Ignore	t_9		13			ns
SCLK Falling Edge to $\overline{SYNC}$ Fall Ignore	t_{10}		0			ns
$\overline{LDAC}$ Pulse Width Low	t_{11}		10			ns
SCLK Falling Edge to $\overline{LDAC}$ Rising Edge	t_{12}		15			ns
$\overline{CLR}$ Pulse Width Low	t_{13}		5			ns
SCLK Falling Edge to $\overline{LDAC}$ Falling Edge	t_{14}		0			ns
$\overline{CLR}$ Pulse Activation Time	t_{15}			300		ns

NOTE:
1 Maximum SCLK frequency is 50MHz at V_{DD} = 2.7V to 5.5V. Guaranteed by design and characterization; not production tested.



NOTES:
1. Asynchronous Load Update Mode.
2. Synchronous Load Update Mode.

Figure 1. Serial Write Operation

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TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line extracted from best-fit method.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Offset Error
Offset error is a measure of the difference between the actual V_{OUT} and the ideal V_{OUT}, expressed in millivolts in the linear region of the transfer function. Offset error is measured on the SGM5349A-16 with Code 512 loaded into the DAC register. It can be negative or positive and is expressed in millivolts.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded into the DAC register. Ideally, the output should be 0V. The zero-code error is always positive in the SGM5349A-16, because the output of the DAC cannot go below 0V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in μV/℃.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/℃.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{DD} - 1 LSB. Full-scale error is expressed as a percentage of the full-scale range.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2V, and VDD is varied ±10%.

DC Crosstalk
DC crosstalk is the DC change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nV-s and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

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TERMINOLOGY (continued)

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high, and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3dB below the input.

Total Harmonic Distortion (THD)

Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

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FUNCTIONAL BLOCK DIAGRAM

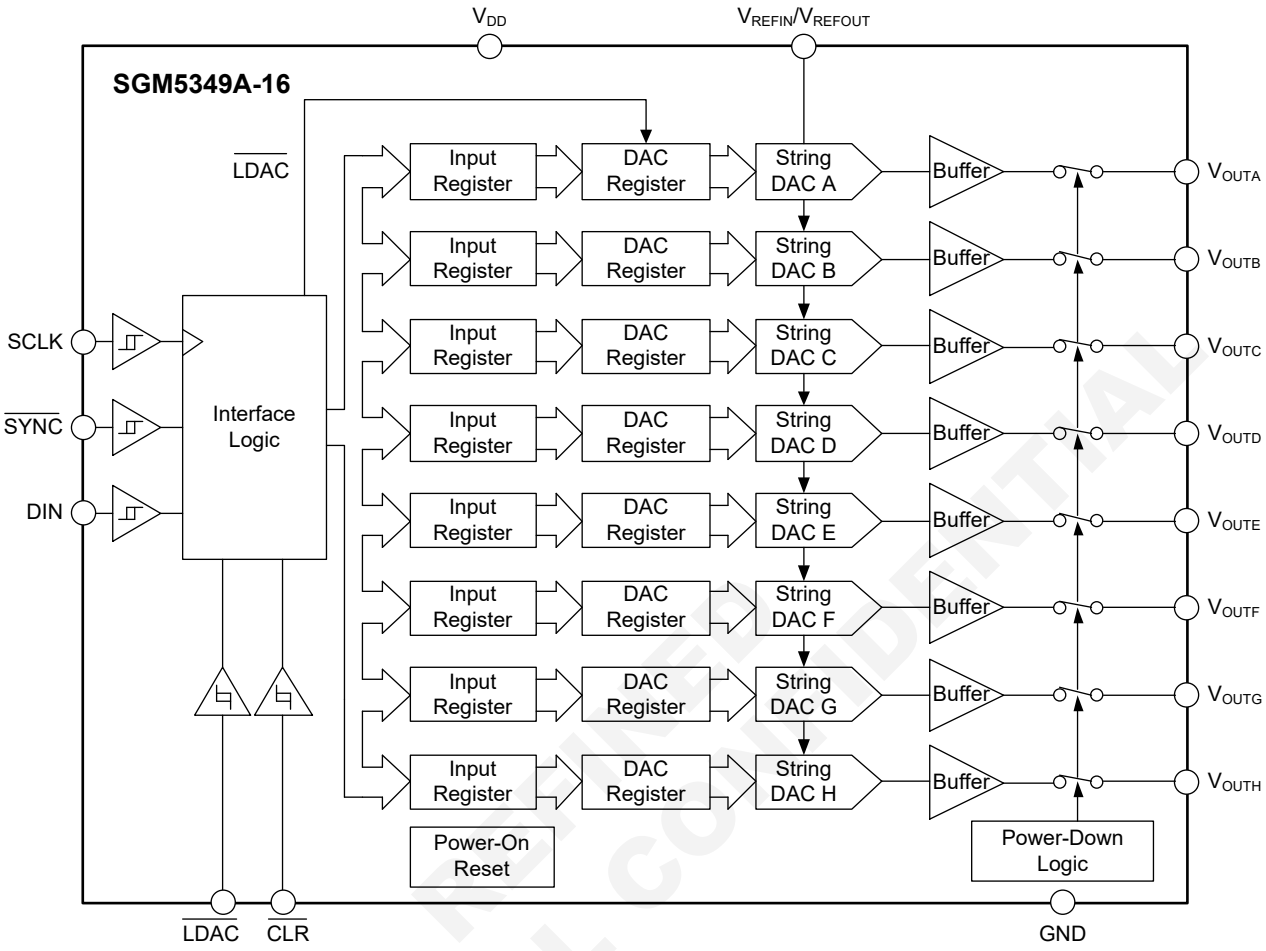

Figure 2. Block Diagram

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THEORY OF OPERATION

D/A Section

The SGM5349A-16 DAC is fabricated on a CMOS process. The architecture consists of a string of DACs followed by an output buffer amplifier. Figure 3 shows a block diagram of the DAC architecture.

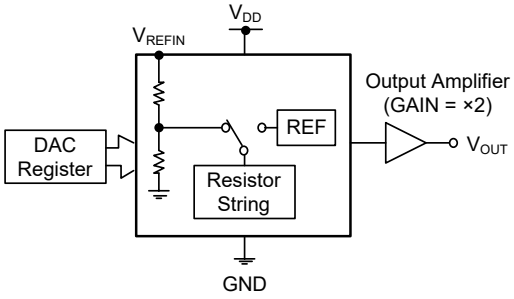

Figure 3. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by:

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

where:

D = Decimal equivalent of the binary code that is loaded to the DAC register. 0 to 65,535 for SGM5349A-16 (16 bits).

N = The DAC resolution.

Resistor String

The resistor string section is shown in Figure 4. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

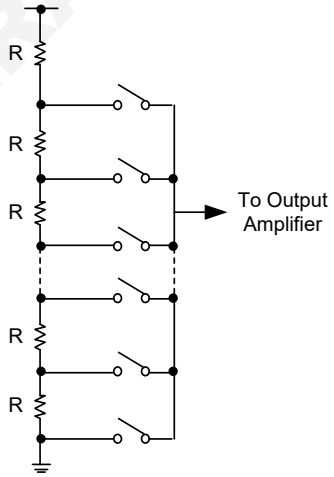

Figure 4. Resistor String

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THEORY OF OPERATION (continued)

Internal Reference

This version of the chip has no reference.

Output Amplifier

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0V to V_{DD}. The amplifier is capable of driving a load of 2kΩ in parallel with 200pF to GND. The slew rate is 1.5V/μs with a ¼ to ¾ scale settling time of 7μs.

Serial Interface

The SGM5349A-16 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 1 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the SGM5349A-16 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{SYNC}$ line keeps in low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned previously, however, $\overline{SYNC}$ must be brought high again just before the next write sequence.

Table 1. Command Definitions

Command				Description
C3	C2	C1	C0	
0	0	0	0	Write to input register n
0	0	0	1	Update DAC register n
0	0	1	0	Write to input register n, update all (software $\overline{LDAC}$)
0	0	1	1	Write to and update DAC channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	1	Reserved
–	–	–	–	Reserved
1	1	1	1	Reserved

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THEORY OF OPERATION (continued)

Table 2. Address Commands

Address (n)				Selected DAC Channel
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

Input Shift Register

The input shift register is 32 bits wide. The first 4 bits are don't cares. The next 4 bits are the command bits, C3 to C0 (see Table 1), followed by the 4-bit DAC address, A3 to A0 (see Table 2) and finally the 16-bit data-word. The data-word comprises the 16-bit input code followed by 4 don't cares bits (see Figure 5). These data bits are transferred to the DAC register on the 32nd falling edge of SCLK.

$\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge and rising edge of $\overline{\text{SYNC}}$. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 6).

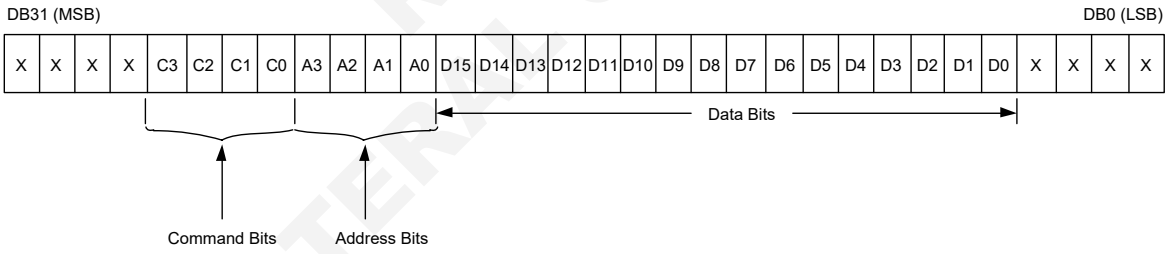

Figure 5. SGM5349A-16 Input Register Contents

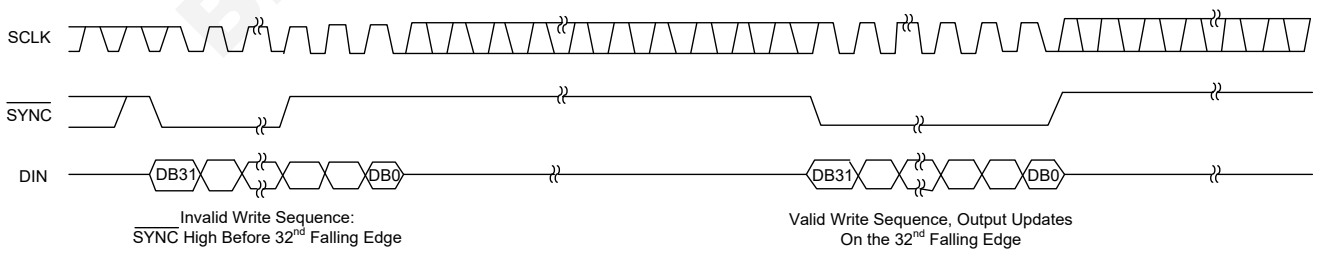

Figure 6. $\overline{\text{SYNC}}$ Interrupt Facility

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THEORY OF OPERATION (continued)

Internal Reference Register

This version of the chip has no reference. The register is reserved, and it must be written to 0.

Power-On Reset

The SGM5349A-16 contains a power-on reset circuit that controls the output voltage during power-up. The SGM5349A-16 DAC output powers up to 0V. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is reserved for this reset function (see Table 1). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

Power-Down Modes

The SGM5349A-16 contains four separate modes of operation. Command 0100 is reserved for the power-down function (see Table 1). These modes are software-programmable by setting two bits, bit DB9 and bit DB8, in the control register.

Table 3 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC H to DAC A) can be powered down to the selected mode by setting the corresponding eight bits (DB7 to DB0) to 1. See Table 6 for the contents of the input shift register during power-down/power-up operation. When using the internal reference, only all channel power-down to the selected modes is supported.

When both bits are set to 0, the part works normally with its normal power consumption of 1.3mA at 5V. However, for the three power-down modes, the supply current falls to 1μA at 5.5V (0.2μA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through either a 1kΩ or a 100kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 7.

The bias generator of the selected DAC(s), output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. The internal reference is powered down only when all channels are powered down. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4μs for V_{DD} = 5V and for V_{DD} = 3V.

Any combination of DACs can be powered up by setting PD1 and PD0 to 0 (normal operation). The output powers up to the value in the input register ($\overline{\text{LDAC}}$ low) or to the value in the DAC register before powering down ($\overline{\text{LDAC}}$ high).

Clear Code Register

The SGM5349A-16 has a hardware $\overline{\text{CLR}}$ pin that is an asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge sensitive. Bringing the $\overline{\text{CLR}}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{\text{CLR}}$ register and sets the analog outputs accordingly. This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting two bits, bit DB1 and bit DB0, in the $\overline{\text{CLR}}$ control register (see Table 5). The default setting clears the outputs to 0V. Command 0101 is reserved for loading the clear code register (see Table 1).

The part exits clear code mode on the 32nd falling edge of the next write to the part. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted.

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THEORY OF OPERATION (continued)

The $\overline{CLR}$ pulse activation time—the falling edge of $\overline{CLR}$ to when the output starts to change—is typically 280ns. However, if outside the DAC linear region, it typically takes 520ns after executing $\overline{CLR}$ for the output to start changing.

See Table 6 for contents of the input shift register during the loading clear code register operation.

Table 3. Power-Down Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1kΩ to GND
1	0	100kΩ to GND
1	1	Three-state

Table 4. 32-Bit Input Shift Register Contents for Power-Down/Power-Up Function

MSB LSB

DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	1	0	0	X	X	X	X	X	PD1	PD0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0) — don't cares				Don't cares	Power-down mode		Power-down/power-up channel selection —set bit to 1 to select							

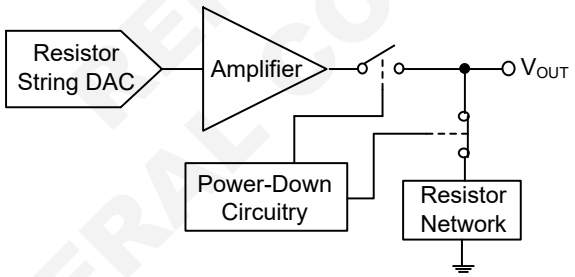

Figure 7. Output Stage during Power-Down

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THEORY OF OPERATION (continued)

Table 5. Clear Code Register

Clear Code Register		Clears to Code
DB1	DB0	
CR1	CR0	
0	0	0x0000
0	1	0x8000
1	0	0xFFFF
1	1	No operation

Table 6. 32-Bit Input Shift Register Contents for Clear Code Function

MSB											LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB2	DB1	DB0
X	0	1	0	1	X	X	X	X	X	CR1	CR0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Clear code register	

$\overline{\text{LDAC}}$ Function

The outputs of all DACs can be updated simultaneously using the hardware $\overline{\text{LDAC}}$ pin.

Synchronous $\overline{\text{LDAC}}$: After new data is read, the DAC registers are updated on the falling edge of the 32nd SCLK pulse. $\overline{\text{LDAC}}$ can be permanently low or pulsed as in Figure 1.

Asynchronous $\overline{\text{LDAC}}$: The outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

Alternatively, the outputs of all DACs can be updated simultaneously using the software $\overline{\text{LDAC}}$ function by writing to input register n and updating all DAC registers. Command 0011 is reserved for this software $\overline{\text{LDAC}}$ function.

An $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin. This register allows the user to select which combination of channels to simultaneously update when the hardware $\overline{\text{LDAC}}$ pin is executed. Setting the $\overline{\text{LDAC}}$ bit register to 0 for a DAC channel means that this channel's update is controlled by the $\overline{\text{LDAC}}$ pin. If this bit is set to 1, this channel updates synchronously; that is, the DAC register is updated after new data is read, regardless of the state of the $\overline{\text{LDAC}}$ pin. It effectively sees the $\overline{\text{LDAC}}$ pin as being tied low. (See Table 7 for the $\overline{\text{LDAC}}$ register mode of operation.) This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using command 0110 loads the 8-bit $\overline{\text{LDAC}}$ register (DB7 to DB0). The default for each channel is 0, that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 means the DAC channel is updated regardless of the state of the $\overline{\text{LDAC}}$ pin. See Table 8 for the contents of the input shift register during the load $\overline{\text{LDAC}}$ register mode of operation.

Table 7. $\overline{\text{LDAC}}$ Register

Load DAC Register		$\overline{\text{LDAC}}$ Operation
$\overline{\text{LDAC}}$ Bits (DB7 to DB0)	$\overline{\text{LDAC}}$ Pin	
0	1/0	Determined by $\overline{\text{LDAC}}$ pin.
1	X—don't cares	DAC channels update, overriding the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 0.

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THEORY OF OPERATION (continued)

Table 8. 32-Bit Input Shift Register Contents for $\overline{\text{LDAC}}$ Register Function

MSB																	LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	1	1	0	X	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0) — don't cares				Don't cares	Setting $\overline{\text{LDAC}}$ bit to 1 overrides $\overline{\text{LDAC}}$ pin							

Power Supply Bypassing and Grounding

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the SGM5349A-16 should have separate analog and digital sections. If the SGM5349A-16 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the SGM5349A-16.

The power supply to the SGM5349A-16 should be decoupled with 10μF and 0.1μF capacitors. The capacitors should physically be placed as close as possible to the device, with the 0.1μF capacitor ideally right up against the device. The 10μF capacitors are the tantalum bead type or ceramic type. It is important that the 0.1μF capacitor has low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic types of capacitors. This 0.1μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other traces in the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

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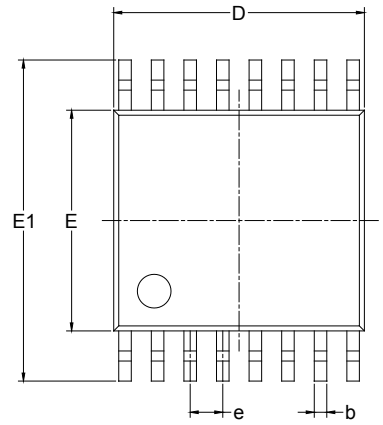
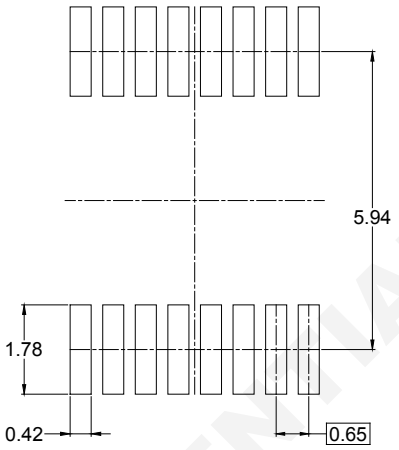
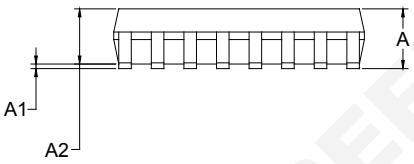
PACKAGE OUTLINE DIMENSIONS

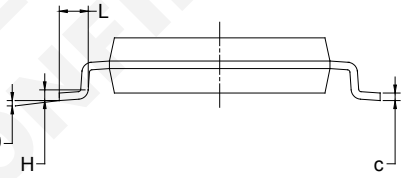
TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

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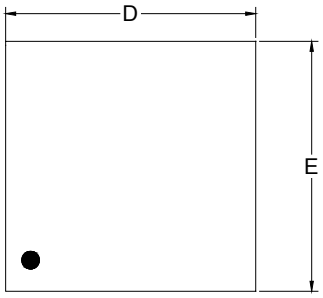
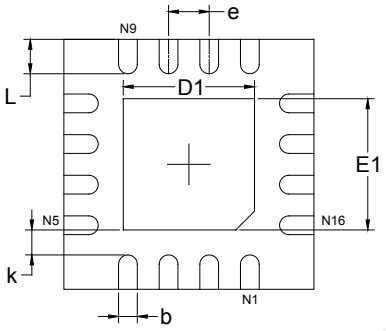
PACKAGE OUTLINE DIMENSIONS

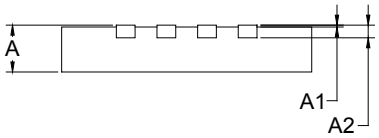
TQFN-4×4-16L



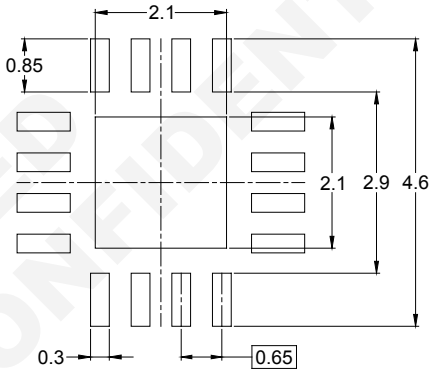
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.000	2.200	0.079	0.087
E	3.900	4.100	0.154	0.161
E1	2.000	2.200	0.079	0.087
k	0.200 MIN		0.008 MIN	
b	0.250	0.350	0.010	0.014
e	0.650 TYP		0.026 TYP	
L	0.450	0.650	0.018	0.026

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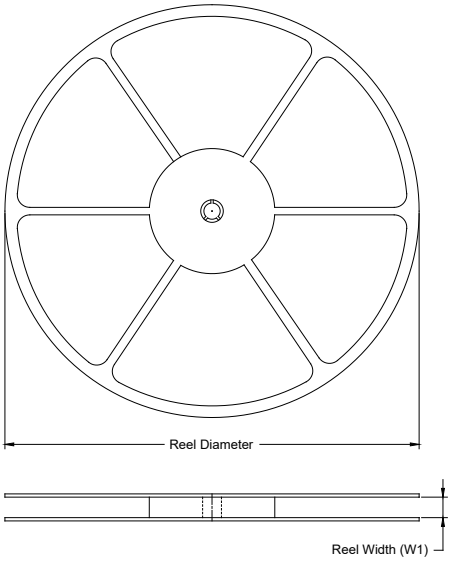
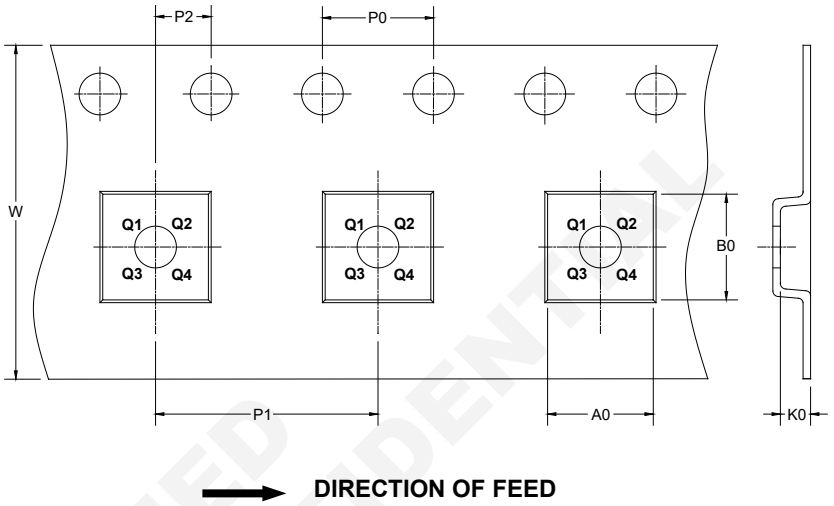
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1
TQFN-4×4-16L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

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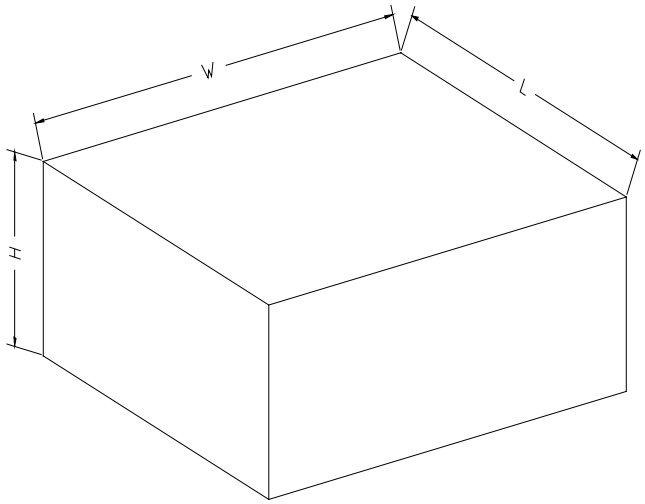
CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002

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