SGM89000
Capless 2Vrms Line Driver with Adjustable Gain

GENERAL DESCRIPTION

The SGM89000 is a 2Vrms pop/click-free stereo line driver designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

The SGM89000 is capable of driving 2Vrms into a 2.5kΩ load with 3.3V supply voltage. The device has differential inputs and uses external gain setting resistors that supports a gain range of ±1V/V to ±10V/V. The use of external gain resistors also allows the implementation of a 2nd-order low pass filter to compliment DAC's and SOC converters. The SGM89000 has build-in shutdown control for pop/click-free on/off control.

Using the SGM89000 in audio products can reduce component count compared to traditional methods of generating a 2Vrms output. The SGM89000 doesn't require a power supply greater than 3.3V to generate a $5.6V_{PP}$ output, nor does the device require a split rail power supply. The SGM89000 integrates a charge pump to generate a negative supply rail that provides a clean, pop/click-free ground-biased 2Vrms output.

The SGM89000 is available in Green TSSOP-14 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Capless Structure**
  - **Eliminates Pop/Clicks**
  - **Eliminates Output DC-Blocking Capacitors**
  - **Provides Flat Frequency Response from DC to 20kHz**
- **Low Noise and THD**
  - **Typical SNR = 107dB**
  - **Typical V_N = 8μVrms**
  - **Typical THD+N = 0.001% (f = 1kHz)**
- **2Vrms Output Voltage into 2.5kΩ Load with 3.3V Supply Voltage**
- **Differential Input**

APPLICATIONS

Set-Top Box
LCD TV
Blue-Ray DVD-Players
Home Theater in a Box

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM89000	TSSOP-14	SGM89000YTS14G/TR	SGM89000 YTS14 XXXXX	Tape and Reel, 3000

NOTE: **XXXXX** = Date Code and Vendor Code.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage.....-0.3V to 4V
Input Voltage.....V_{SS} - 0.3V to V_{DD} + 0.3V
Minimum Load Impedance (R_L) 600Ω
EN to GND.....-0.3V to V_{DD} + 0.3V
Operating Temperature Range.....-40℃ to +85℃
Junction Temperature.....150℃
Storage Temperature..... -65℃ to +150℃
Lead Temperature (Soldering, 10s)
.....260℃
ESD Susceptibility
HBM.....3000V
MM.....250V

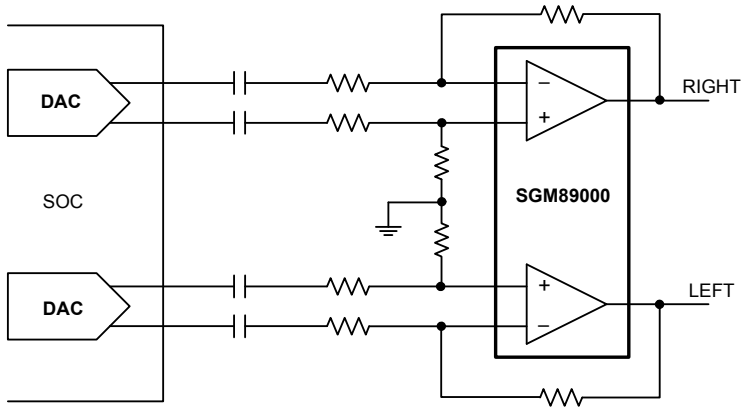
NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

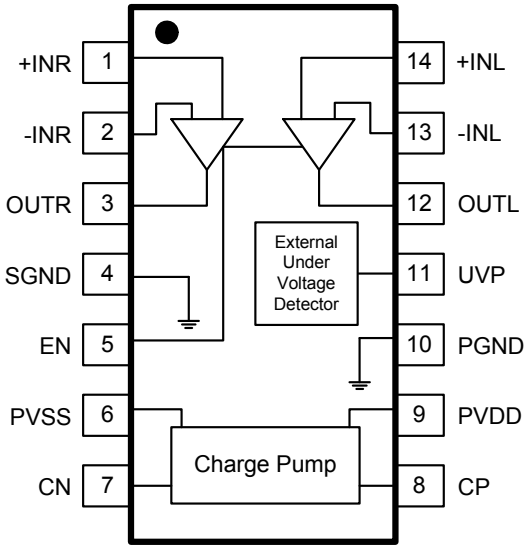
This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

TYPICAL OPERATION CIRCUIT



PIN CONFIGURATION (TOP VIEW)



TSSOP-14

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	+INR	Right Channel OPAMP Positive Input.
2	-INR	Right Channel OPAMP Negative Input.
3	OUTR	Right Channel OPAMP Output.
4	SGND	Signal Ground.
5	EN	Enable Input. Active high.
6	PVSS	Negative Supply Voltage Output.
7	CN	Charge Pump Flying Capacitor Negative Terminal.
8	CP	Charge Pump Flying Capacitor Positive Terminal.
9	PVDD	Positive Supply.
10	PGND	Power Ground.
11	UVP	Undervoltage Protection Input.
12	OUTL	Left Channel OPAMP Output.
13	-INL	Left Channel OPAMP Negative Input.
14	+INL	Left Channel OPAMP Positive Input.

ELECTRICAL CHARACTERISTICS

(T_A = 25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS					
Output Offset Voltage ($\|V_{OS}\|$)	V_{DD} = 3.3V		1.2	5	mV
Power Supply Rejection Ratio (PSRR)	V_{DD} = 3V to 3.6V		97		dB
High-Level Output Voltage (V_{OH})	V_{DD} = 3.3V, R_L = 2.5kΩ	3.18			V
Low-Level Output Voltage (V_{OL})	V_{DD} = 3.3V, R_L = 2.5kΩ			-3.1	V
High-Level Input Current (EN) ($\|I_{IH}\|$)	V_{DD} = 3.3V, V_I = V_{DD}			1	μA
Low-Level Input Current (EN) ($\|I_{IL}\|$)	V_{DD} = 3.3V, V_I = 0V			1	μA
Supply Current (I_{DD})	V_{DD} = 3.3V, No load, EN = V_{DD}	8.1	11.5		mA
	Shutdown mode, V_{DD} = 3V to 3.6V		0.1	0.2	
OPERATING CHARACTERISTICS (V_{DD} = 3.3V, R_L = 2.5kΩ, C_{PUMP} = 0.33μF, C_{PVSS} = 0.33μF, C_{IN} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ.) (1)					
Output Voltage (Outputs in Phase) (V_O)	THD = 1%, V_{DD} = 3.3V, f = 1kHz	2.05			Vrms
Total Harmonic Distortion Plus Noise (THD+N)	V_O = 2Vrms, f = 1kHz		0.001		%
	V_O = 2Vrms, f = 6.8kHz		0.004		
Crosstalk	V_O = 2Vrms, f = 1kHz		115		dB
Output Current Limit (I_O)	V_{DD} = 3.3V		20		mA
Input Resistor Range (R_{IN})		1	10	47	kΩ
Feedback Resistor Range (R_{FB})		4.7	20	100	kΩ
Slew Rate			8		V/μs
Maximum Capacitive Load			220		pF
Noise Output Voltage (V_N)	A-weighted, BW = 20kHz		8		μVrms
Signal to Noise Ratio (SNR)	V_O = 2Vrms, THD+N = 0.1%, BW = 20kHz, A-weighted		107		dB
Unity Gain Bandwidth (G_{BW})			5.3		MHz
Open-Loop Voltage Gain (A_{VO})			120		dB
Charge Pump Frequency (F_{CP})		300	410	550	kHz
External Undervoltage Detection (V_{UVP})		1.05	1.13	1.25	V
External Undervoltage Detection Hysteresis Current (I_{Hys})			4.6		μA
SHUTDOWN PIN					
Input High Voltage (V_{INH})		1.2			V
Input Low Voltage (V_{INL})				0.6	V
RECOMMENDED OPERATING CONDITIONS					
DC Supply Voltage (V_{DD})		3		3.6	V

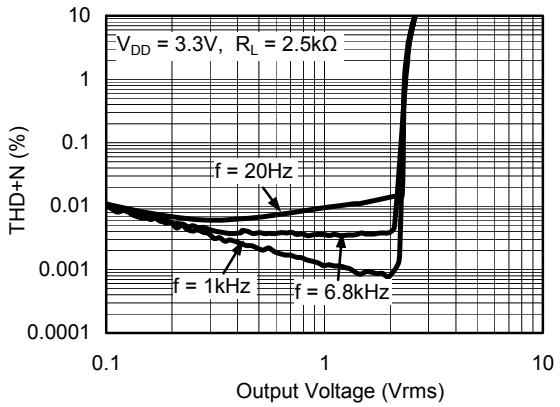
NOTE:

1. For C_{PUMP}, C_{PVSS}, C_{IN}, R_{IN} and etc, please refer to the APPLICATION CIRCUIT on page 7.

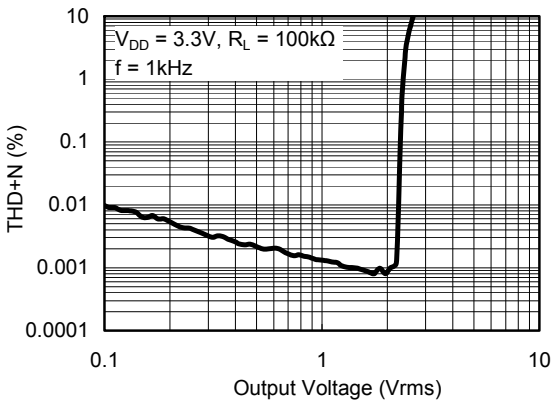
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, T_A = 25℃, R_L = 2.5kΩ, C_{PUMP} = 0.33μF, C_{PVSS} = 0.33μF, C_{IN} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ, unless otherwise noted.

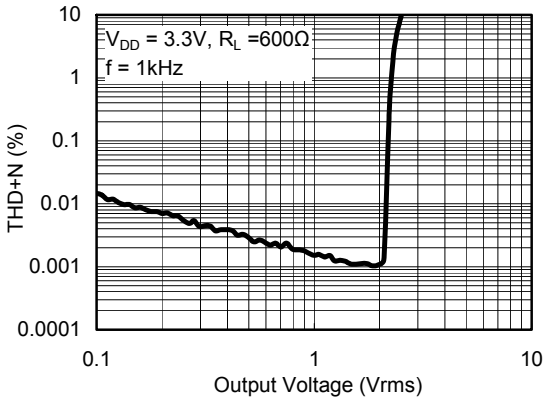
THD+N vs. Output Voltage



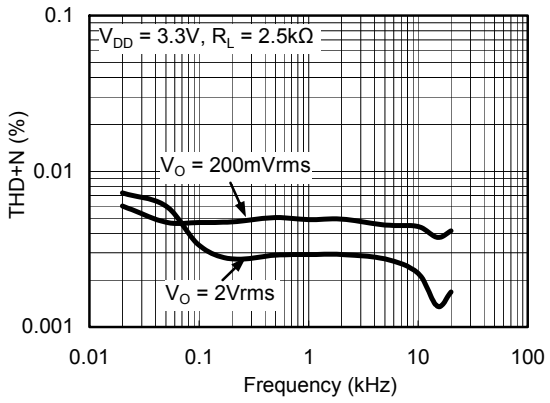
THD+N vs. Output Voltage



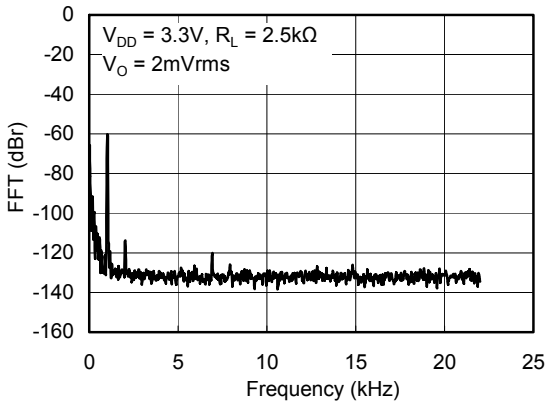
THD+N vs. Output Voltage



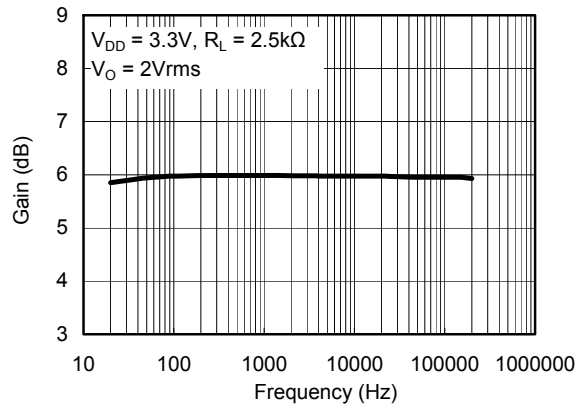
THD+N vs. Frequency



FFT vs. Frequency



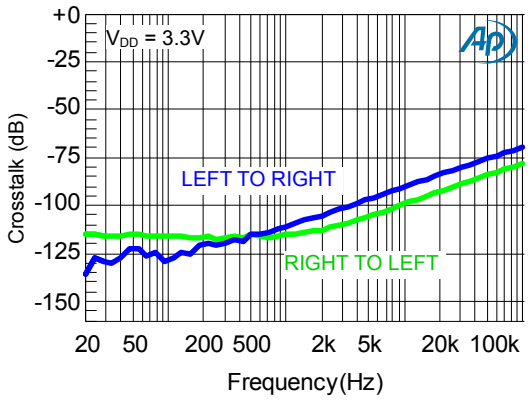
Gain vs. Frequency



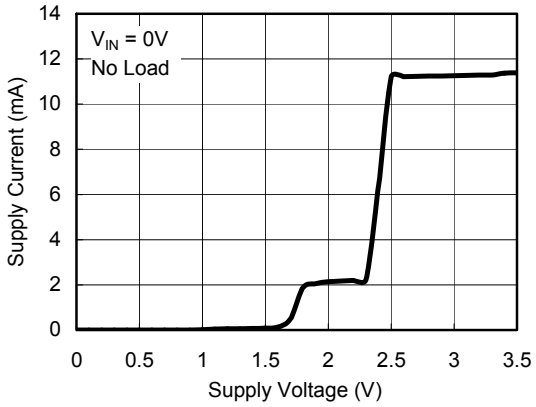
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, T_A = 25℃, R_L = 2.5kΩ, C_{PUMP} = 0.33μF, C_{PVSS} = 0.33μF, C_{IN} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ, unless otherwise noted.

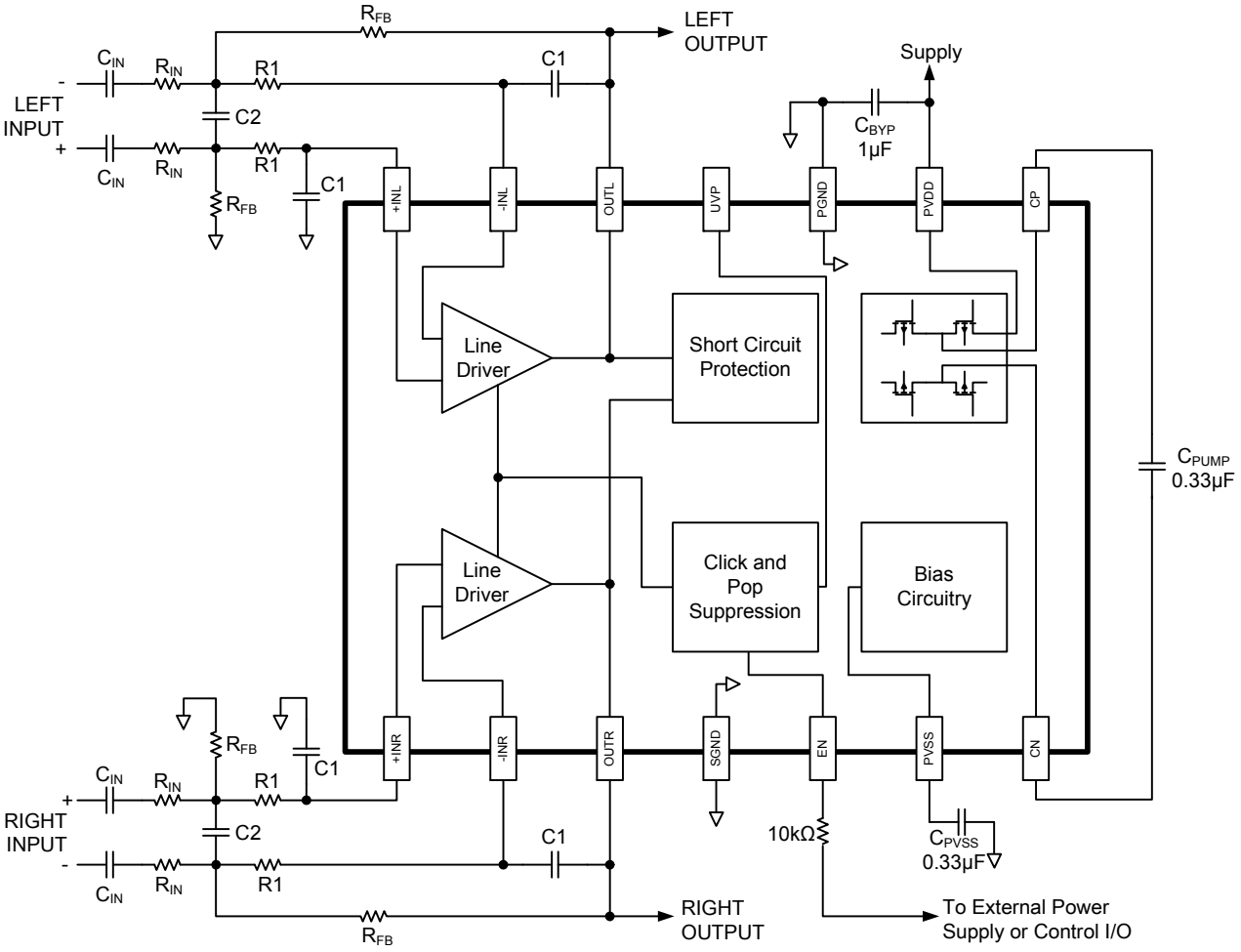
Crosstalk vs. Frequency



Supply Current vs. Supply Voltage



APPLICATION CIRCUIT



NOTES:

1. In order to get good performance, it's important to select the right C_{PUMP}, C_{PVSS} and C_{BYP} in application. All tests are performed with circuit set up with X5R and X7R capacitors. Capacitors having high dissipative loss, such as Y5V capacitor, may cause performance degradation and unexpected system behavior.

2. A 10kΩ resistor must be serially connected to EN pin.

APPLICATION INFORMATION

Decoupling Capacitors

The SGM89000 is a capless line driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead, works best. Placing this decoupling capacitor close to the SGM89000 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10μF or larger capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Gain Setting Resistors Ranges

The gain setting resistors, R_{IN} and R_{FB}, must be chosen so that noise, stability and input capacitor size of the SGM89000 are kept within acceptable limits. Voltage gain is defined as R_{FB} divided by R_{IN}.

Selecting values that are too low demands a large input AC coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different gain settings.

Table 1. Recommended Resistor Values

INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{FB}	DIFFERENTIAL INPUT GAIN	INVERTING INPUT GAIN	NON INVERTING INPUT GAIN
22kΩ	22kΩ	1.0V/V	-1.0V/V	2.0V/V
20kΩ	30kΩ	1.5V/V	-1.5V/V	2.5V/V
33kΩ	68kΩ	2.1V/V	-2.1V/V	3.1V/V
10kΩ	100kΩ	10.0V/V	-10.0V/V	11.0V/V

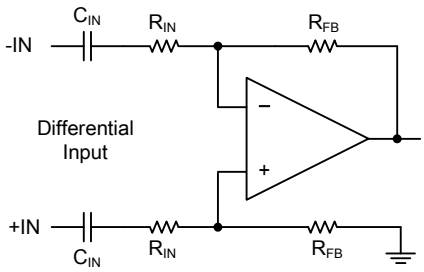


Figure 1. Differential Input

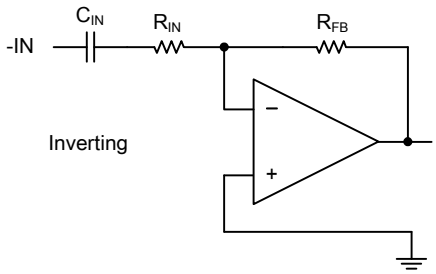


Figure 2. Inverting

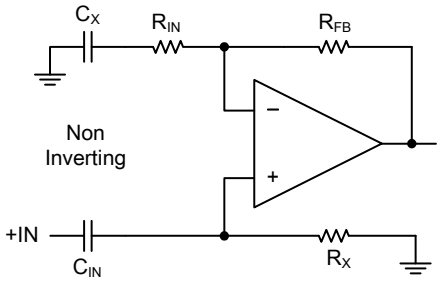


Figure 3. Non-Inverting

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the SGM89000. These capacitors block the DC portion of the audio source and allow the SGM89000 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC-gain to one, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1, then the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad or \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \qquad (1)$$

Using the SGM89000 as 2nd-Order Filter

Several audio DACs used today require an external low-pass filter to remove out of band noise. This is possible with the SGM89000 as it can be used like a standard OPAMP.

Several filter topologies can be implemented both single-endedly and differentially. In Figure 4, a Multi Feedback (MFB), with differential input and single-ended input is shown.

An AC coupling capacitor to remove DC-content from the source is shown. It serves to block any DC-content from the source and lowers the DC-gain to one, helping reducing the output DC-offset to minimum.

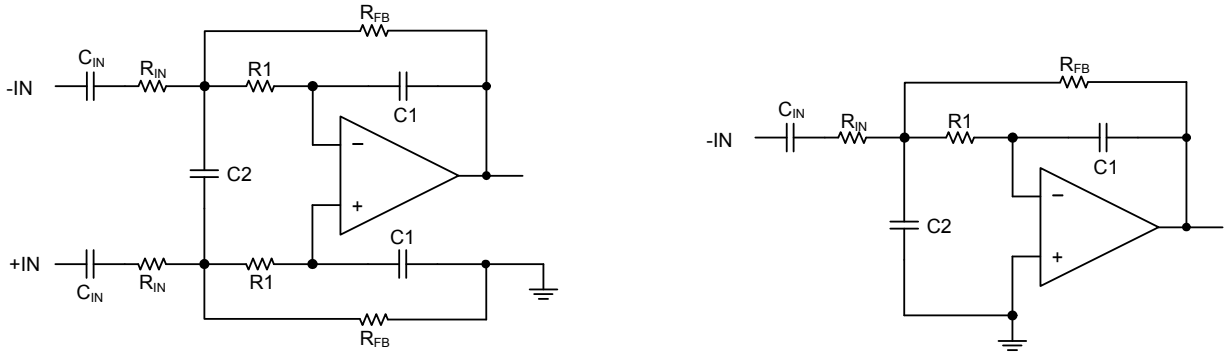


Figure 4. 2nd-Order Active Low Pass Filter

The resistor values should be kept low to obtain low noise, but should also be high enough to get a small size AC coupling cap. Using 5.6kΩ for the resistors, C1 = 220pF, and C2 = 470pF, an SNR of 107dB can be achieved with a 10μF input AC coupling capacitor.

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{SD}$ (EN) (shutdown pin) low during power supply ramp up and down. The EN pin should be kept low until the input AC coupling capacitors are fully charged before asserting the EN pin high. This way proper precharge of the AC coupling is performed, and pop-free power-up is achieved. Figure 5 illustrates the preferred sequence.

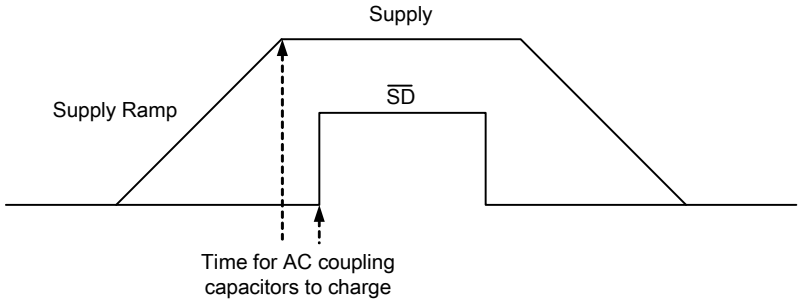


Figure 5. Power-Up Sequence

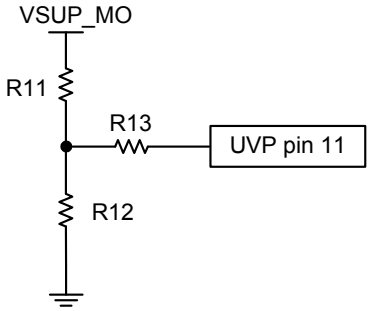
External Undervoltage Detection

External undervoltage detection can be used to mute/shut down the SGM89000 before an input device can generate a pop.

The threshold seen at the UVP pin is 1.13V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:

Startup Threshold: V_{UDPR} = 1.13V × (R11 + R12) / R12
Shutdown Threshold: V_{UDPF} = 1.13V × (R11+R12) / R12 - 4.6μA × (R13 + R11 || R12) × (R11 + R12) / R12
Hysteresis: 4.6μA × (R13 + R11 || R12) × (R11 + R12) / R12

The R13 is optional. If the R13 is not used, the UVP pin connects to the divider center tap directly.



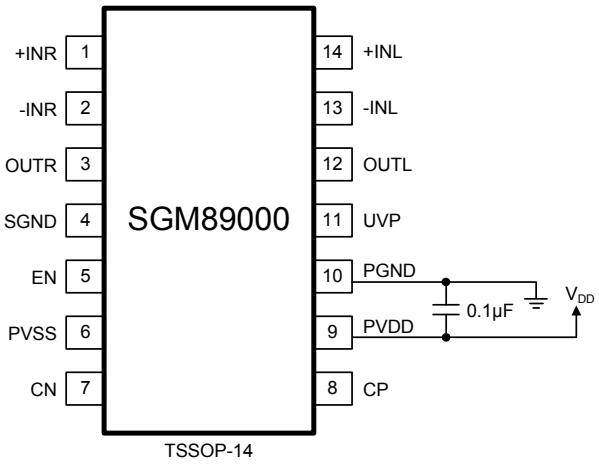
Capacitive Load

The SGM89000 has the ability to drive large capacitive load up to 220pF directly, and larger capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

Gain-Setting Resistors

The gain setting resistors, R_{IN} and R_{FB}, must be placed close to the input pins to minimize the capacitive loading on these pins and to ensure maximum stability of the SGM89000.

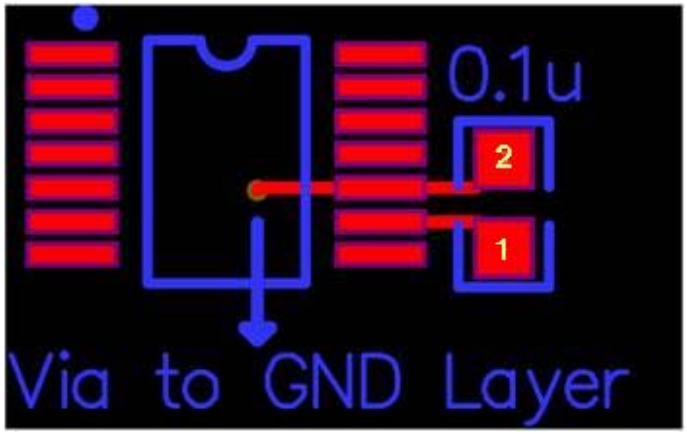
PCB Layout Guide



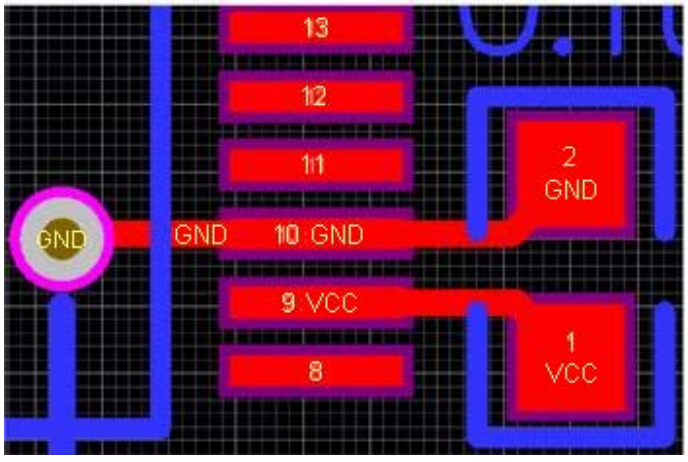
TSSOP-14

NOTE: 0.1μF decoupling capacitor must be close to PGND and PVDD pins; capacitor can be connected between PVDD and PGND pins directly and then connect PGND pin to GND layer.

The reference PCB layout is shown in below:

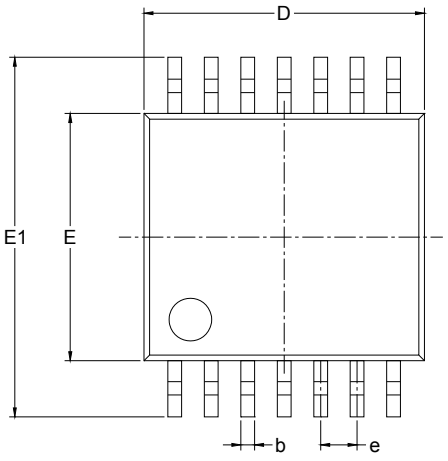


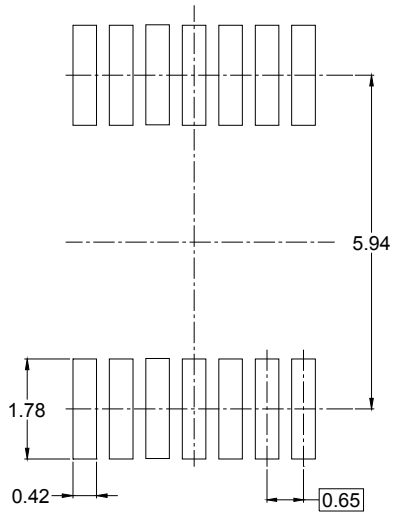
Zoomed in:



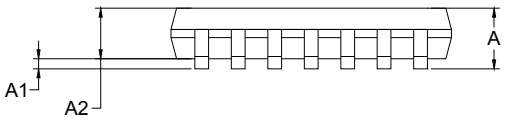
PACKAGE OUTLINE DIMENSIONS

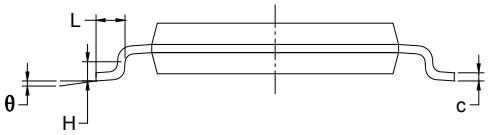
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

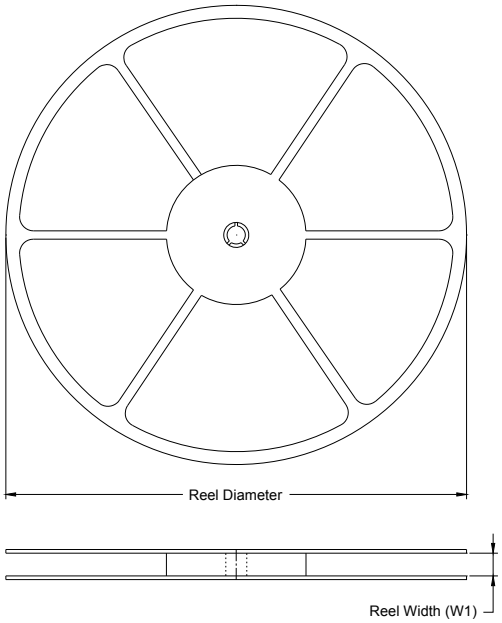




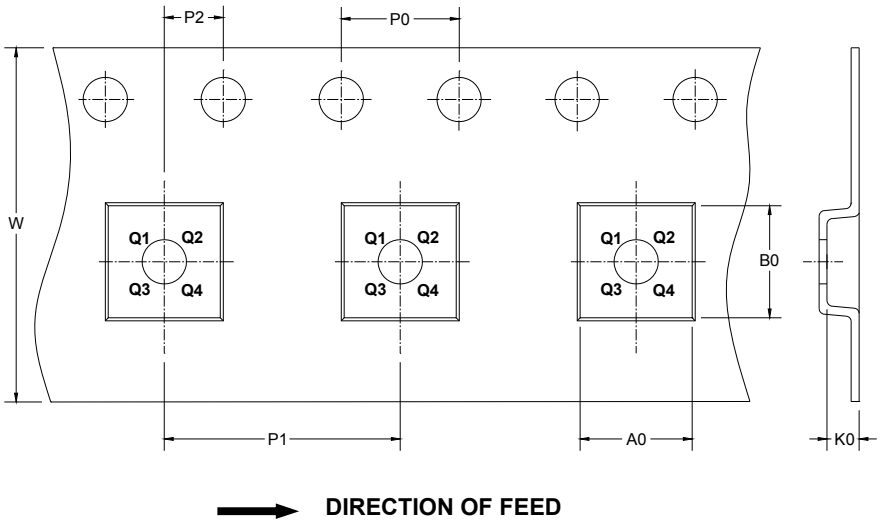
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

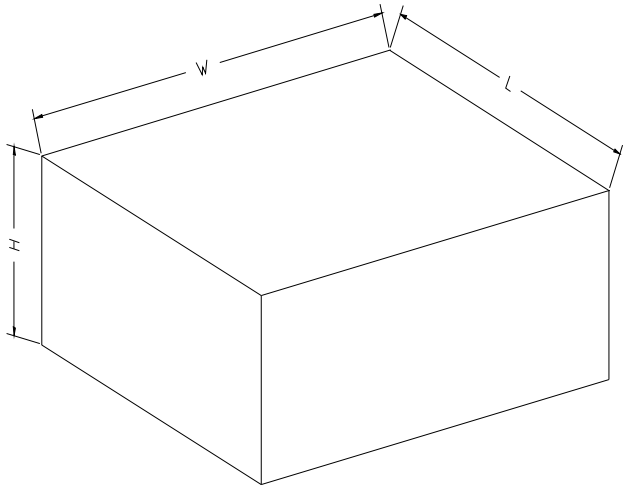


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.6	1.2	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5