SGM9150
4-Channel, Video Filter Driver for SD/HD (1080p)

PRODUCT DESCRIPTION

The SGM9150 video filter is intended to replace passive LC filters and drivers with an integrated device. One 6th-order channel offers Standard Definition (SD) filter while the other three channels are High Definition (HDp) filters. The SGM9150 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal clamp and bias circuitry may be used if AC-coupled inputs are required.

The outputs can be AC- or DC-coupled. DC coupling the outputs removes the need for large output coupling capacitors.

The SGM9150 is available in Green TSSOP-14 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Three Fixed 6th-Order Filters for 1080p High Definition Mode**
- **One 6th-Order Standard Definition Filter**
- **Independent Shutdown Control to Save Power**
- **Clamp Mode on SD Channel Input**
- **Bias Mode on HD Channel Input**
- **Bias Mode Active with AC-Coupled Inputs for HD Video**
- **Bias Mode Inactive with DC-Coupled Inputs for HD Video**
- **AC- or DC-Coupled Outputs**
- **DC-Coupled Output Eliminates AC Coupling Capacitor**
- **Available in Green TSSOP-14 Package**
- **-40℃ to +85℃ Operating Temperature Range**

APPLICATIONS

Set-Top Boxes
Communication Devices
Portable and Handheld Products
Personal Video Recorders
Video on Demand
DVD Players
HDTVs

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM9150	TSSOP-14	40℃ to +85℃	SGM9150YTS14G/TR	SGM9150 YTS14 XXXXX	Tape and Reel, 3000

NOTE: **XXXXX** = Date Code and Vendor Code.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, GND to V_{CC} 6V
Input Voltage Range ..... GND - 0.3V to V_{CC} + 0.3V
Storage Temperature Range ..... -65℃ to +150℃
Junction Temperature ..... 150℃
Operating Temperature Range ..... -40℃ to +85℃
Lead Temperature (Soldering, 10s) ..... 260℃
ESD Susceptibility
HBM 8000V
MM 400V

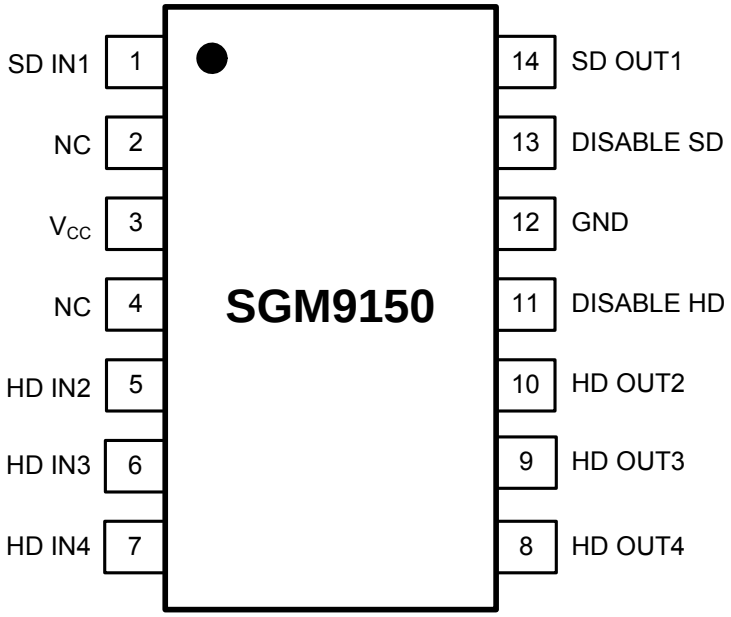
NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATION (TOP VIEW)

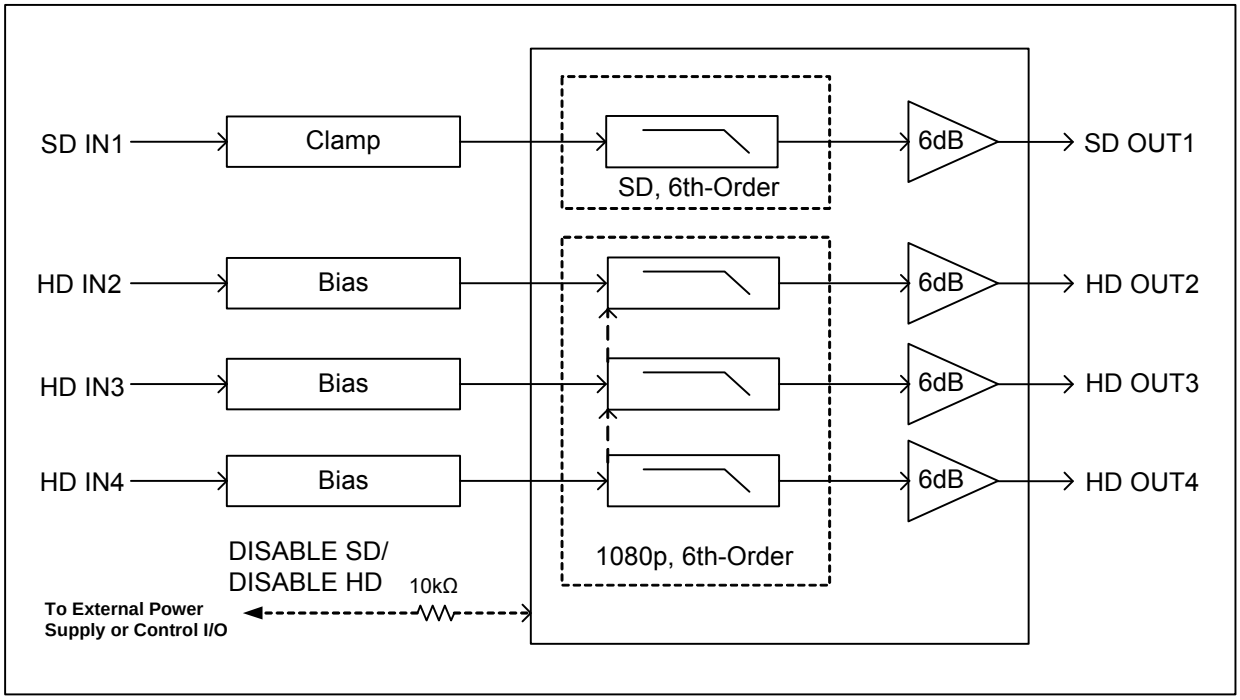


TSSOP-14

PIN DESCRIPTION

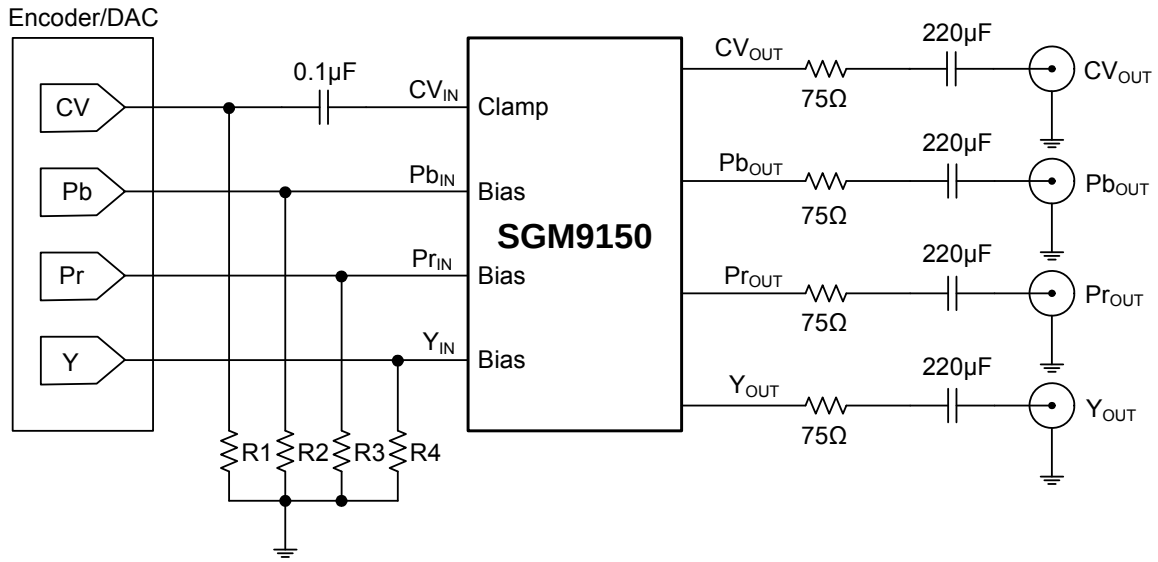
PIN	NAME	FUNCTION
1	SD IN1	SD Video Input.
2, 4	NC	No Connect.
3	V_{CC}	Power Supply.
5	HD IN2	HD Video Input.
6	HD IN3	HD Video Input.
7	HD IN4	HD Video Input.
8	HD OUT4	Filtered HD Video Output.
9	HD OUT3	Filtered HD Video Output.
10	HD OUT2	Filtered HD Video Output.
11	DISABLE HD	Disable Standard Full High-Definition Channel. Logic “high” disables the HD channel and logic “low” enables the HD channel. This pin defaults to logic low if left open.
12	GND	Ground.
13	DISABLE SD	Disable Standard Definition Channel. Logic “high” disables the SD channel and logic “low” enables the SD channel. This pin defaults to logic low if left open.
14	SD OUT1	Filtered SD Video Output.

BLOCK DIAGRAM



NOTES:
1. A 10kΩ resistor must be serially connected to DISABLE SD or DISABLE HD pin.
2. Power supply V_{CC} must be sequenced on first before input video signals.

TYPICAL APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS

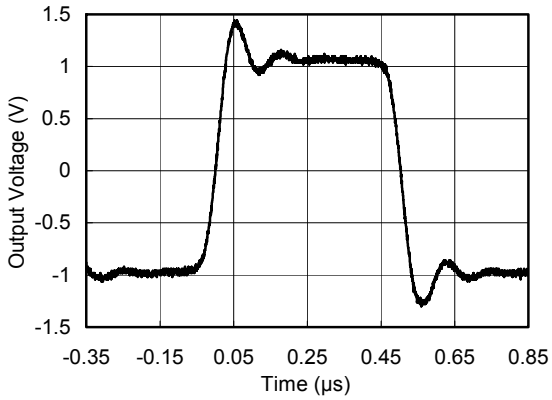
(T_A = +25℃, V_{IN} = 1V_{PP}, V_{CC} = 5.0V, R_{SOURCE} = 37.5Ω; all inputs are AC-coupled with 0.1μF; all outputs are AC-coupled with 220μF into 150Ω, referenced to 400kHz, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Operating Voltage Range (V_{CC})			3.1	5	5.5	V
Quiescent Current (I_Q)	V_{CC} = 5.0V, no load	SD channel		9.5	12.8	mA
		All		77	98	
Output Level Shift Voltage (V_{OLS})	V_{IN} = 0V, no load	SD channel		410	600	mV
		HD channels		550	700	
Voltage Gain (A_V)	R_L = 150Ω		5.8	6.1	6.35	dB
Output Voltage High Swing	V_{IN} = 3V, R_L = 150Ω to GND			4.8		V
Shutdown Current				2	15	μA
Video Input Voltage Range	Referenced to GND if DC-coupled			1.4		V_{PP}
Power Supply Rejection Ratio (PSRR)	DC (All channels)			50		dB
V_{IH}	Disable		2.4			V
V_{IL}	Enable				0.8	V
STANDARD DEFINITION MODE ELECTRICAL CHARACTERISTICS						
-0.1dB Bandwidth	SD channel			6.4		MHz
-1dB Bandwidth	SD channel			7.6		MHz
-3dB Bandwidth	SD channel			8.5		MHz
Filter Response (Normalized Gain)	SD channel, f_{IN} = 400kHz to 27MHz			50		dB
Slew Rate	2V output step, 80% to 20%			34		V/μs
Differential Gain (DG)	AC-AC coupled, PAL			0.5		%
	AC-DC coupled, PAL			0.4		
Differential Phase (DP)	AC-AC coupled, PAL			1.0		deg
	AC-DC coupled, PAL			1.0		
Group Delay Variation (D/DT)	Difference between 400kHz and 6.5MHz			35		ns
Crosstalk (channel-to-channel)	V_{OUT} = 1.4V_{PP}, f = 1MHz			-63		dB
Signal-to-Noise Ratio (SNR)	100kHz to 5MHz			-66		dB
Fall Time	2V output step, 80% to 20%			34		ns
Rise Time	2V output step, 80% to 20%			34		ns
Chroma Luma Gain (CLG_{SD})	f = 3.58MHz (Referenced to SD_{IN} at 400kHz)			102		%
Chroma Luma Delay (CLD_{SD})	f = 3.58MHz (Referenced to SD_{IN} at 400kHz)			9		ns
Enable Time (t_{ON})				1.4		μs
Disable Time (t_{OFF})				28		ns
1080p HIGH DEFINITION MODE ELECTRICAL CHARACTERISTICS						
-0.1dB Bandwidth	R_L = 150Ω			78		MHz
-1dB Bandwidth	R_L = 150Ω			86		MHz
-3dB Bandwidth	R_L = 150Ω			98		MHz
Filter Response (Normalized Gain)	f_{IN} = 400kHz to 148MHz			21		dB
Slew Rate	2V output step, 80% to 20%			340		V/μs
Group Delay Variation (D/DT)	Difference between 400kHz and 70MHz			5.3		ns
Crosstalk (channel-to-channel)	V_{OUT} = 1.4V_{PP}, f = 1MHz			-64		dB
Fall Time	2V output step, 80% to 20%			3.3		ns
Rise Time	2V output step, 80% to 20%			3.6		ns
Enable Time (t_{ON})				1.7		μs
Disable Time (t_{OFF})				29		ns

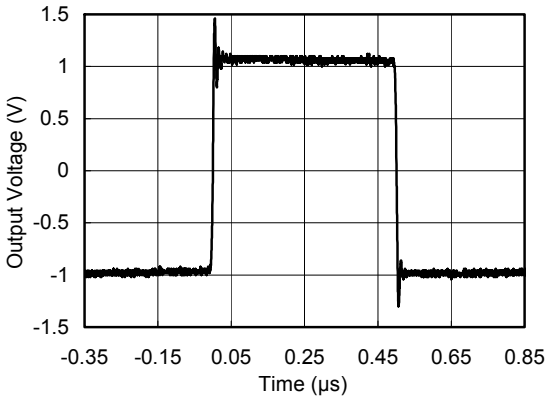
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 1V_{PP}, V_{CC} = 5.0V, R_{SOURCE} = 37.5Ω; all inputs are AC-coupled with 0.1μF; all outputs are AC-coupled with 220μF into 150Ω, referenced to 400kHz, unless otherwise noted.

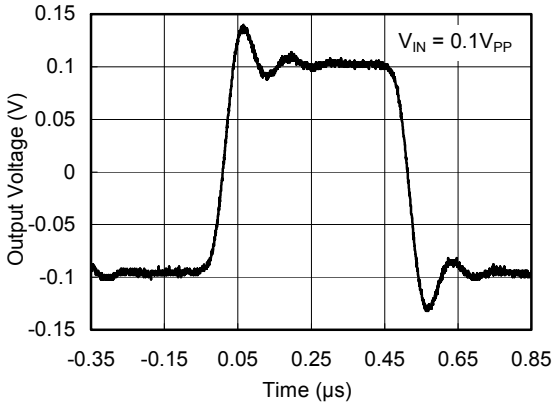
SD Large Signal Step Response



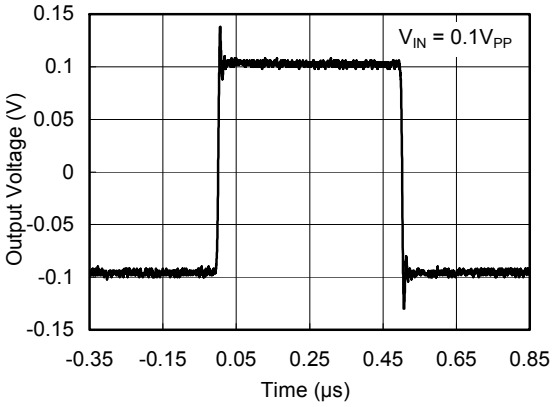
1080p Large Signal Step Response



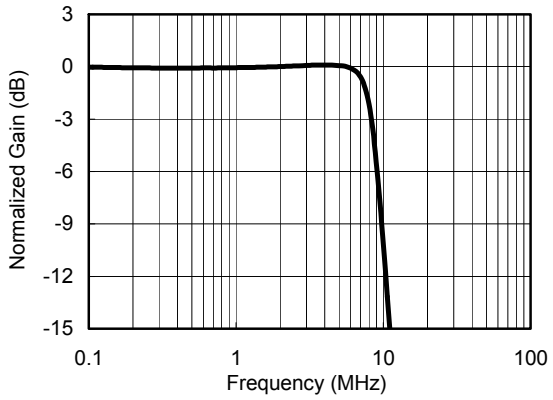
SD Small Signal Step Response



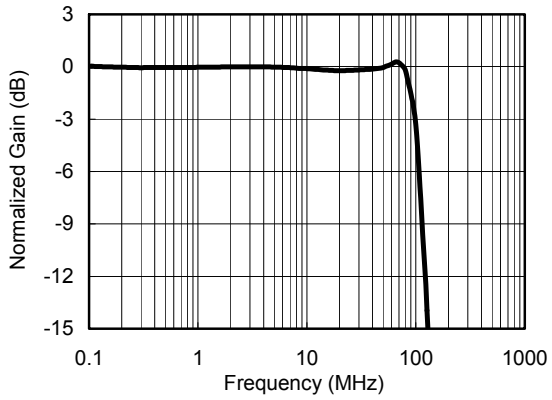
1080p Small Signal Step Response



SD Gain vs. Frequency



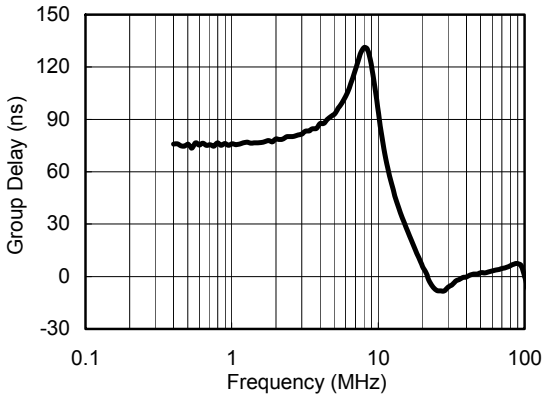
1080p Gain vs. Frequency



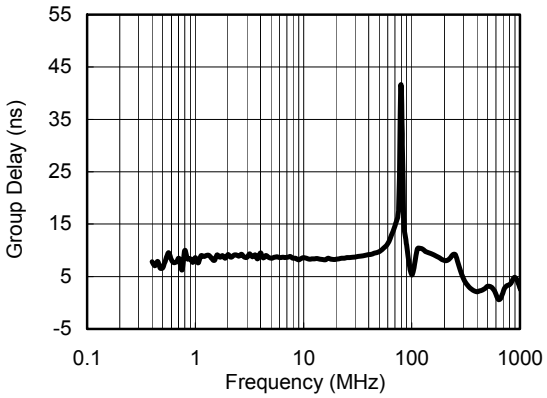
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 1V_{PP}, V_{CC} = 5.0V, R_{SOURCE} = 37.5Ω; all inputs are AC-coupled with 0.1μF; all outputs are AC-coupled with 220μF into 150Ω, referenced to 400kHz, unless otherwise noted.

SD Group Delay vs. Frequency



1080p Group Delay vs. Frequency



APPLICATION INFORMATION

Application Circuits

The SGM9150 video filter provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load.

The SGM9150 provides an internal clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the SGM9150 without an AC coupling capacitor. When the input is AC-coupled, the clamp sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp cannot exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb and Pr, the average DC bias is fairly constant and the inputs can be AC-coupled. DAC outputs can also drive these same signals without the AC coupling capacitor.

I/O Configurations

For a DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 1.

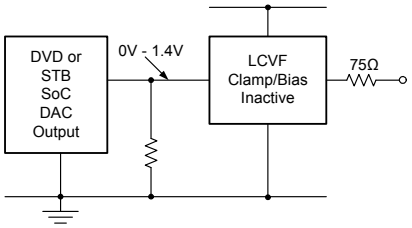


Figure 1. DC-Coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range from 0V to 1.4V, it can be AC-coupled as shown in Figure 2.

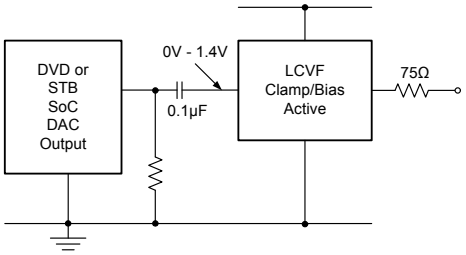


Figure 2. AC-Coupled Inputs, DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

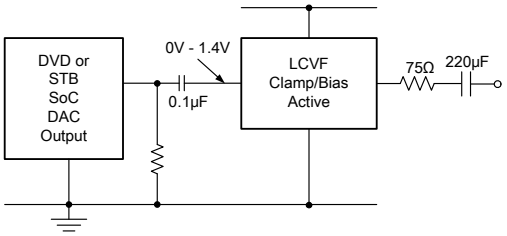


Figure 3. AC-Coupled Inputs and Outputs

NOTE: The video tilt or line time distortion is dominated by the AC coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The SGM9150 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following equations can be used to calculate the power dissipation and internal temperature rise.

$T_J = T_A + P_D \bullet \theta_{JA}$ (1)

where:

$P_D = P_{CH1} + P_{CH2} + P_{CH3}$ (2)

$P_{CHX} = V_{CC} \bullet I_{CH} - (V_O^2/R_L)$ (3)

where:

$V_O = 2V_{IN} + 0.55V$ (4)

$I_{CH} = (I_{CC}/3) + (V_O/R_L)$ (5)

V_{IN} = RMS value of input signal

I_{CC} = 77mA (all channels on)

V_{CC} = 5.0V

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the Layout Considerations section for details.

The SGM9150 is specified to operate with output currents typically less than 50mA. Internal amplifiers are current limited to a maximum of 80mA and should withstand brief duration of short-circuit conditions. This capability is not guaranteed.

APPLICATION INFORMATION

Output Considerations

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. In order to obtain the highest quality output video signal the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the SGM9150 output driver. Recommended distance from device pin to series termination resistor should be no greater than 0.1 inches.

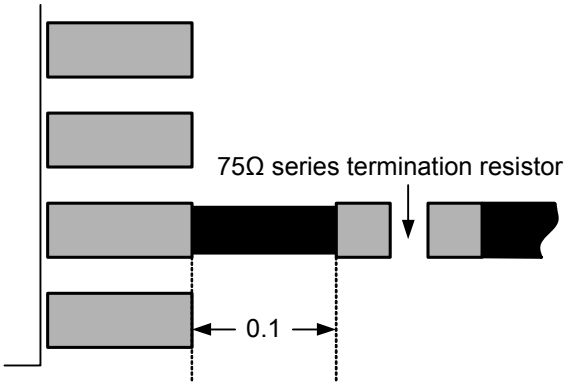


Figure 4. Distance from Device Pin to Series Termination Resistor

Thermal Considerations

Since the interior of systems such as set-top boxes, TVs and DVD players are at +70℃, consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane) each other on the PCB.

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. We offer a demonstration board to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

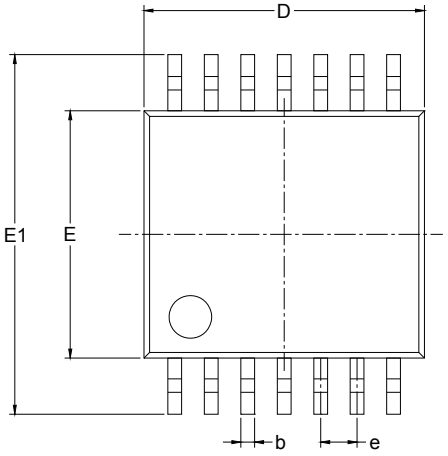
- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Do not run traces on top of the ground plane.
- Run no traces over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 0.01μF and 0.1μF ceramic power supply bypass capacitors.
- Place the 0.1μF capacitor within 0.1 inches of the device power pin.
- Place the 0.01μF capacitor within 0.75 inches of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 0.5 inches on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.
- Place a 75Ω series resistor within 0.5 inches of the output pin to isolate the output driver from board parasitics.

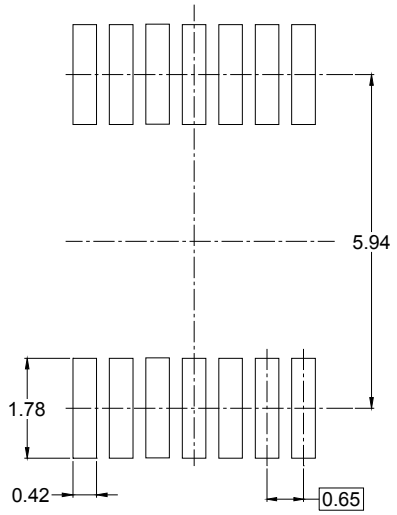
PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70μm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in the power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Consider modeling techniques a first-order approximation.

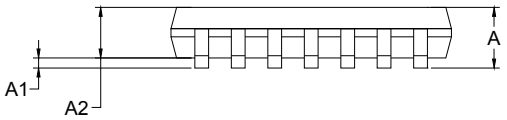
PACKAGE OUTLINE DIMENSIONS

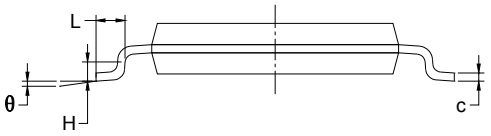
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

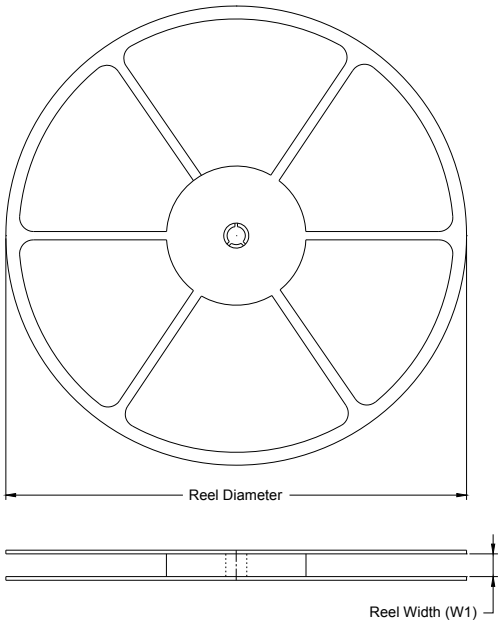




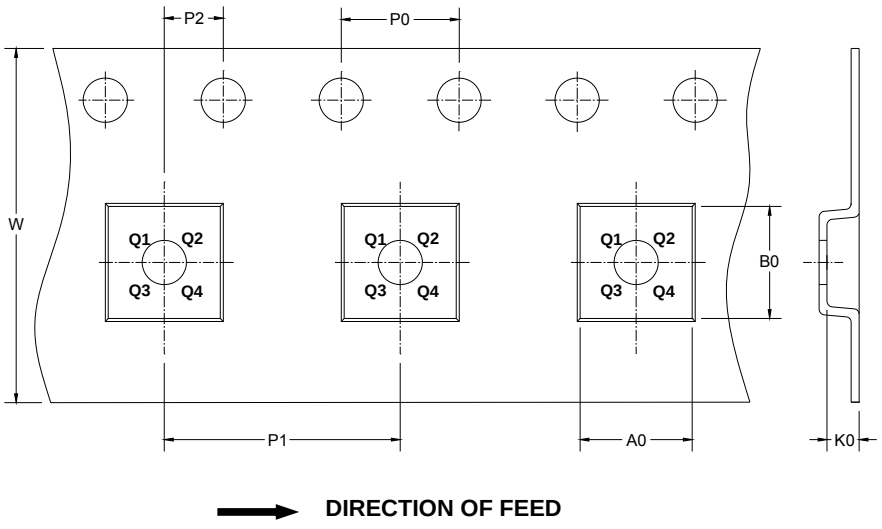
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

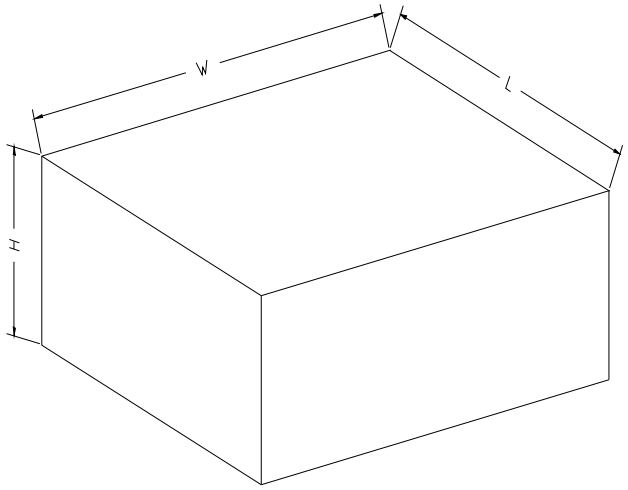


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.6	1.2	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5