SGM48753
CMOS Analog Switch

GENERAL DESCRIPTION

The SGM48753 is a CMOS analog IC configured as three single-pole/double-throw (SPDT) switches. This CMOS device can operate from 2.5V to 5.5V single supplies. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA (TYP) at +25℃.

All digital inputs can support 1.8V logic control I/O.

The SGM48753 is available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3×3-16L packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Guaranteed On-Resistance 48Ω (TYP) with +5V Supply**
- **Guaranteed On-Resistance Match Between Channels**
- **Low Off-Leakage Current 1nA (TYP) at +25℃**
- **Low On-Leakage Current 1nA (TYP) at +25℃**
- **Optimized Rise Time and Fall Time of A, B, C Control Pins to Reduce Clock Feedthrough Effect**
- **2.5V to 5.5V Single-Supply Operation**
- **1.8V Logic Compatible**
- **Low Distortion: 0.7% (R_L = 600Ω, f = 20Hz to 20kHz)**
- **High Off-Isolation: -83dB (R_L = 50Ω, f = 1MHz)**
- **Low Crosstalk: -110dB (R_L = 50Ω, f = 1MHz)**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3×3-16L Packages**

APPLICATIONS

Battery-Operated Equipment
Audio and Video Signal Routing
Low-Voltage Data-Acquisition Systems
Communications Circuits
Automotive

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48753	SOIC-16	-40℃ to +85℃	SGM48753YS16G/TR	SGM48753YS16 XXXXX	Tape and Reel, 2500
	SSOP-16	-40℃ to +85℃	SGM48753YQS16G/TR	SGM48753 YQS16 XXXXX	Tape and Reel, 3000
	TSSOP-16	-40℃ to +85℃	SGM48753YTS16G/TR	SGM48753 YTS16 XXXXX	Tape and Reel, 4000
	TQFN-3×3-16L	-40℃ to +85℃	SGM48753YTQ16G/TR	48753TQ XXXXX	Tape and Reel, 4000

NOTE: **XXXXX** = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... -0.3V to 6V
Voltage into Any Terminal (1) ..... -0.3V to (V_{CC} + 0.3V)
Continuous Current into Any Terminal ..... ±20mA
Peak Current, X_, Y_, Z_
(Pulsed at 1ms, 10% duty cycle) ..... ±40mA
Junction Temperature ..... 150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... 260℃
ESD Susceptibility
HBM 3000V
MM 200V

NOTE:
1. Voltages exceeding V_{CC} or V_{EE} on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.5V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

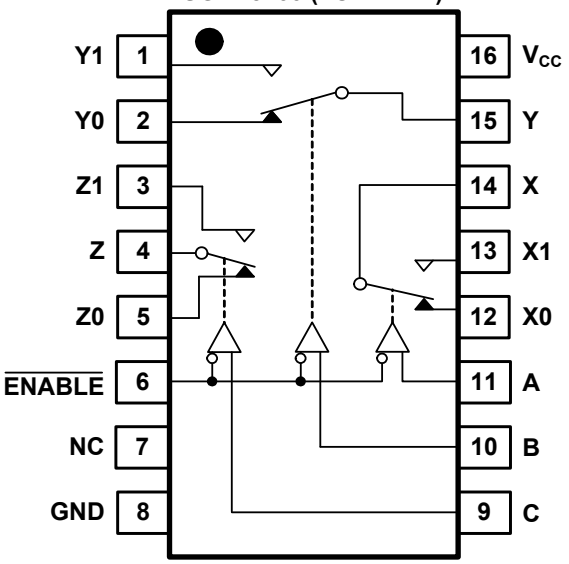
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

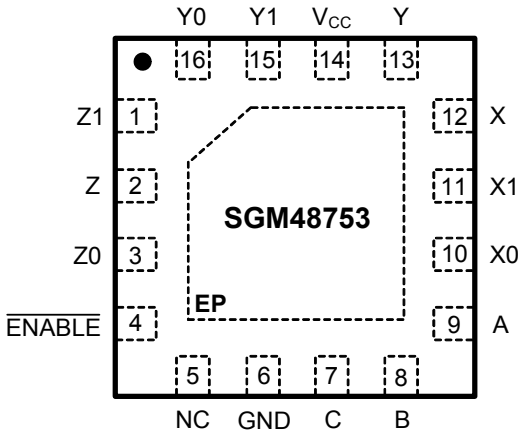
PIN CONFIGURATIONS

SGM48753 (TOP VIEW)



SOIC-16/SSOP-16/TSSOP-16

SGM48753 (TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN		NAME	FUNCTION
SOIC-16/SSOP-16/ TSSOP-16	TQFN-3×3-16L		
1	15	Y1	Analog Switch “Y” Normally Open Input.
2	16	Y0	Analog Switch “Y” Normally Closed Input.
3	1	Z1	Analog Switch “Z” Normally Open Input.
4	2	Z	Analog Switch “Z” Output.
5	3	Z0	Analog Switch “Z” Normally Closed Input.
6	4	$\overline{\text{ENABLE}}$	Digital Enable Input. Normally connected to GND.
7	5	NC	No Connect.
8	6	GND	Ground. Connect to digital ground.
9	7	C	Digital Address “C” Input.
10	8	B	Digital Address “B” Input.
11	9	A	Digital Address “A” Input.
12	10	X0	Analog Switch “X” Normally Closed Input.
13	11	X1	Analog Switch “X” Normally Open Input.
14	12	X	Analog Switch “X” Output.
15	13	Y	Analog Switch “Y” Output.
16	14	V_{CC}	Positive Analog and Digital Supply Voltage Input.
—	Exposed Pad	EP	Exposed Pad. Connect EP to GND.

FUNCTION TABLE

$\overline{\text{ENABLE}}$ INPUT	SELECT INPUTS			ON SWITCHES
	C	B	A	
H	*X*	*X*	*X*	All Switches Open
L	L	L	L	X-X0, Y-Y0, Z-Z0
L	L	L	H	X-X1, Y-Y0, Z-Z0
L	L	H	L	X-X0, Y-Y1, Z-Z0
L	L	H	H	X-X1, Y-Y1, Z-Z0
L	H	L	L	X-X0, Y-Y0, Z-Z1
L	H	L	H	X-X1, Y-Y0, Z-Z1
L	H	H	L	X-X0, Y-Y1, Z-Z1
L	H	H	H	X-X1, Y-Y1, Z-Z1

X = Don’t care

NOTE: Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$, V_X, V_Y, V_Z		Full	GND		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 5.0V, I_X, I_Y, I_Z = 1mA	+25℃		48	58	Ω
			Full			67	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 5.0V, I_X, I_Y, I_Z = 1mA	+25℃		1.5	5	Ω
			Full			5.3	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 5.0V, I_X, I_Y, I_Z = 1mA	+25℃		17	25	Ω
			Full			28	
X_, Y_, Z_ Off Leakage Current	$I_{X\_(OFF)}$, $I_{Y\_(OFF)}$, $I_{Z\_(OFF)}$	V_{CC} = 5.0V, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 4.5V, V_X, V_Y, V_Z = 4.5V, 1V	+25℃		1	1000	nA
X, Y, Z Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V_{CC} = 5.0V, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 4.5V, V_X, V_Y, V_Z = 4.5V, 1V	+25℃		1	1000	nA
X, Y, Z On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_{CC} = 5.0V, V_X, V_Y, V_Z = 4.5V, 1V	+25℃		1	1000	nA
DIGITAL I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, $V_{\overline{ENABLE}}$		+25℃	1.7			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, $V_{\overline{ENABLE}}$		+25℃			0.5	V
Input-Current High	I_{AH}, I_{BH}, I_{CH}, $I_{\overline{ENABLE}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC}	+25℃		1	1000	nA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}, $I_{\overline{ENABLE}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = 0V	+25℃		1	1000	nA
DYNAMIC CHARACTERISTICS							
Address Transition Time	t_{TRANS}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		85		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		60		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		70		ns
Internal A, B, C Rise Time	t_R		+25℃		45		ns
Internal A, B, C Fall Time	t_F		+25℃		50		ns
Break-Before-Make Time	t_D	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		50		ns
Charge Injection	Q	R_S = 0Ω, C = 1nF, V_S = 0V, Test Circuit 4	+25℃		3		pC
Off Isolation	O_{ISO}	R_L = 50Ω, f = 1MHz, Test Circuit 5	+25℃		-83		dB
Channel-to-Channel Crosstalk	X_{TALK}	R_L = 50Ω, f = 1MHz, Test Circuit 5	+25℃		-110		dB
Input Off-Capacitance	$C_{X\_(OFF)}$, $C_{Y\_(OFF)}$, $C_{Z\_(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Test Circuit 6	+25℃		8		pF
Output Off-Capacitance	$C_{X(OFF)}$, $C_{Y(OFF)}$, $C_{Z(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Test Circuit 6	+25℃		9		pF
Output On-Capacitance	$C_{X(ON)}$, $C_{Y(ON)}$, $C_{Z(ON)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0V, f = 1MHz, Test Circuit 6	+25℃		16		pF
-3dB Bandwidth	BW	R_L = 50Ω	+25℃		180		MHz
Total Harmonic Distortion	THD	R_L = 600Ω, $5V_{P-P}$, f = 20Hz to 20kHz	+25℃		0.7		%
POWER SUPPLY							
Power Supply Range	V_{CC}		Full	2.5		5.5	V
Power Supply Current	I_{CC}	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC} or 0	+25℃		0.001	6	μA

ELECTRICAL CHARACTERISTICS

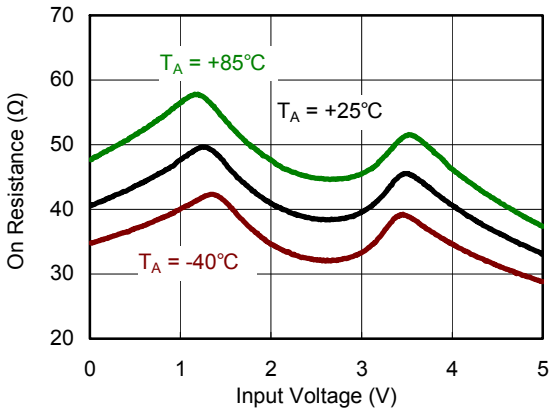
(V_{CC} = 3.3V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$, V_X, V_Y, V_Z		Full	GND		V_{CC}	V
On-Resistance	R_{ON}	I_X, I_Y, I_Z = 1mA	+25℃		80	110	Ω
			Full			116	
X_, Y_, Z_ Off Leakage Current	$I_{X\_(OFF)}$, $I_{Y\_(OFF)}$, $I_{Z\_(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 3V, V_X, V_Y, V_Z = 3V, 1V	+25℃		1	1000	nA
X, Y, Z Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 3V, V_X, V_Y, V_Z = 3V, 1V	+25℃		1	1000	nA
X, Y, Z On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V_X, V_Y, V_Z = 3V, 1V	+25℃		1	1000	nA
DIGITAL I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, $V_{\overline{ENABLE}}$		+25℃	1.7			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, $V_{\overline{ENABLE}}$		+25℃			0.5	V
Input-Current High	I_{AH}, I_{BH}, I_{CH}, $I_{\overline{ENABLE}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC}	+25℃		1	1000	nA
Input-Current Low	I_{AL}, I_{BL}, I_{CL}, $I_{\overline{ENABLE}}$	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = 0V	+25℃		1	1000	nA
DYNAMIC CHARACTERISTICS							
Address Transition Time	t_{TRANS}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		150		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		110		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		110		ns
Internal A, B, C Rise Time	t_R		+25℃		80		ns
Internal A, B, C Fall Time	t_F		+25℃		85		ns
Break-Before-Make Time	t_D	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		80		ns
Charge Injection	Q	R_S = 0Ω, C = 1nF, V_S = 0V, Test Circuit 4	+25℃		3		pC
-3dB Bandwidth	BW	R_L = 50Ω	+25℃		180		MHz
POWER SUPPLY							
Power Supply Current	I_{CC}	V_A, V_B, V_C, $V_{\overline{ENABLE}}$ = V_{CC} or 0	+25℃		0.001	3	μA

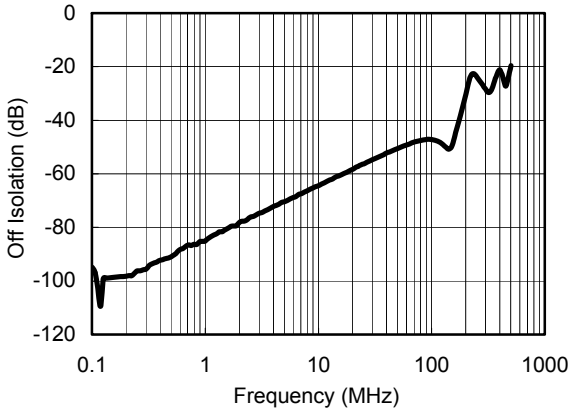
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5.0V, unless otherwise noted.

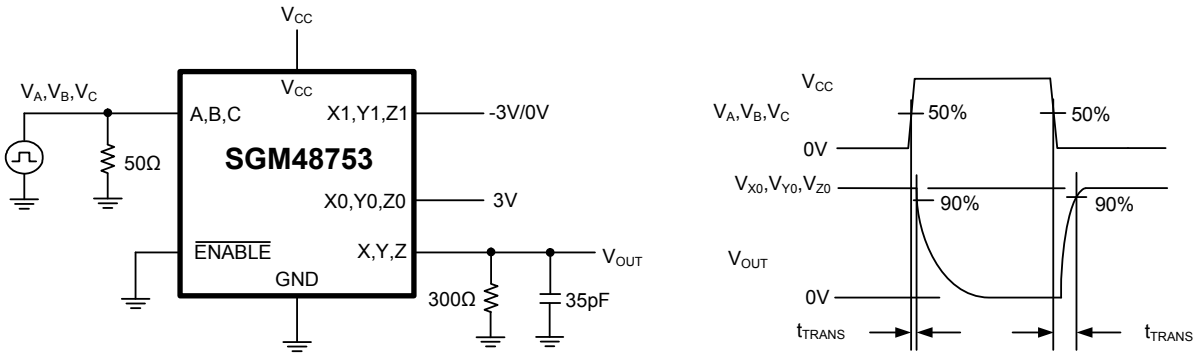
On Resistance vs. Input Voltage



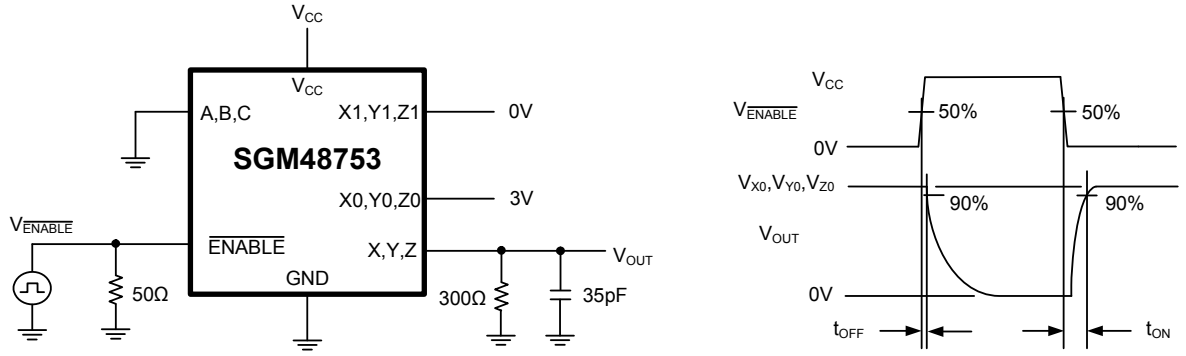
Off Isolation vs. Frequency



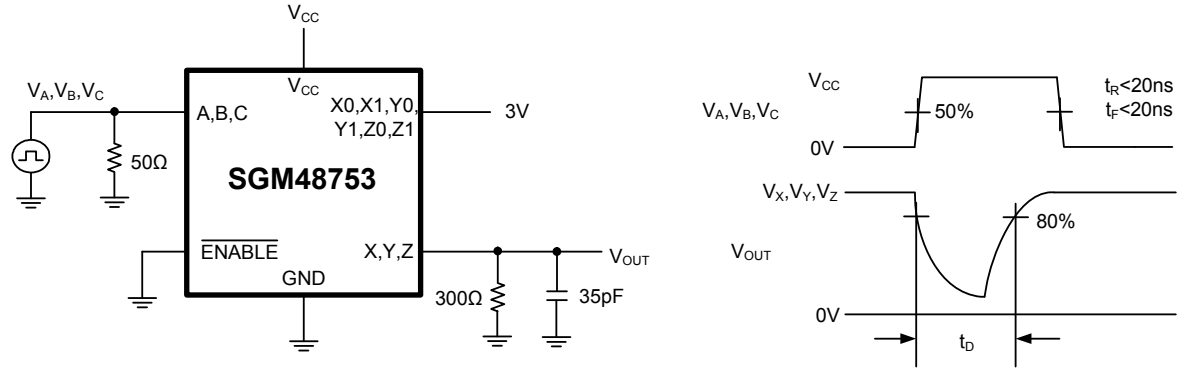
TEST CIRCUITS



Test Circuit 1. Address Transition Times (t_{TRANS})

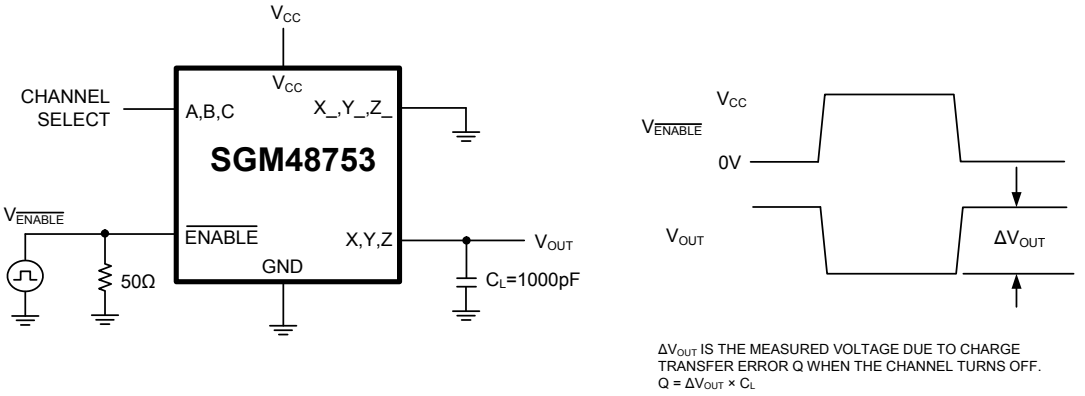


Test Circuit 2. Switching Times (t_{ON}, t_{OFF})



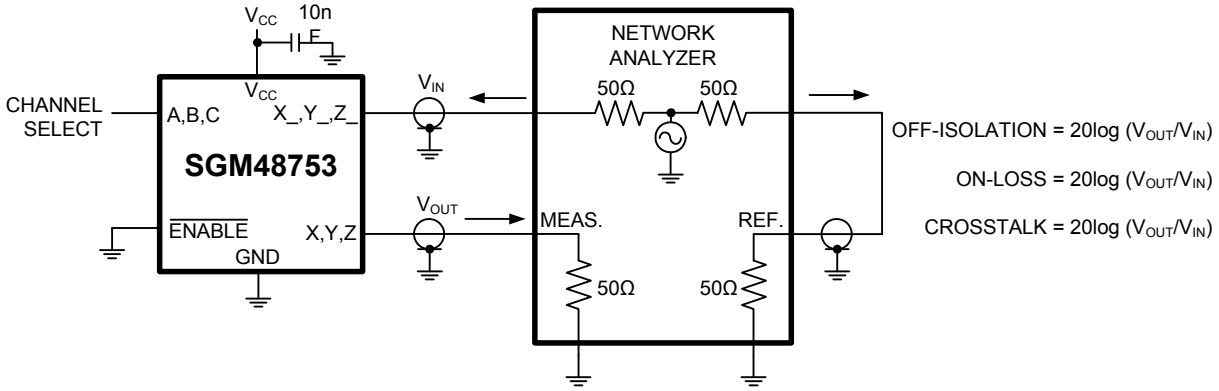
Test Circuit 3. Break-Before-Make Time (t_D)

TEST CIRCUITS



ΔV_{OUT} IS THE MEASURED VOLTAGE DUE TO CHARGE TRANSFER ERROR Q WHEN THE CHANNEL TURNS OFF.
$Q = \Delta V_{OUT} \times C_L$

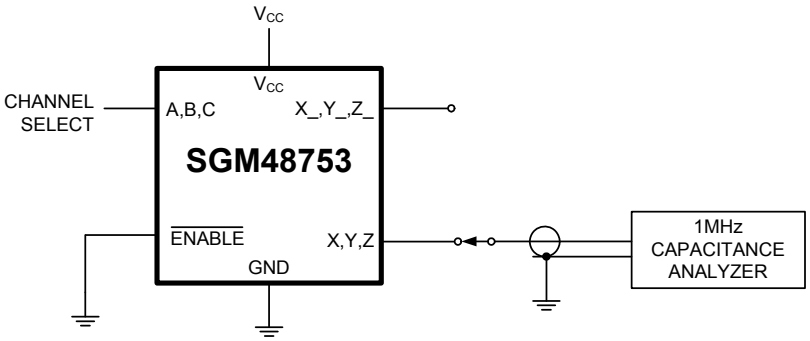
Test Circuit 4. Charge Injection (Q)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK IS MEASURED FROM ONE CHANNEL (A, B, C) TO ALL OTHER CHANNELS.

SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

Test Circuit 5. Off Isolation, On Loss and Crosstalk



Test Circuit 6. Capacitance

APPLICATION INFORMATION

Power-Supply Considerations

Overview

The SGM48753 construction is typical of most CMOS analog switch. It supports single power supply. V_{CC} and GND are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog-signal pin and both V_{CC} and GND. If any analog signal exceeds V_{CC} or GND, one of these diodes will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V_{CC} or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V_{CC} or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_{CC} and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

Over-Voltage Protection

Proper power-supply sequencing is recommended for the CMOS device. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add one 100Ω resistor in series with the supply V_{CC} pin for over-voltage protection (Figure 1).

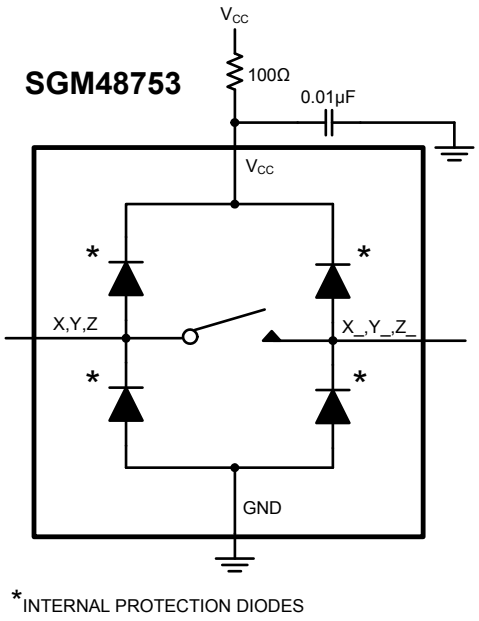
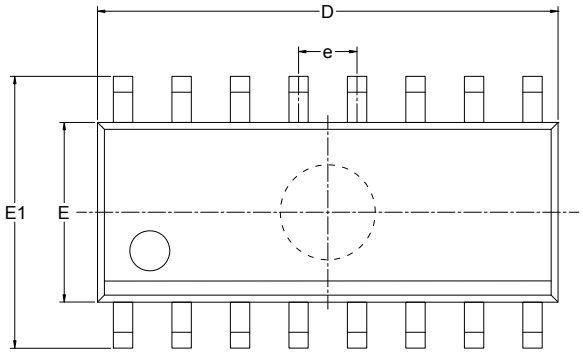
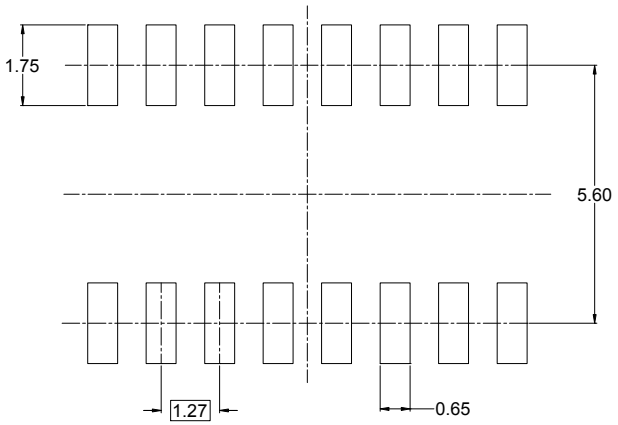


Figure 1. Over-Voltage Protection Using External Resistor

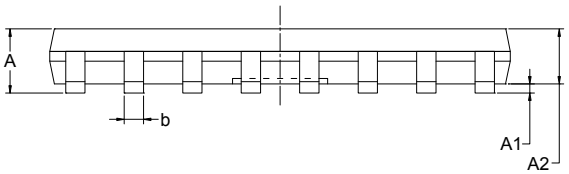
PACKAGE OUTLINE DIMENSIONS

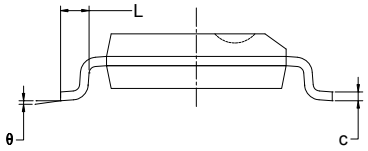
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)

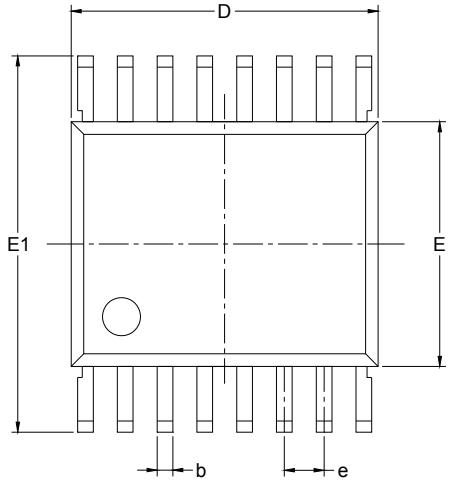


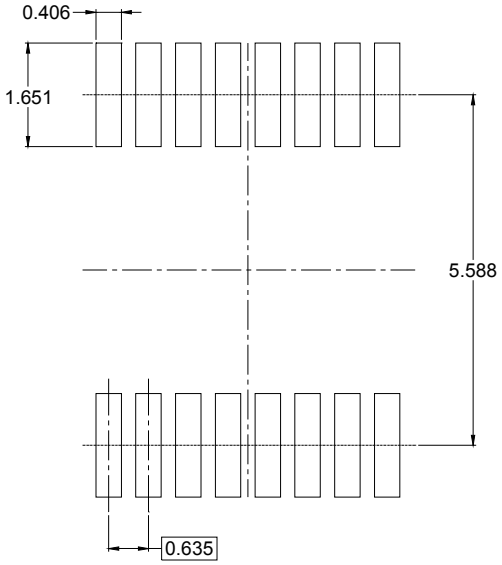


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

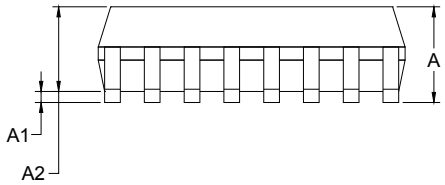
PACKAGE OUTLINE DIMENSIONS

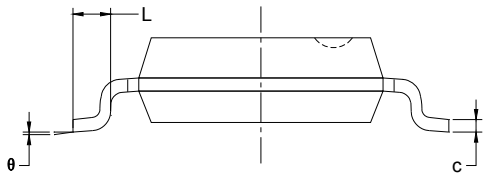
SSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

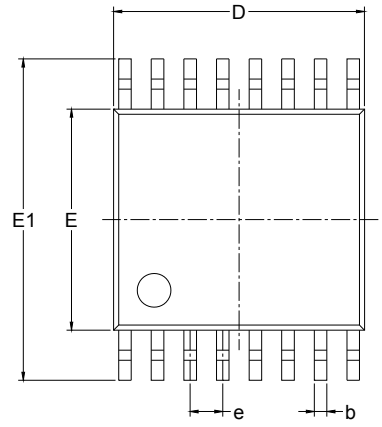


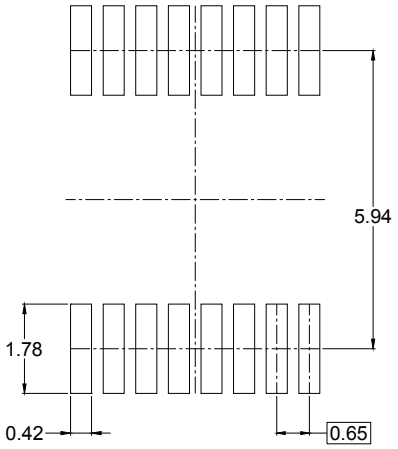


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635 BSC		0.025 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

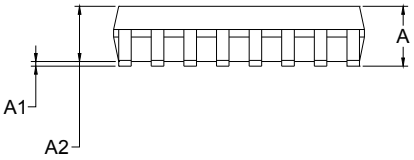
PACKAGE OUTLINE DIMENSIONS

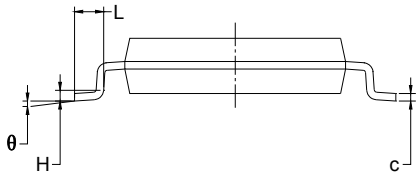
TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

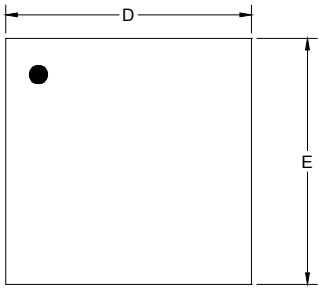




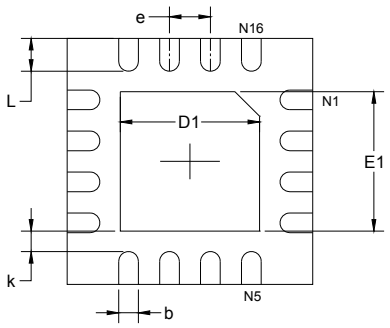
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

PACKAGE OUTLINE DIMENSIONS

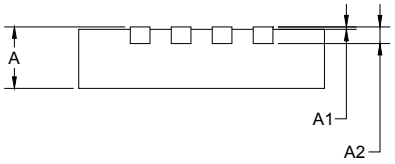
TQFN-3×3-16L



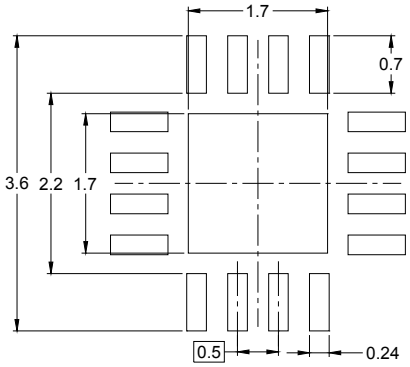
TOP VIEW



BOTTOM VIEW



SIDE VIEW

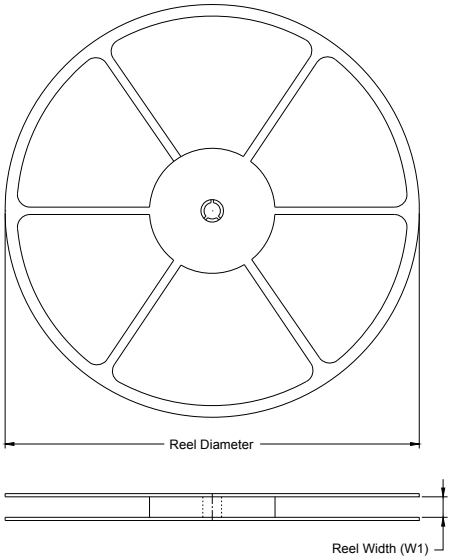


RECOMMENDED LAND PATTERN (Unit: mm)

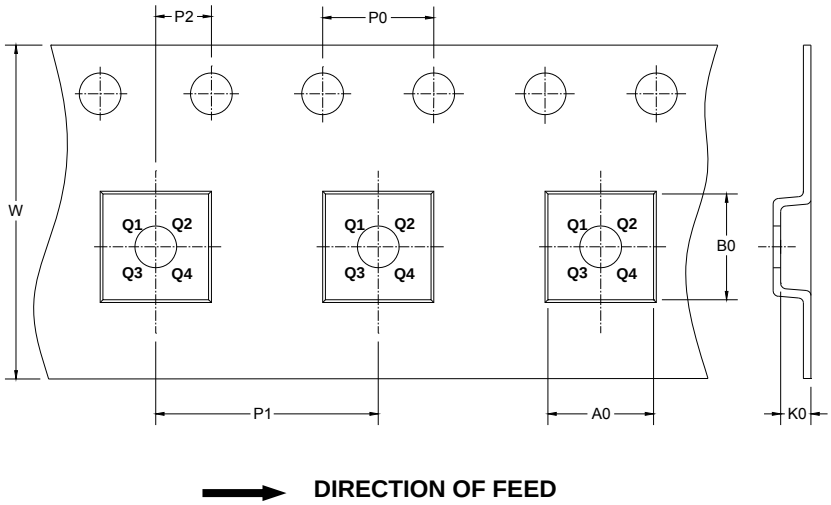
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



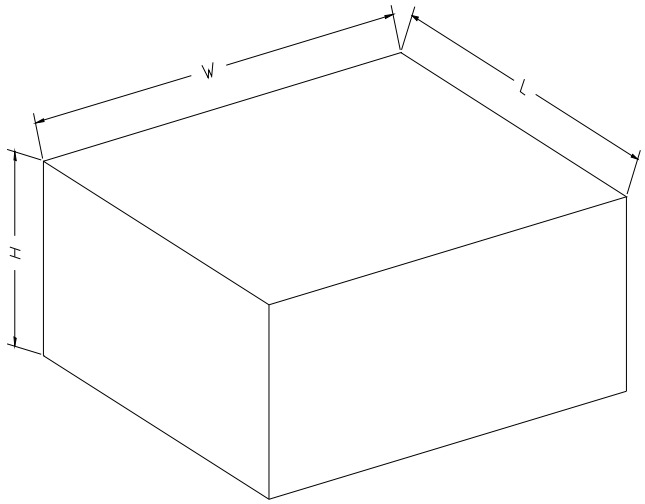
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13″	16.4	6.5	10.3	2.1	4.0	8.0	2.0	16.0	Q1
SSOP-16	13″	12.4	6.4	5.4	2.1	4.0	8.0	2.0	12.0	Q1
TSSOP-16	13″	12.4	6.9	5.6	1.2	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16L	13″	12.40	3.35	3.35	1.13	4.00	4.00	2.00	12.00	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002