SGM6502
8-Input, 6-Output Video Switch Matrix with Output Drivers, Input Clamp, and Bias Circuitry

GENERAL DESCRIPTION

The SGM6502 provides eight inputs that can be routed to any of six outputs. Each input can be routed to one or more outputs, but only one input may be routed to any output.

Each input supports an integrated clamp option to set the output sync tip level of video with sync to ~600mV. Alternatively, the input may be internally biased to center output signals without sync (Chroma, Pb, Pr) at ~1.3V.

All outputs are designed to drive a 150Ω DC-coupled load. Each output can be programmed to provide either 0dB or 6dB of signal gain.

Input-to-output routing and input bias mode functions are controlled via an I^2C-compatible digital interface.

The SGM6502 is available in Green TSSOP24 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **8 x 6 Crosspoint Switch Matrix**
- **One - to - One or One - to - Many Input - to - Output Switching**
- **I^2C - Compatible Digital Interface, Standard Mode**
- **Supports SD, PS, and HD Video**
- **Input Clamp and Bias Circuitry**
- **Doubly Terminated 75Ω Cable Drivers**
- **Programmable 0dB or 6dB Gain**
- **AC- or DC-Coupled Inputs**
- **AC- or DC-Coupled Outputs**
- **Single Supply: 3.1V to 5.5V**
- **Green TSSOP24 Package**

APPLICATIONS

Video Distribution
TV and HDTV Sets
Cable and Satellite Set-Top Boxes
A / V Switchers
Personal Video Recorders (PVR)
Security and Surveillance
Automotive (In-Cabin Entertainment)

PACKAGE/ORDERING INFORMATION

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION	MARKING INFORMATION
SGM6502	SGM6502YTS24G/TR	TSSOP24	Tape and Reel, 2500	SGM6502YTS24

ABSOLUTE MAXIMUM RATINGS

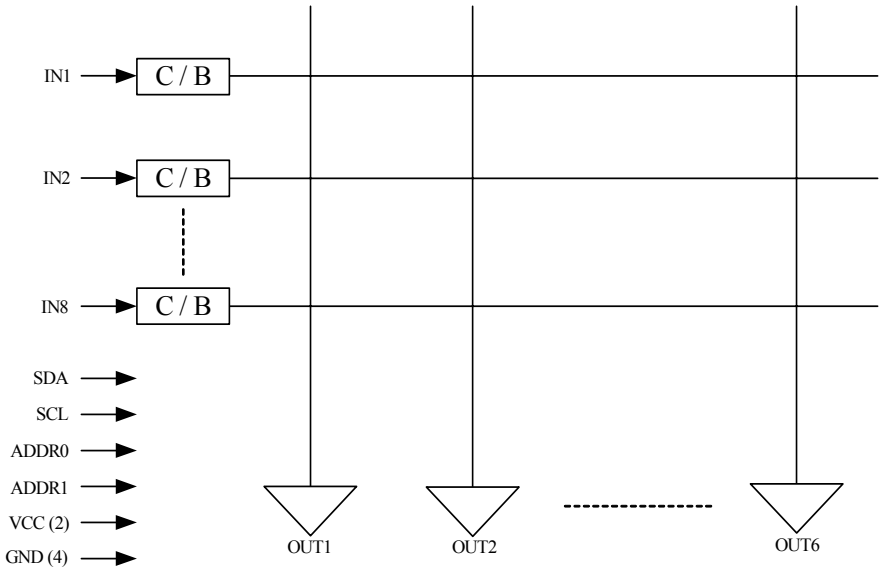
DC Supply Voltage ..... -0.3V to 6V
Analog and Digital I / O ..... -0.3V to V_{CC} + 0.3V
Output Current Any One Channel, Do Not Exceed 40mA
Storage Temperature Range ..... -65℃ to +150℃
Junction Temperature ..... 150℃
Operating Temperature Range ..... -40℃ to +85℃
Lead Temperature Range (Soldering 10 sec) ..... 260℃
ESD Susceptibility
HBM 8000V
MM 400V

NOTES
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

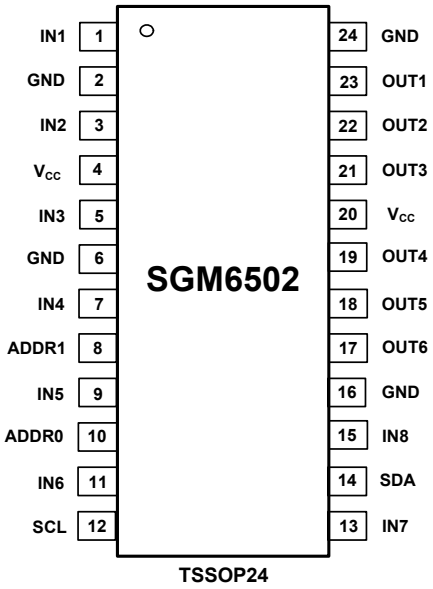
CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



TSSOP24

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	IN1	Input, channel 1
2	GND	Must be tied to ground
3	IN2	Input, channel 2
4	V_{CC}	Positive power supply
5	IN3	Input, channel 3
6	GND	Must be tied to ground
7	IN4	Input, channel 4
8	ADDR1	Selects I^2C address
9	IN5	Input, channel 5
10	ADDR0	Selects I^2C address
11	IN6	Input, channel 6
12	SCL	Serial clock for I^2C port
13	IN7	Input, channel 7
14	SDA	Serial data for I^2C port
15	IN8	Input, channel 8
16	GND	Must be tied to ground
17	OUT6	Output, channel 6
18	OUT5	Output, channel 5
19	OUT4	Output, channel 4
20	V_{CC}	Positive power supply
21	OUT3	Output, channel 3
22	OUT2	Output, channel 2
23	OUT1	Output, channel 1
24	GND	Must be tied to ground

ELECTRICAL CHARACTERISTICS

(T_A = 25℃, V_{CC} = 5V, V_{IN} = 1V_{PP}, input bias mode, one - to - one routing, 6dB gain, all inputs AC-coupled with 0.1μF, unused inputs AC-terminated through 75Ω to GND, all outputs AC-coupled with 220μF into 150Ω, referenced to 400kHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage Range			3.1	5	5.5	V
DC PERFORMANCE						
Video Output Range	V_{OUT}			2.8		V_{PP}
Supply Current	I_Q	No Load, All Outputs Enabled		60.8		mA
DC Input Level	V_{clamp}	Clamp Mode, All Gain Settings		0.42		V
DC Output Level		Clamp Mode, 0dB Gain Setting		0.42		V
DC Output Level		Clamp Mode, 6dB Gain Setting		0.84		V
DC Input Level	V_{bias}	Bias Mode, All Gain Settings		0.65		V
DC Output Level		Bias Mode, 0dB Gain Setting		0.65		V
DC Output Level		Bias Mode, 6dB Gain Setting		1.3		V
Power Supply Rejection Ratio	PSRR	All Channels, DC		80		dB
AC PERFORMANCE						
Channel Gain	AV_{0dB}	DC, All Channels, 0dB Gain Setting		0		dB
Channel Gain	AV_{6dB}	DC, All Channels, 6dB Gain Setting		6		dB
-1dB Bandwidth	f_{-1dB}	V_{OUT} = 1.4V_{PP}		67		MHz
-3dB Bandwidth	f_C	V_{OUT} = 1.4V_{PP}		88		MHz
Differential Gain	DG	V_{CC} = 5.0V, 4.43MHz		0.1		%
Differential Phase	DP	V_{CC} = 5.0V, 4.43MHz		0.4		°
SD Output Distortion	THD_{SD}	V_{OUT} = 1.4V_{PP}, 5MHz, V_{CC} = 5.0V		0.26		%
HD Output Distortion	THD_{HD}	V_{OUT} = 1.4V_{PP}, 22MHz, V_{CC} = 5.0V		0.93		%
Input Crosstalk	X_{TALK1}	1MHz, V_{OUT} = 2V_{PP}		-77		dB
Input Crosstalk	X_{TALK2}	15MHz, V_{OUT} = 2V_{PP}		-55		dB
Output Crosstalk	X_{TALK3}	1MHz, V_{OUT} = 2V_{PP}		-73		dB
Output Crosstalk	X_{TALK4}	15MHz, V_{OUT} = 2V_{PP}		-48		dB
Multi-Channel Crosstalk	X_{TALK5}	4.43MHz, V_{OUT} = 2V_{PP}		-55		dB
Multi-Channel Crosstalk	X_{TALK6}	6.5MHz, V_{OUT} = 2V_{PP}		-53		dB
Multi-Channel Crosstalk	X_{TALK7}	9MHz, V_{OUT} = 2V_{PP}		-50		dB
Signal-to-Noise Ratio	SNR_{SD}	NTC-7 Weighting, 4.2MHz LP, 100kHz HP		78		dB
Channel Noise	V_{NOISE}	400kHz to 100MHz, Input Referred		20		nV/$\sqrt{Hz}$
Amplifier Recovery Time	AMP_{ON}	Post I^2C Programming		200		ns

Specifications subject to changes without notice.

DIGITAL INTERFACE

The I^2C - compatible interface is used to program output enables, input-to-output routing, and input bias configuration. The I^2C address of the SGM6502 is 0x06 (0000 0110) with the ability to offset based upon the values of the ADDR0 and ADDR1 inputs. Offset addresses are defined below:

ADDR1	ADDR0	Binary	Hex
0	0	0000 0110	0x06
0	1	0100 0110	0x46
1	0	1000 0110	0x86
1	1	1100 0110	0xC6

Data and address data of eight bits each are written to the SGM6502 I^2C address register to access control functions. For efficiency, a single data register is shared between two outputs for input selection. More than one output can select the same input channel for one - to - many routing.

The clamp / bias control bits are written to their own internal address since they should remain the same regardless of signal routing. They are set based on the input signal that is connected to the SGM6502.

All undefined addresses may be written without effect.

Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
In-A	4 bits	Write	0	3:0	Input selected to drive this output: 0000 = OFF(1), 0001 = IN1, 0010 = IN2, 1000 = IN8
In-B	4 bits	Write	0	7:4	Input selected to drive this output: 0000 = OFF(1), 0001 = IN1, 0010 = IN2, 1000 = IN8

Note:

1. When the OFF input selection is used, the output amplifier is powered down and enters a high-impedance state.

Output Control Register MAP

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUT1,2	0x00	B3-Out2	B2-Out2	B1-Out2	B0-Out2	B3-Out1	B2-Out1	B1-Out1	B0-Out1
OUT3,4	0x01	B3-Out4	B2-Out4	B1-Out4	B0-Out4	B3-Out3	B2-Out3	B1-Out3	B0-Out3
OUT5,6	0x02	B3-Out6	B2-Out6	B1-Out6	B0-Out6	B3-Out5	B2-Out5	B1-Out5	B0-Out5

Clamp Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Clmp	1 bit	Write	0	7:0	Clamp / Bias selection: 1 = Clamp, 0 = Bias

Clamp Control Register Map

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLAMP	0x03	Clmp8	Clmp7	Clmp6	Clmp5	Clmp4	Clmp3	Clmp2	Clmp1

Gain Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Gain	1 bit	Write	0	7:0	Output Gain selection: 0 = 6dB, 1 = 0dB

Gain Control Register Map

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GAIN	0x04	Unused	Unused	Gain6	Gain5	Gain4	Gain3	Gain2	Gain1

I²C BUS CHARACTERISTICS

(T_A = 25℃, V_{CC} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Low	V_{IL}	SDA, SCL, ADDR	0		1.5	V
Digital Input High	V_{IH}	SDA, SCL, ADDR	3.0		V_{CC}	V
Clock Frequency	f_{SCL}	SCL		100		kHz
Input Rise Time	tr	1.5V to 3V		1000		ns
Input Fall Time	tf	1.5V to 3V		300		ns
Clock Low Period	t_{LOW}			4.7		μs
Clock High Period	t_{HIGH}			4.0		μs
Data Set-up Time	$t_{SU, DAT}$			300		ns
Data Hold Time	$t_{HD, DAT}$			0		ns
Set-up Time from Clock High to Stop	$t_{SU, STO}$			4.0		μs
Start Set-up Time following a Stop	t_{BUF}			4.7		μs
Start Hold Time	$t_{HD, STA}$			4.0		μs
Start Set-up Time following Clock Low to High	$t_{SU, STA}$			4.7		μs

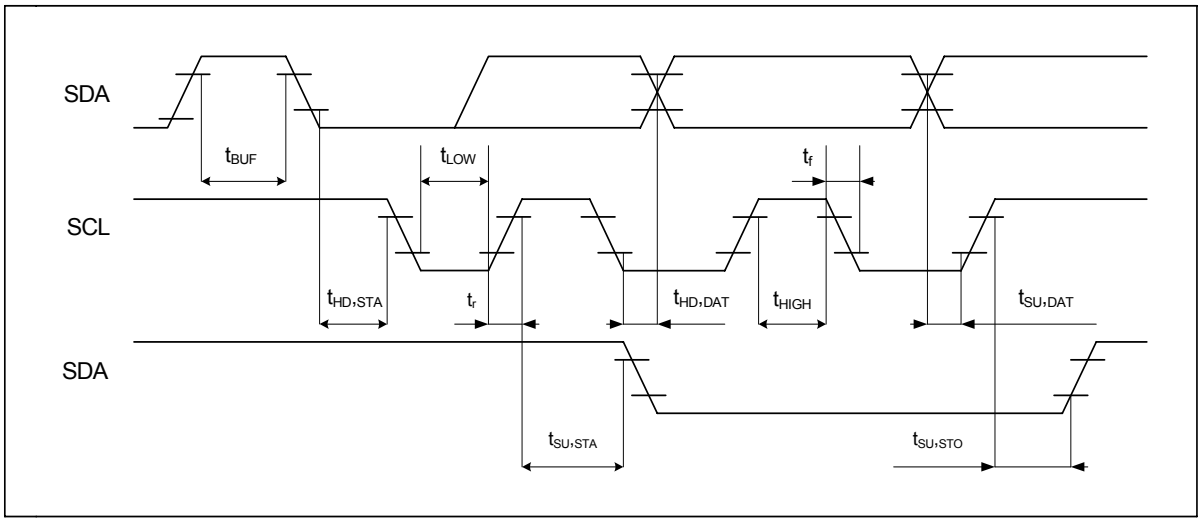


Figure 3. I²C Bus Timing

I²C INTERFACE

Operation

The I²C-compatible interface conforms to the I²C specification for Standard Mode. Individual addresses may be written, but there is no read capability. The interface consists of two lines: a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply through an external resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line during this time are interpreted as control signals.

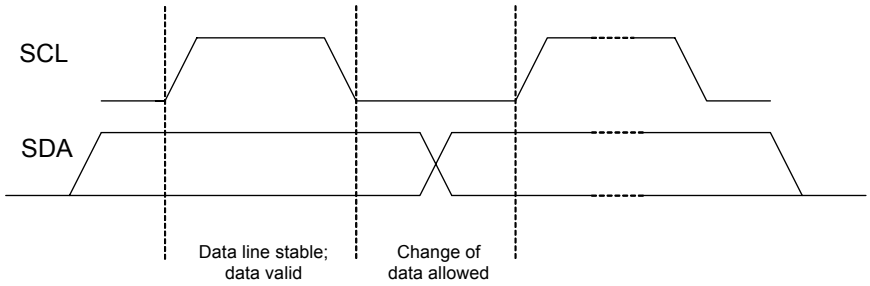


Figure 4. Bit Transfer

START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH - to - LOW transition of the data line, while the clock is HIGH, is defined as start condition (S).

A LOW - to - HIGH transition of the data line, while the clock is HIGH, is defined as stop condition (P).

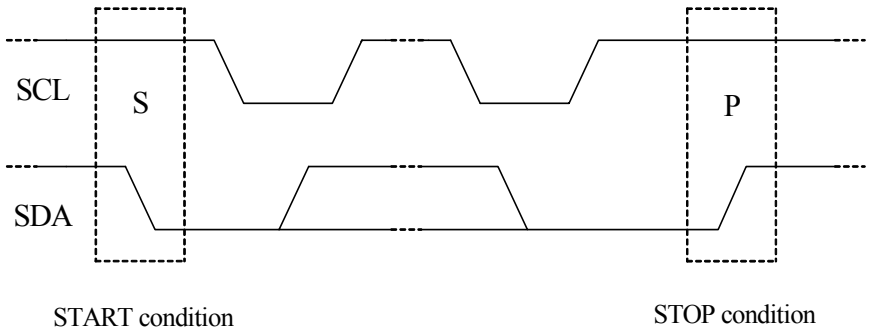


Figure 5. START and STOP conditions

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter while the master generates an extra acknowledge-related clock pulse. The slave receiver addressed must generate an acknowledge after the reception of each byte. A master receiver must generate an acknowledge after the reception of each byte clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

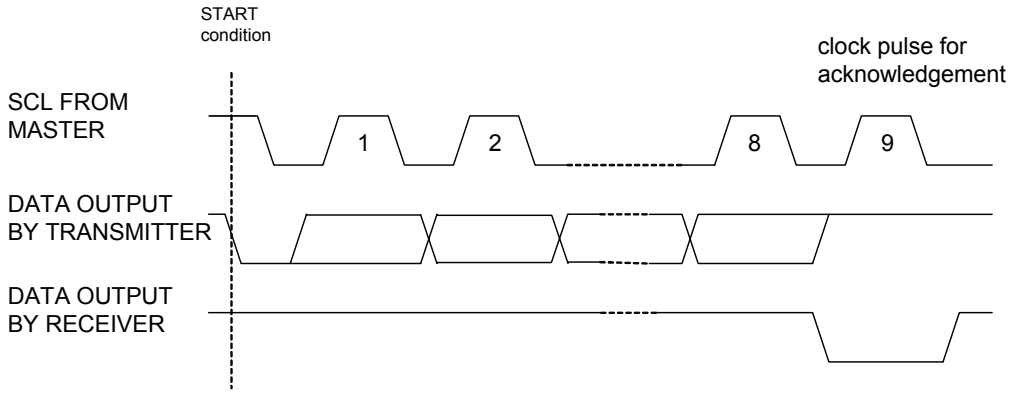


Figure 6. Acknowledgement on the I²C Bus

I²C Bus Protocol

Before any data is transmitted on the I²C bus, the device which is to respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C bus configuration for a data write to the SGM6502 is shown in Figure 7.

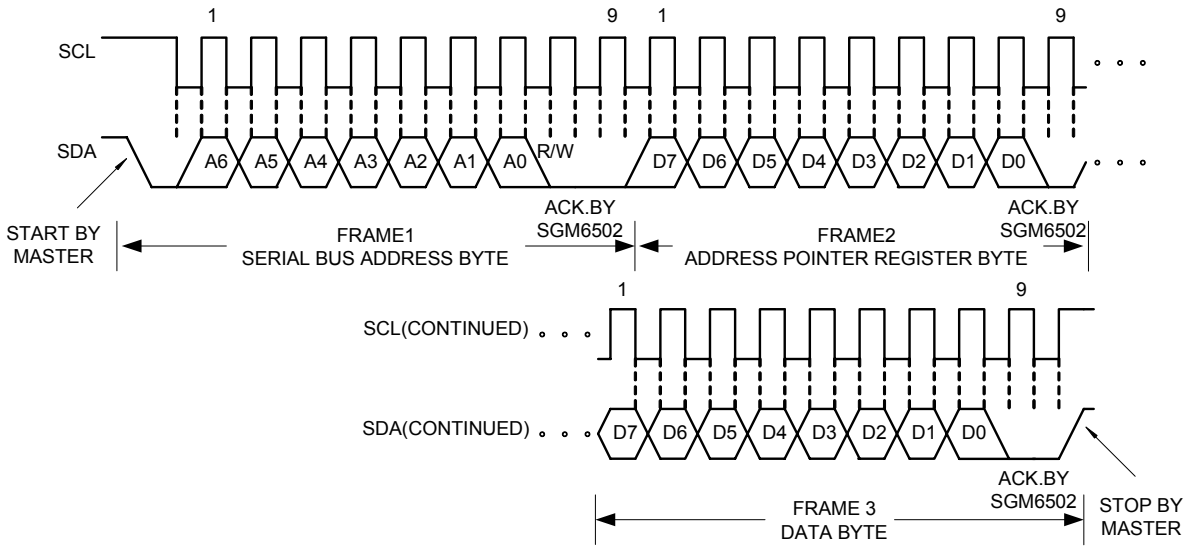


Figure 7. Write Register Address to Pointer Register; Write Data to Selected Register

3.3V Operation

The SGM6502 operates from a single 3.3V supply. With V_{CC} = 3.3V, the digital input low (V_{IL}) is 0V to 1V and the digital input high (V_{IH}) is 1.8V to 2.9V.

APPLICATION NOTES

Input Clamp / Bias Circuitry

The SGM6502 can accommodate AC- or DC-coupled inputs. Internal clamping and bias circuitry are provided to support AC-coupled inputs. These are selectable through the CLMP bits via the I^2C-compatible interface. For DC-coupled inputs, the device should be programmed to use the 'bias' input configuration. In this configuration, the input is internally biased to 650mV through a 100kΩ resistor. Distortion is optimized with the output levels set between 250mV above ground and 500mV below the power supply.

With AC-coupled inputs, the SGM6502 uses a simple clamp rather than a full DC-restore circuit. For video signals with and without sync; (Y, CV, R, G, B), the lowest voltage at the output pins is clamped to approximately 600mV above ground.

If symmetric AC-coupled input signals are used (Chroma, Pb, Pr, Cb, Cr), the bias circuit can be used to center them within the input common range. The average DC value at the output is approximately 1.3V.

Figure 8 shows the clamp mode input circuit and the internally controlled voltage at the input pin for AC-coupled inputs.

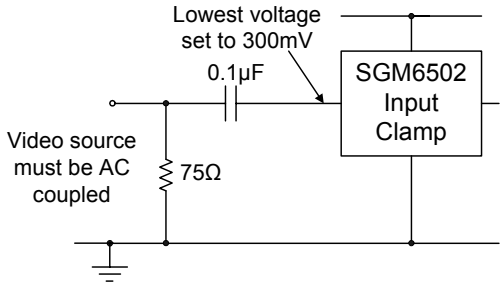


Figure 8. Clamp Mode Input Circuit

Figure 9 shows the bias mode input circuit and the internally controlled voltage at the input pin for AC-coupled inputs.

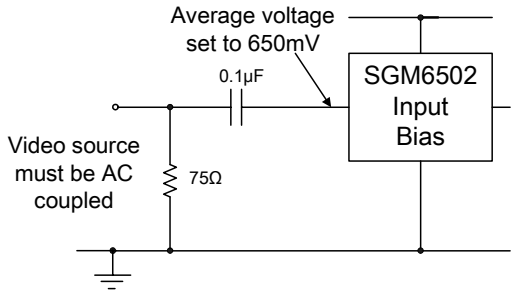


Figure 9. Bias Mode Input Circuit

Output Configuration

The SGM6502 outputs may be AC or DC-coupled. DC-coupled loads can drive a 150Ω load. AC-coupled outputs are capable of driving a single, doubly terminated video load of 150Ω. An external transistor is needed to drive DC low-impedance loads. DC-coupled outputs should be connected as indicated in Figure 10.

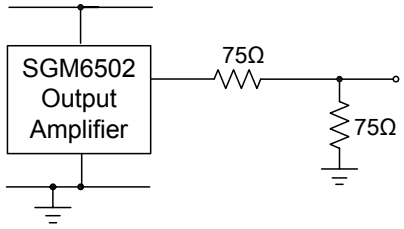


Figure 10. DC-Coupled Load Connection

Configure AC-coupled loads as shown in Figure 11.

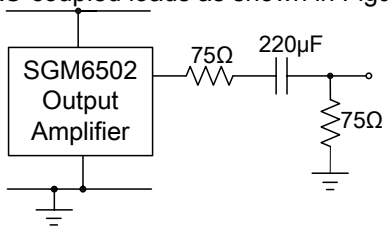


Figure 11. AC-Coupled Load Connection

When an output channel is not connected to an input, the input to that particular channel's amplifier is forced to approximately 150mV. The output amplifier is still active unless specifically disabled by the I^2C interface. Voltage output levels depend on the programmed gain for that channel.

Driving Capacitive Loads

When driving capacitive loads, use a 10Ω-series resistance to buffer the output, as indicated in Figure 12.

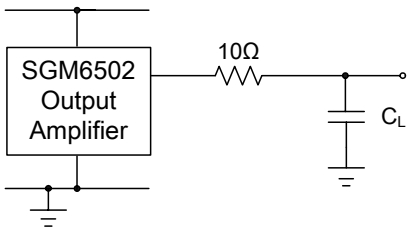


Figure 12. Driving Capacitive Loads

Crosstalk

Crosstalk is an important consideration when using the SGM6502. Input and output crosstalk represent the two major coupling modes that may be present in a typical application. Input crosstalk is crosstalk in the input pins and switches when the interfering signal drives an open switch. It is dominated by inductive coupling in the package lead frame between adjacent leads. It decreases rapidly as the interfering signal moves further away from the pin adjacent to the input signal selected. Output crosstalk is coupling from one driven output to another active output. It decreases with increasing load impedance as it is caused mainly by ground and power coupling between output amplifiers. If a signal is driving an open switch, its crosstalk is mainly input crosstalk. If it is driving a load through an active output, its crosstalk is mainly output crosstalk.

Input and output crosstalk measurements are performed with the test configuration shown in Figure 13.

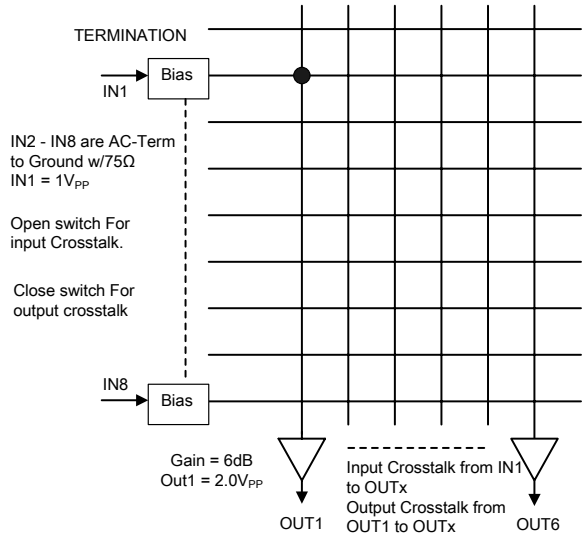


Figure 13. Test Configuration for Crosstalk

For input crosstalk, the switch is open and all inputs are in bias mode. Channel 1 input is driven with a 1Vpp signal, while all other inputs are AC terminated with 75Ω. All outputs are enabled and crosstalk is measured from IN1 to any output.

For output crosstalk, the switch is closed. Crosstalk from OUT1 to any output is measured.

Crosstalk from multiple sources into a given channel is measured with the setup shown in Figure 14. Input In1 is driven with a 1Vpp pulse source and connected to outputs Out1 to Out5. Input In6 is driven with a secondary, asynchronous gray field video signal and is connected to Out6. All other inputs are AC terminated with 75Ω. Crosstalk effects on the gray field are measured and calculated with respect to a standard 1Vpp output measured at the load.

If not all inputs and outputs are needed, avoid using adjacent channels to reduce crosstalk.

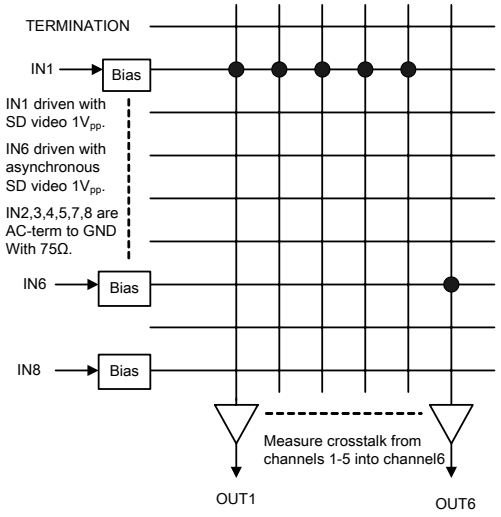


Figure 14. Test Configuration for Multi-Channel Crosstalk

Layout Consideration

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10μF and 0.1μF ceramic power supply bypass capacitors.
- Place the 0.1μF capacitor within 0.1 inches of the device power pin.
- Place the 10μF capacitor within 0.75 inches of the device power pin.
- For multilayer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body by at least 0.5 inches on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players, are at +70ºC; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane) each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70μm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Modeling techniques can provide a first-order approximation.

Power Dissipation

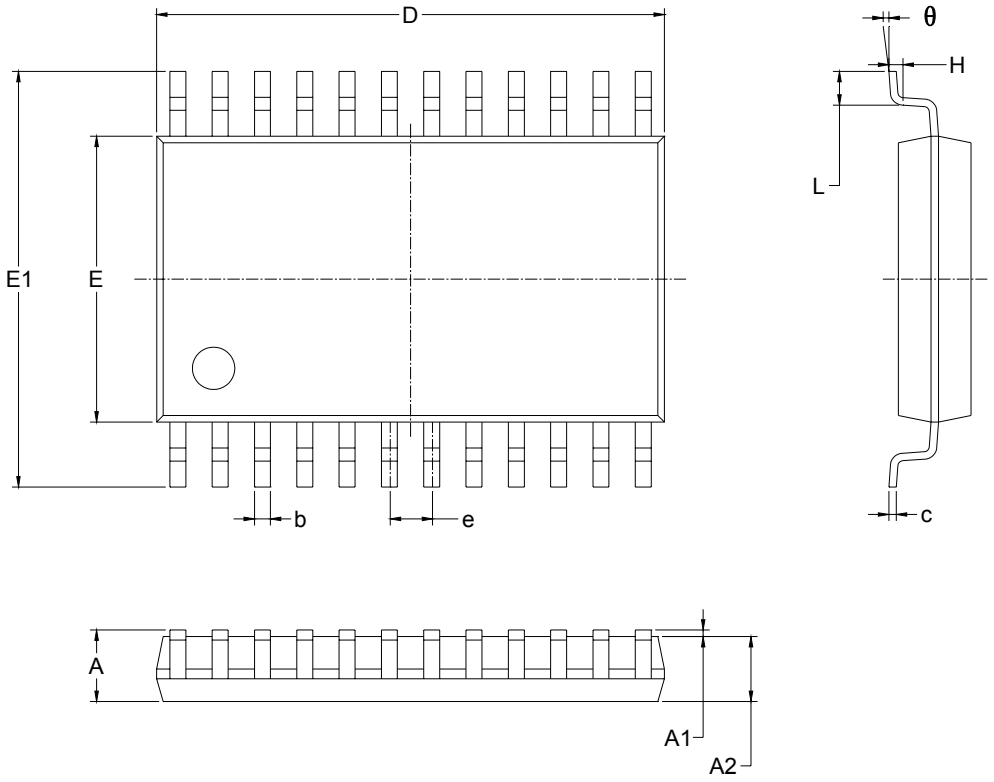
Worst-case, additional die power due to DC loading can be estimated at $Vcc^2/4Rload$ per output channel. This assumes a constant DC output voltage of $V_{CC}/2$. For 5V V_{CC} with a dual DC video load, add 25/(4*75) = 83mW, per channel.

Applications for the SGM6502 Video Switch Matrix

The increased demand for consumer multimedia systems has created a large challenge for system designers to provide cost-effective solutions to capitalize on the growth potential in graphics display technologies. These applications require cost-effective video switching and filtering solutions to deploy high-quality display technologies rapidly and effectively to the target audience. Areas of specific interest include HDTV, media centers, and automotive infotainment (such as navigation, in-cabin entertainment, and back-up cameras). In all cases, the advantages the integrated video switch matrix provides are high-quality video switching specific to the application, as well as video input clamps and on-chip, low impedance output cable drivers with switchable gain. Generally the largest application for a video switch is for the front-end of an HDTV. This is used to take multiple inputs and route them to their appropriate signal paths (main picture and picture-in-picture, or PiP). These are normally routed into ADCs that are followed by decoders. Technologies for HDTV include LCD, plasma, and CRT, which have similar analog switching circuitry.

PACKAGE OUTLINE DIMENSIONS

TSSOP24



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.100		0.043
A1	0.020	0.150	0.001	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°