SGM6510
16-Input, 4-Output Crosspoint Switch

GENERAL DESCRIPTION

The SGM6510 crosspoint switch provides flexible options for applications. The 16 inputs can be routed to any of 4 outputs. Each input can be routed to one or more outputs, but only one input can be routed to any one output. More than one output can connect to the same input channel for one-to-many routing. The input to output routing is controlled via an I^2C-compatible digital interface.

For analog signal switching application, 4 outputs can be 4 single outputs or 2 differential outputs depending on configuration. Crosspoint structure can reduce PCB complexity. For digital signal switching, SGM6510 supports up to 400kHz digital signal.

The resistance profile of SGM6510 is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. For video application, SGM6510 supports up to 1080p or VGA video.

The SGM6510 is available in Green TSSOP-28 and TQFN-4×4-28L packages. It operates over an ambient temperature range of -40℃ to +85℃.

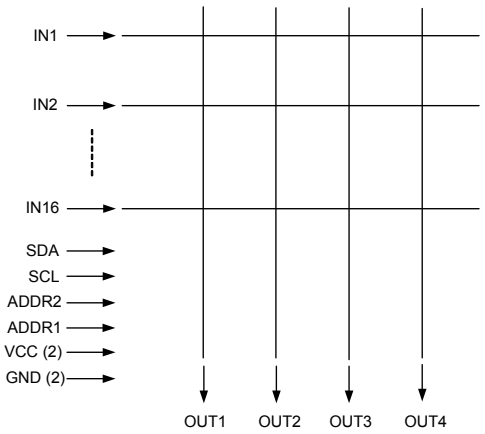
FEATURES

- **Supply Range: 2.7V to 5.5V**
- **16 × 4 Crosspoint Switch**
- **One-to-One or One-to-Many Output Switching**
- **Supports Bidirectional Transmission**
- **I^2C-Compatible Digital Interface, Standard Mode**
- **Supports XVGA (1280 × 960) Video**
- **Supports -110dB Off Isolation for 1kHz Audio Signal**
- **Supports -110dB Channel-to-Channel Crosstalk for 1kHz Audio Signal**
- **Supports Low Noise Analog Signal Switching**
- **-3dB Bandwidth: 120MHz**
- **Available in Green TSSOP-28 and TQFN-4×4-28L Packages**
- **Extended Industrial Temperature Range: -40℃ to +85℃**

APPLICATIONS

Video and Audio Matrix Switching System
Audio and Video Receiver
Automotive Entertainment System
Data Acquisition and Control System

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6510	TSSOP-28	-40℃ to +85℃	SGM6510YTS28G/TR	SGM6510 YTS28 XXXXX	Tape and Reel, 2500
	TQFN-4×4-28L	-40℃ to +85℃	SGM6510YTQH28G/TR	SGM6510 YTQH28 XXXXX	Tape and Reel, 3000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage……....-0.3V to 6V
Analog and Digital I/O…….-0.3V to V_{CC} + 0.3V
Continuous Current IN, OUT……..…10mA
Storage Temperature Range……-65℃ to +150℃
Junction Temperature……..150℃
Operating Temperature Range……...-40℃ to +85℃
Lead Temperature (Soldering 10 sec)..……..…….260℃
ESD Susceptibility
HBM 7000V
MM 300V

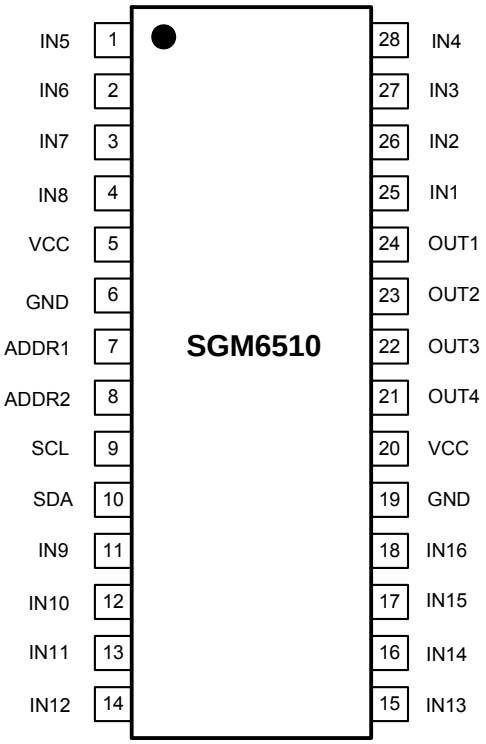
NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

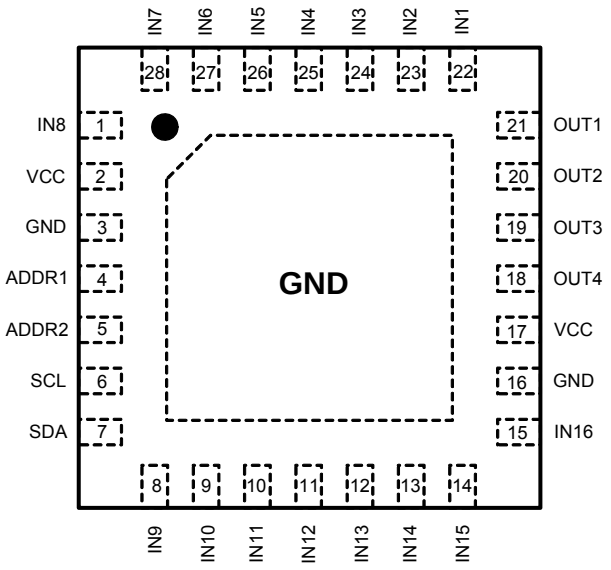
This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATIONS (TOP VIEW)



TSSOP-28



TQFN-4×4-28L

PIN DESCRIPTION

PIN		NAME	DESCRIPTION
TSSOP-28	TQFN-4×4-28L		
1	26	IN5	Input. Channel 5.
2	27	IN6	Input. Channel 6.
3	28	IN7	Input. Channel 7.
4	1	IN8	Input. Channel 8.
5, 20	2, 17	VCC	Positive Power Supply.
6, 19	3, 16	GND	Ground.
7	4	ADDR1	Selects I^2C Address.
8	5	ADDR2	Selects I^2C Address.
9	6	SCL	Serial Clock for I^2C Port.
10	7	SDA	Serial Data for I^2C Port.
11	8	IN9	Input. Channel 9.
12	9	IN10	Input. Channel 10.
13	10	IN11	Input. Channel 11.
14	11	IN12	Input. Channel 12.
15	12	IN13	Input. Channel 13.
16	13	IN14	Input. Channel 14.
17	14	IN15	Input. Channel 15.
18	15	IN16	Input. Channel 16.
21	18	OUT4	Output. Channel 4.
22	19	OUT3	Output. Channel 3.
23	20	OUT2	Output. Channel 2.
24	21	OUT1	Output. Channel 1.
25	22	IN1	Input. Channel 1.
26	23	IN2	Input. Channel 2.
27	24	IN3	Input. Channel 3.
28	25	IN4	Input. Channel 4.
—	Exposed Pad	GND	Exposed pad should be soldered to PCB board and connected to GND or left floating.

I^2C ADDRESS SELECTION TABLE

ADDR2	ADDR1	I^2C ADDRESS
0	0	0x06 (0000 0110)
0	1	0x46 (0100 0110)
1	0	0x86 (1000 0110)
1	1	0xC6 (1100 0110)

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, Full = -40℃ to +85℃. Typical values are at V_{CC} = +5.0V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{IN}, V_{OUT}			Full	0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		30	37	Ω
				Full			42	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 4.5V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		4	7.5	Ω
				Full			8.6	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 4.5V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		8	12	Ω
				Full			12.5	
Source OFF Leakage Current	I_{OFF}	V_{CC} = 5.5V, V_{IN} = 4.5V/1V, V_{OUT} = 1V/4.5V		Full			1	μA
Channel ON Leakage Current	I_{ON}	V_{CC} = 5.5V, V_{OUT} = 1V/4.5V, V_{IN} = 1V/4.5V or floating		Full			1	μA
Supply Current	I_{CC}	V_{CC} = 5.5V		Full		15	60	μA
DYNAMIC CHARACTERISTICS								
Break-Before-Make Time Delay	t_D	V_{IN} = 3V, R_L = 50Ω, C_L = 35pF		+25℃		7		ns
Charge Injection	Q	V_G = GND, R_G = 0Ω, C_L = 1.0nF, Q = C_L × V_{OUT}		+25℃		7		pC
Off Isolation	O_{ISO}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-78		dB
			10MHz	+25℃		-58		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
Channel-to-Channel Crosstalk	X_{TALK}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-75		dB
			10MHz	+25℃		-55		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
-3dB Bandwidth	BW	V_{IN} = 0dBm, R_L = 75Ω		+25℃		120		MHz
Channel ON Capacitance	C_{ON}	f = 1MHz		+25℃		40		pF
Digital Input Capacitance	C_{DIN}	V_{CC} = 5V		+25℃		7		pF

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, Full = -40℃ to +85℃. Typical values are at V_{CC} = +3.0V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{IN}, V_{OUT}			Full	0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 2.7V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		60	78	Ω
				Full			82	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 2.7V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		4	9.5	Ω
				Full			10.5	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 2.7V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		30	43.5	Ω
				Full			44.5	
Source OFF Leakage Current	I_{OFF}	V_{CC} = 3.6V, V_{IN} = 3.3V/0.3V, V_{OUT} = 0.3V/3.3V		Full			1	μA
Channel ON Leakage Current	I_{ON}	V_{CC} = 3.6V, V_{OUT} = 0.3V/3.3V, V_{IN} = 0.3V/3.3V or floating		Full			1	μA
Supply Current	I_{CC}	V_{CC} = 3.6V		Full		8	40	μA
DYNAMIC CHARACTERISTICS								
Break-Before-Make Time Delay	t_D	V_{IN} = 1.5V, R_L = 50Ω, C_L = 35pF		+25℃		10		ns
Charge Injection	Q	V_G = GND, R_G = 0Ω, C_L = 1.0nF, Q = C_L × V_{OUT}		+25℃		3		pC
Off Isolation	O_{ISO}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-78		dB
			10MHz	+25℃		-58		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
Channel-to-Channel Crosstalk	X_{TALK}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-75		dB
			10MHz	+25℃		-55		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
-3dB Bandwidth	BW	V_{IN} = 0dBm, R_L = 75Ω		+25℃		120		MHz
Channel ON Capacitance	C_{ON}	f = 1MHz		+25℃		45		pF
Digital Input Capacitance	C_{DIN}	V_{CC} = 3V		+25℃		7		pF

DIGITAL INTERFACE

The I^2C-compatible interface is used to program output enables, and input to output routing. The I^2C address of the SGM6510 can be programmed to 0x06 (0000 0110) or 0x46 (0100 0110) or 0x86 (1000 0110) or 0xC6 (1100 0110) by connecting ADDR2, ADDR1 pin to "LOW" or "HIGH".

Both data and address data, of eight bits each, are written to the I^2C address to access all the control functions.

There are separate internal addresses for each output. Each output's address includes bits to select an input channel. More than one output can connect to the same input channel for one-to-many routing. When the outputs are disabled, they are placed in a high-impedance state. This allows multiple SGM6510 devices to be paralleled to create a larger switch matrix. Typical output power-up time is less than 500ns.

All undefined addresses may be written without effect.

Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit (s)	Description
INx	5 bits	Write	0	Bit4:Bit0	Input selected to drive this output: 00000 = OFF, 00001 = IN1, 00010 = IN2, …, 01100 = IN12, …, 01111 = IN15, 10000 = IN16.

Output Control Register Map

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUT1	0x01	X	X	X	IN4	IN3	IN2	IN1	IN0
OUT2	0x02	X	X	X	IN4	IN3	IN2	IN1	IN0
OUT3	0x03	X	X	X	IN4	IN3	IN2	IN1	IN0
OUT4	0x04	X	X	X	IN4	IN3	IN2	IN1	IN0

NOTE: "X" means "don't care".

I²C BUS CHARACTERISTICS

(T_A = +25℃, V_{CC} = +5.0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Input Low	V_{IL}	SDA, SCL, ADDR	V_{CC} = 3V	0		0.6	V
			V_{CC} = 5V	0		0.6	
Digital Input High	V_{IH}	SDA, SCL, ADDR	V_{CC} = 3V	1.7		V_{CC}	V
			V_{CC} = 5V	2.5		V_{CC}	
Clock Frequency	f_{SCL}	SCL			100		kHz
Input Rise Time	t_r	1.5V to 3V			1000		ns
Input Fall Time	t_f	1.5V to 3V			300		ns
Clock Low Period	t_{LOW}				4.7		μs
Clock High Period	t_{HIGH}				4.0		μs
Data Set-up Time	$t_{SU, DAT}$				300		ns
Data Hold Time	$t_{HD, DAT}$				0		ns
Set-up Time from Clock High to Stop	$t_{SU, STO}$				4		μs
Start Set-up Time Following a Stop	t_{BUF}				4.7		μs
Start Hold Time	$t_{HD, STA}$				4		μs
Start Set-up Time Following Clock Low to High	$t_{SU, STA}$				4.7		μs

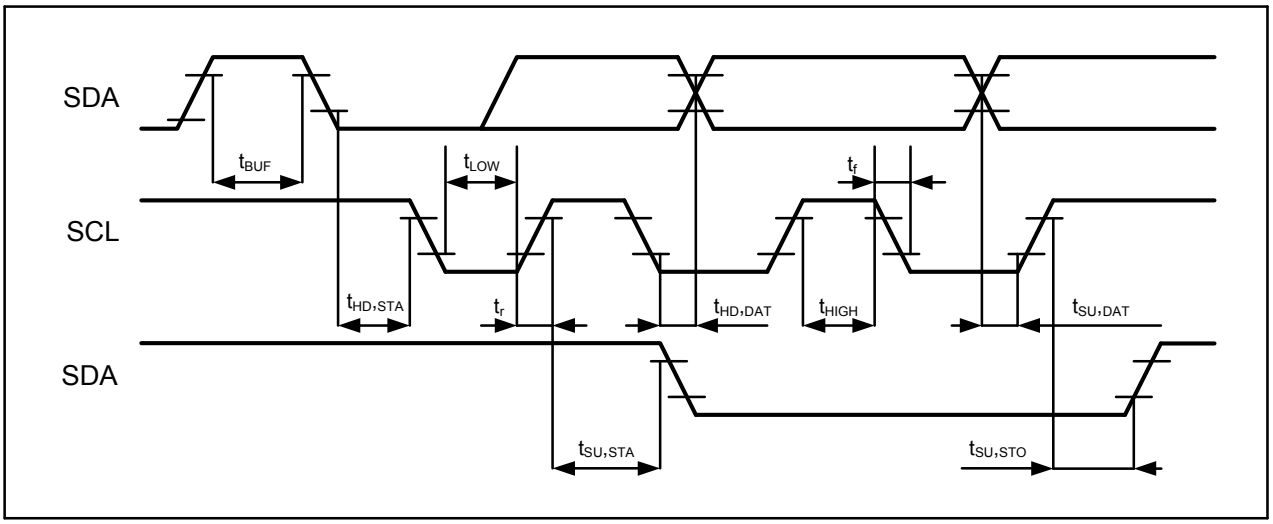


Figure 1. I²C Bus Timing

I²C INTERFACE

Operation

The I²C-compatible interface conforms to the I²C specification for standard mode. Individual addresses may be written, but there is no read capability. The interface consists of two lines: a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply through an external resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line during this time are interpreted as control signals.

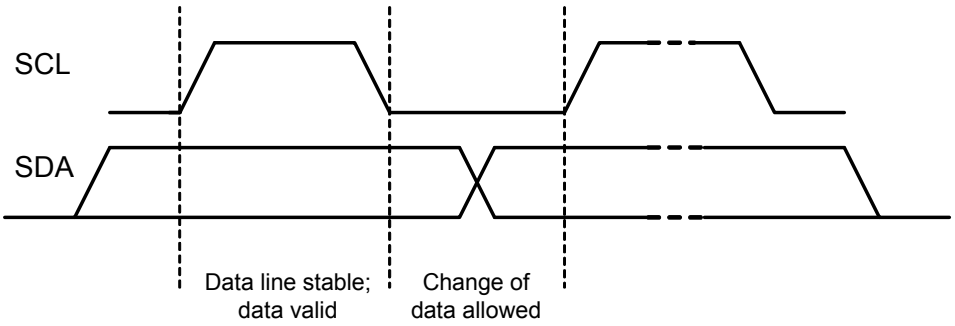


Figure 2. Bit Transfer

START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as START condition (S).

A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as STOP condition (P).

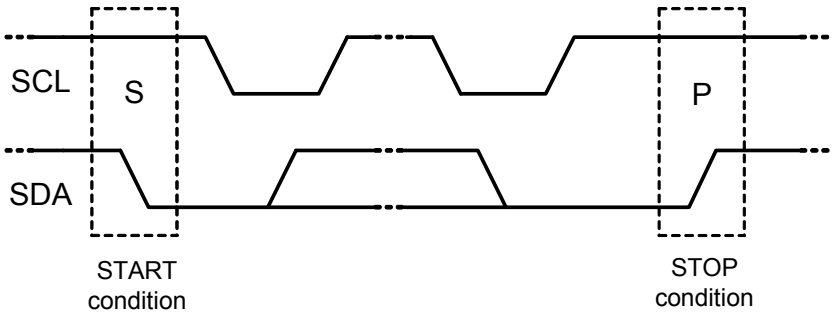


Figure 3. START and STOP Conditions

I²C INTERFACE

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter while the master generates an extra acknowledge-related clock pulse. The slave receiver addressed must generate an acknowledge after the reception of each byte. A master receiver must generate an acknowledge after the reception of each byte clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

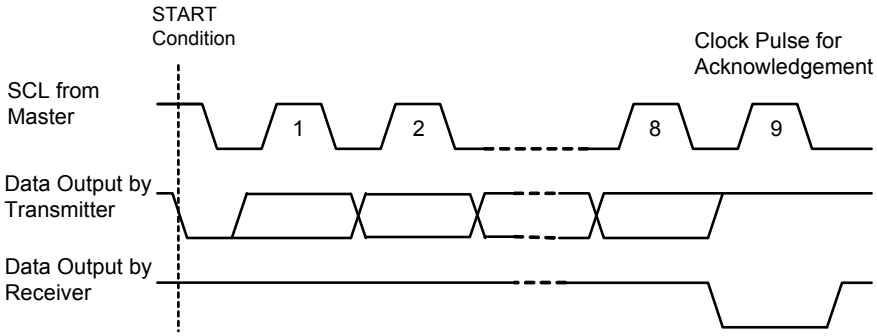


Figure 4. Acknowledgement on the I²C Bus

I²C Bus Protocol

Before any data is transmitted on the I²C bus, the device which is to respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C bus configuration for a data write to the SGM6510 is shown in Figure 5.

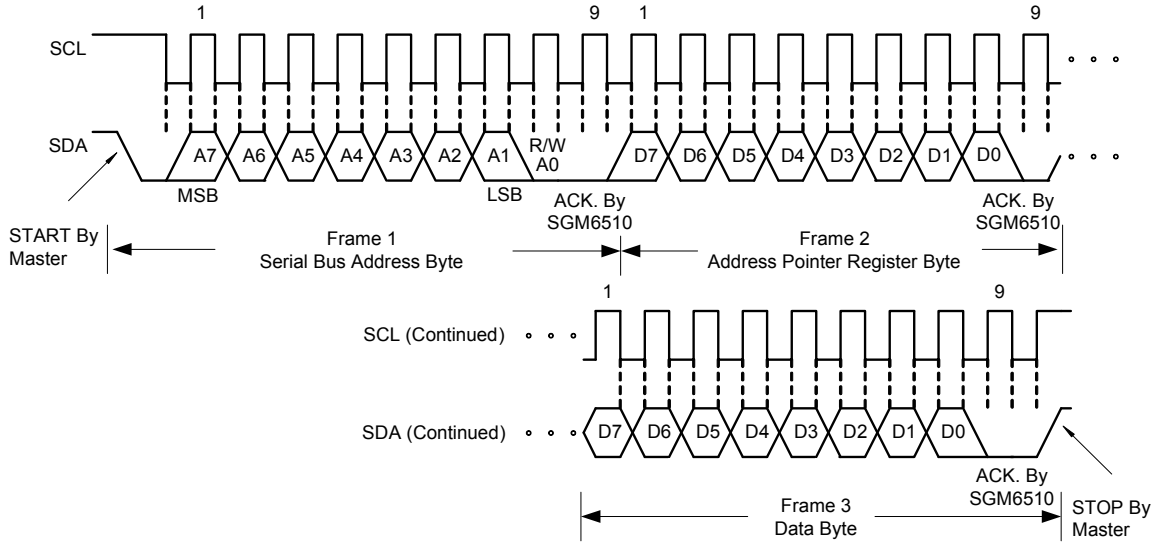


Figure 5. Write Register Address to Pointer Register; Write Data to Selected Register

APPLICATION NOTES

Layout Considerations

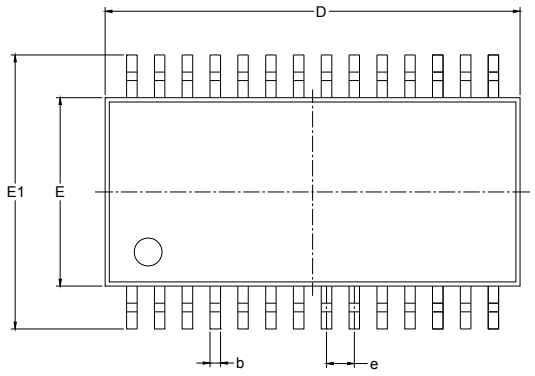
General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. SGMICRO offers a demonstration board to guide layout and aid device evaluation. The demo board is a four layers board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

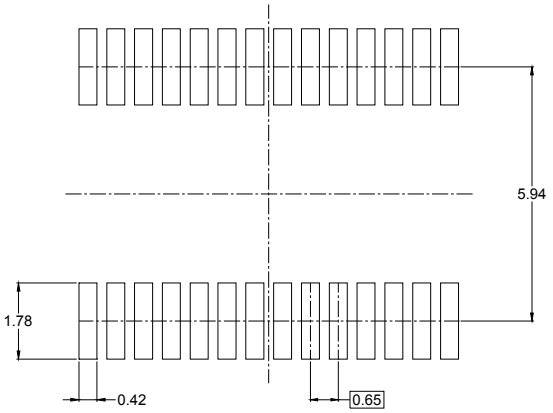
Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10μF and 0.1μF ceramic power supply bypass capacitors.
- Place the 0.1μF capacitor within 0.1 inches of the device power pin.
- Place the 10μF capacitor within 0.75 inches of the device power pin.
- For multilayer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body by at least 0.5 inches on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

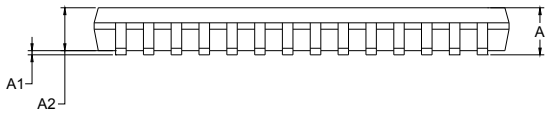
PACKAGE OUTLINE DIMENSIONS

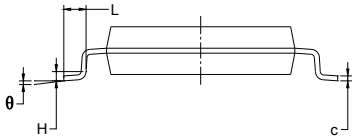
TSSOP-28





RECOMMENDED LAND PATTERN (Unit: mm)

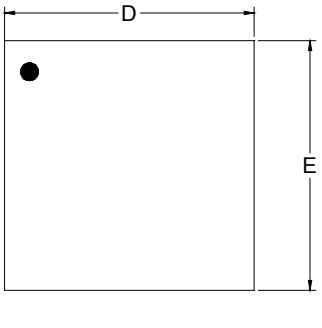




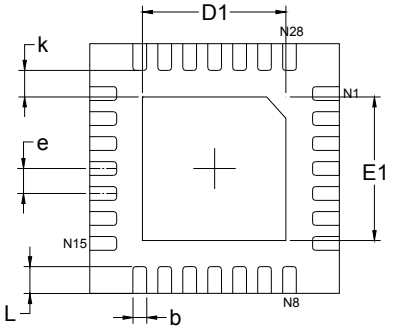
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.020	0.150	0.001	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

PACKAGE OUTLINE DIMENSIONS

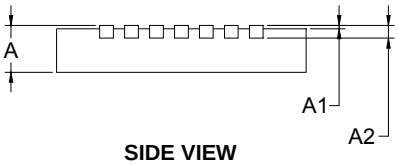
TQFN-4×4-28L



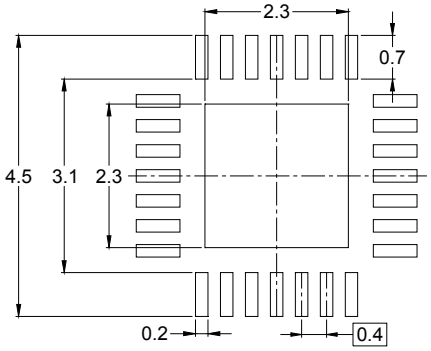
TOP VIEW



BOTTOM VIEW



SIDE VIEW

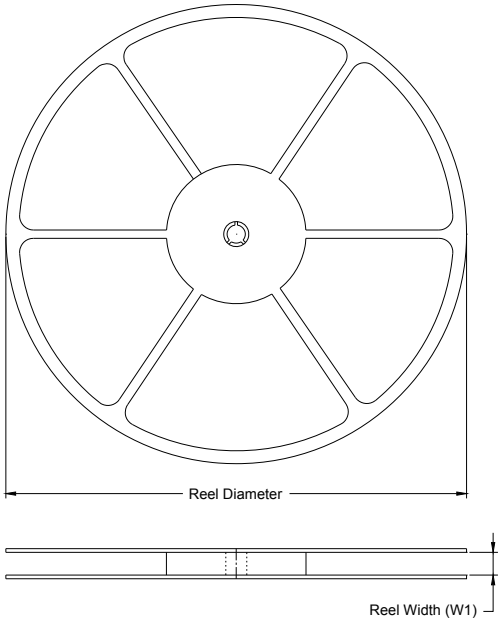


RECOMMENDED LAND PATTERN (Unit: mm)

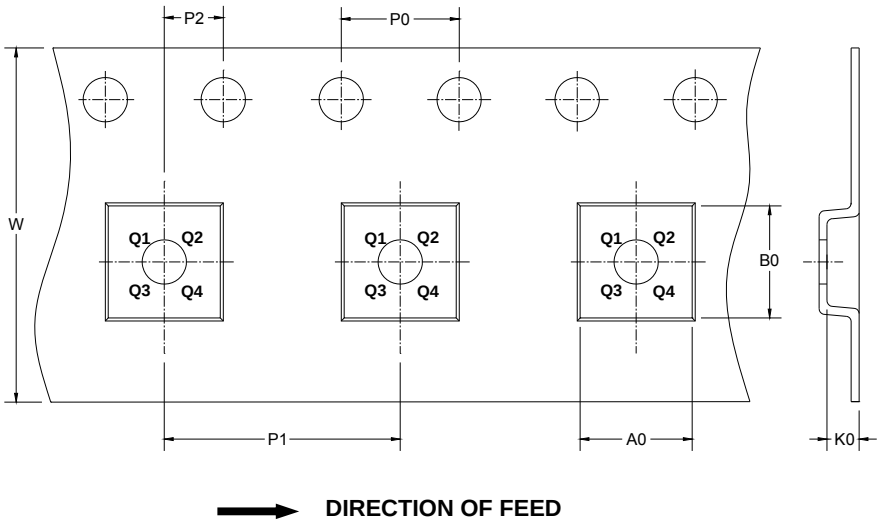
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.200	2.400	0.087	0.094
E1	2.200	2.400	0.087	0.094
k	0.200 MIN		0.008 MIN	
b	0.150	0.250	0.006	0.010
e	0.400 TYP		0.016 TYP	
L	0.324	0.476	0.013	0.019

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

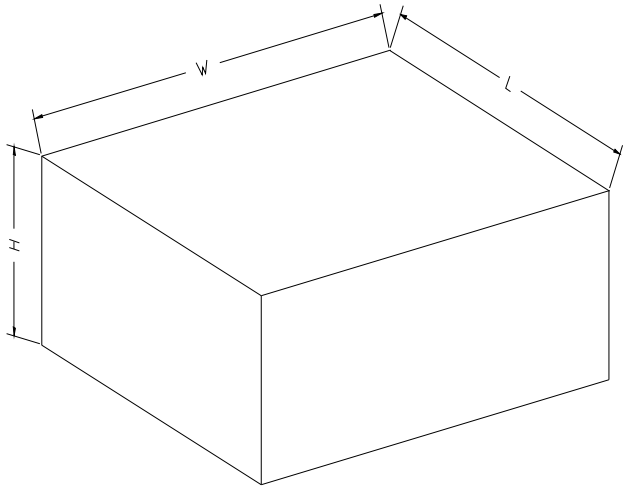


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-28	13″	16.4	6.8	10.25	1.6	4.0	8.0	2.0	16.0	Q1
TQFN-4×4-28L	13″	12.4	4.3	4.3	1.1	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5