2A/1.5MHz, Synchronous Step-Down Converter with Soft Start

DESCRIPTION

The EUP3420 is a synchronous current mode step-down dc-dc converter, capable of delivering 2A load current with excellent line and load regulation. Operating with an input voltage range between 2.7V and 5.5V, the device is ideal for portable applications powered by a single Li-Ion battery cell or by 3-cell NiMH/NiCd batteries. The EUP3420 operates at 1.5MHz fixed frequency PWM mode and provides very low output ripple voltage for noise sensitive applications. The internal integrated synchronous switch increases efficiency while eliminates the need for an external Schottky diode. The EUP3420 is available in the 10-pin MSOP and 10-pin TDFN package.

FEATURES

- High Efficiency up to 96%
- Up to 2A Load Current
- 300μA Typical Quiescent Current
- 1.5MHz Constant Switching Frequency
- 2.7V to 5.5V Input Voltage Range
- Adjustable Output Voltage as Low as 0.7V
- 100% Duty Cycle Low Dropout Operation
- No Schottky Diode Required
- Short Circuit and Thermal Protection
- Excellent Line and Load Transient Response
- ＜1μA Shutdown Current
- Built-In Soft-Start
- Available in MSOP-10 and TDFN-10 Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Cellular and Smart Phones
- Portable Media Players/ MP3 Players
- Digital Still and Video Cameras
- Portable Instruments
- WLAN PC Cards

Typical Application Circuit

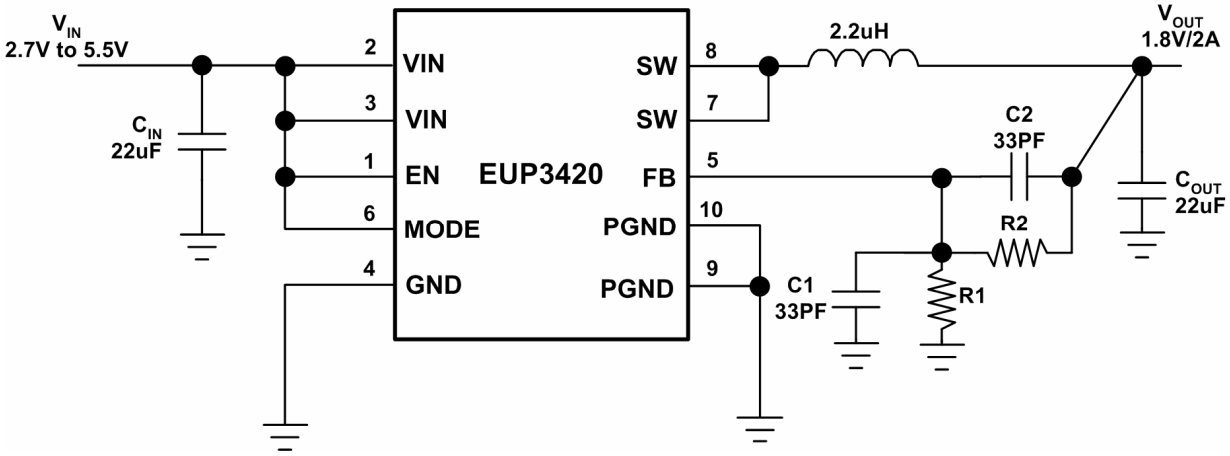
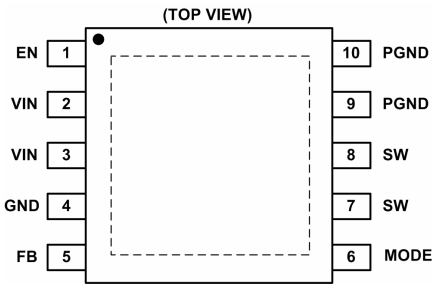
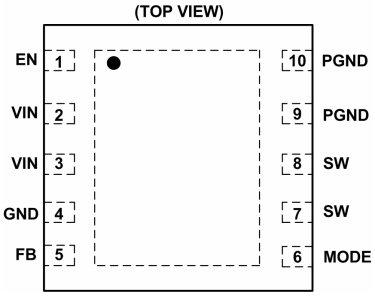


Figure 1.

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
MSOP-10	 Note: The exposed pad must be connected GND.	TDFN-10	 Note: The exposed pad must be connected GND.

Pin Description

Name	MSOP-10	TDFN-10	DESCRIPTION
EN	1	1	Chip enable pin. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. Do not leave EN floating.
VIN	2,3	2,3	Supply voltage input.
GND	4	4	Analog ground.
FB	5	5	Feedback pin.
MODE	6	6	Pulling the MODE pin high allows the device to be forced into fixed frequency operation.
SW	7,8	7,8	Switch node connection to inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
PGND	9,10	9,10	Power ground.

Block Diagram

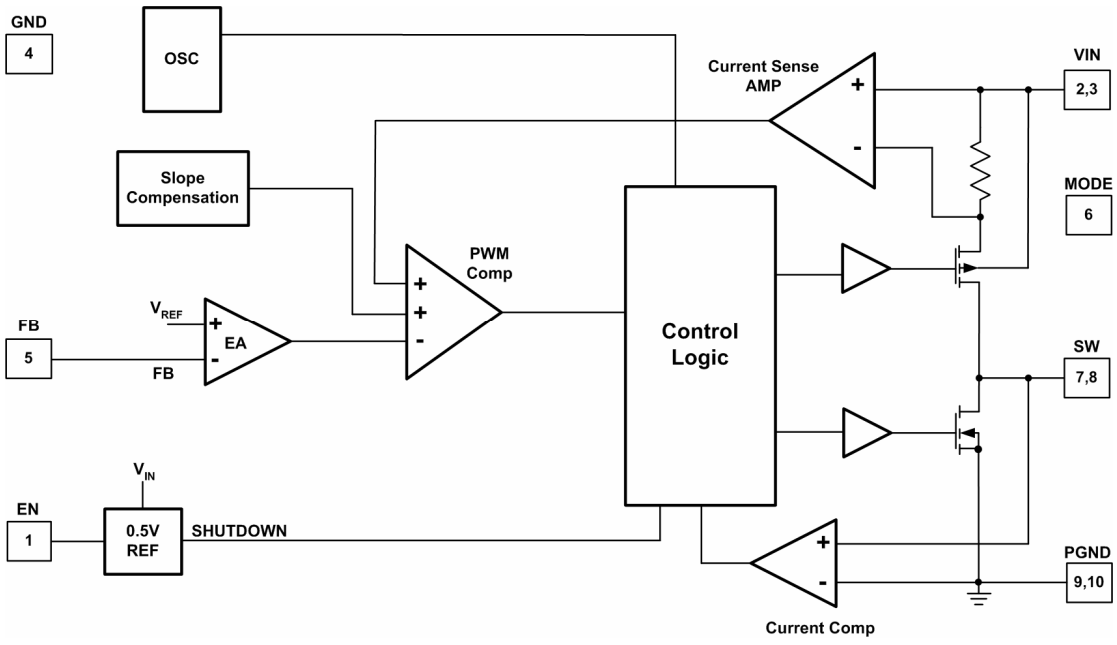


Figure 2.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3420MIR1	MSOP-10	xxxxx P3420	-40 °C to +85°C
EUP3420JIR1	TDFN-10	xxxxx P3420	-40 °C to +85°C

EUP3420 □ □ □ □

Lead Free Code

1: Lead Free, Halogen Free

Packing

R: Tape & Reel

Operating temperature range

I: Industry Standard

Package Type

M: MSOP

J: TDFN

Absolute Maximum Ratings (1)

- Input Supply Voltage ---------- -0.3V to 6V
- EN, FB, MODE Voltages ---------- -0.3V to V_{IN}
- P-Channel Switch Source Current (DC) ---------- 2.2A
- N-Channel Switch Sink Current (DC) ---------- 2.2A
- Peak SW Sink and Source Current ---------- 3A
- Junction Temperature ---------- 125°C
- Storage Temperature ---------- -65°C to 150°C
- Lead Temp (Soldering, 10sec) ---------- 260°C

Recommend Operating Conditions (2)

- Supply Voltage (V_{IN}) ---------- 2.7V to 5.5V
- Operating Temperature Range ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

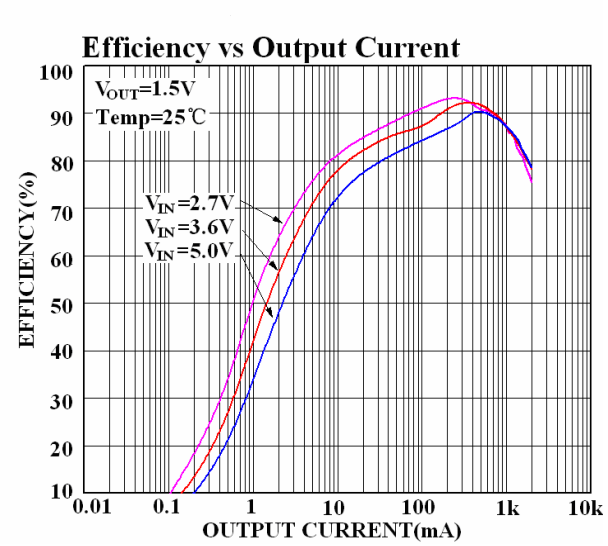
Electrical Characteristics

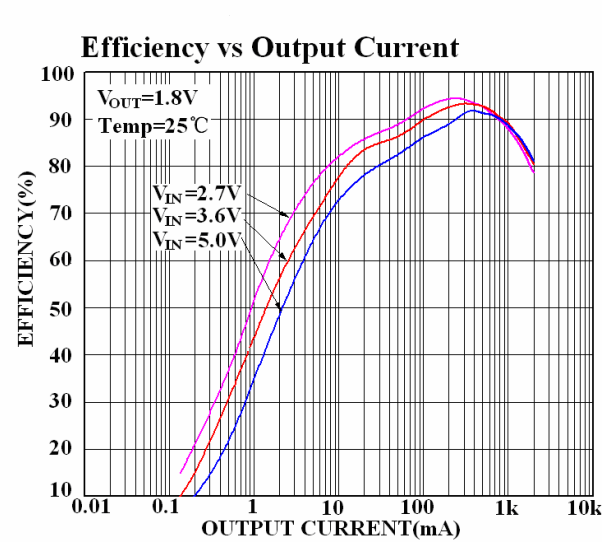
The ● denote the Spec. apply over the full operating temperature range, otherwise Spec. are T_A=+25°C. V_{IN}=3.6V unless otherwise specified.

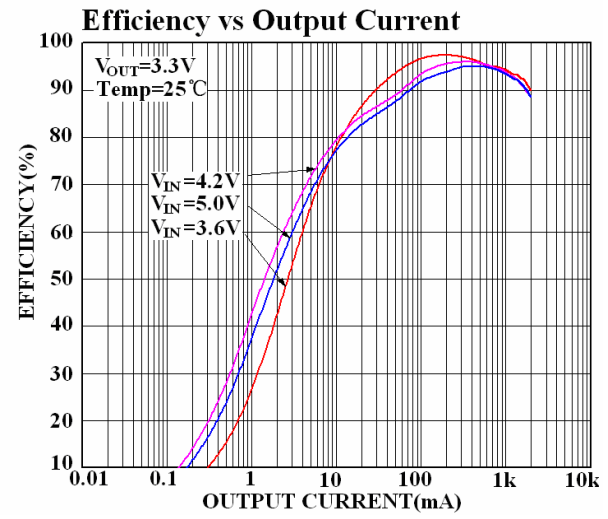
Symbol	Parameter	Conditions		EUP3420			Unit
				Min.	Typ.	Max.	
V_{IN}	Input Voltage Range		●	2.7		5.5	V
UVLO	Input Undervoltage Lockout		●	1.5		2.3	V
I_{FB}	Feedback Current				0		nA
V_{FB}	Regulated Feedback Voltage	T_A=+25°C (Note 3)		0.49	0.5	0.51	V
		-40°C≤ T_A≤+85°C (Note 3)	●	0.485	0.5	0.515	
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN}=2.7V to 5.5V			0.26	0.4	%/V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN}=2.7V to 5.5V			0.26	0.4	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{LOAD}=0mA to 2000mA			0.2		%
I_Q	Quiescent Current	V_{FB}=0.45V, I_{LOAD}=0A	●		300	400	μA
I_{SHDN}	Shutdown Current	V_{EN}=0V			0.1	1	μA
I_{PK}	Peak Inductor Current	V_{IN}=3.6V, V_{FB}=0.45V			2.8		A
f_{OSC}	Oscillator Frequency	V_{FB}=0.45V	●	1.2	1.5	1.8	MHz
		V_{FB}=0V			750		kHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW}=200mA	●		132	210	mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW}=200mA	●		126	210	mΩ
I_{LSW}	SW Leakage Current	V_{EN}=0V, V_{SW}=0 or 5V, V_{IN}=5V		-1		1	μA
V_{EN}	EN Threshold		●	0.3	1.0	1.5	V
I_{EN}	EN Leakage Current					1	μA

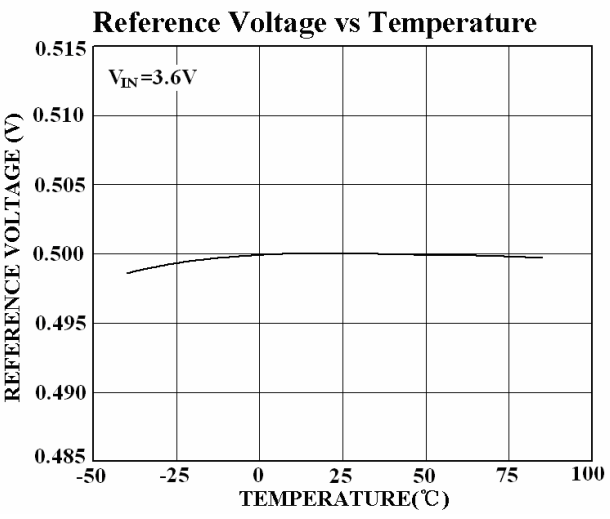
Note (3): The EUP3420 is tested in a proprietary test mode that connects FB to the output of the error amplifier.

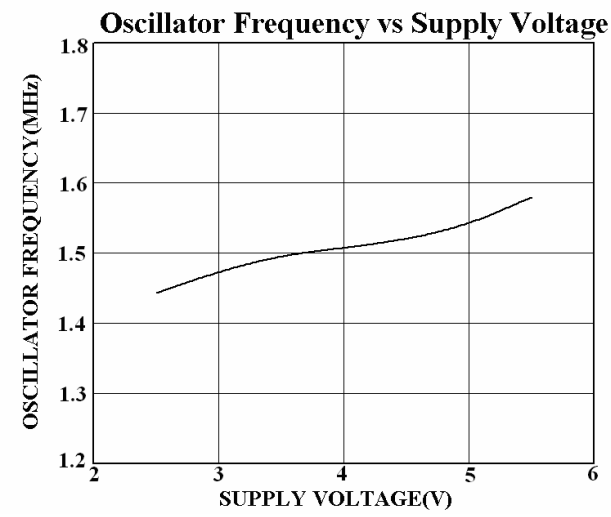
Typical Operating Characteristics

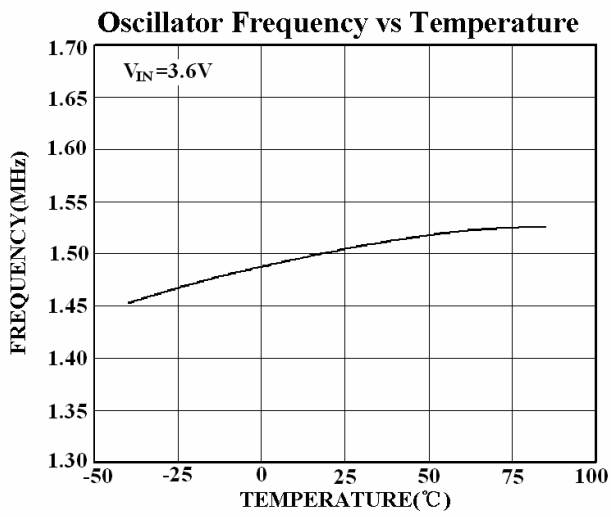




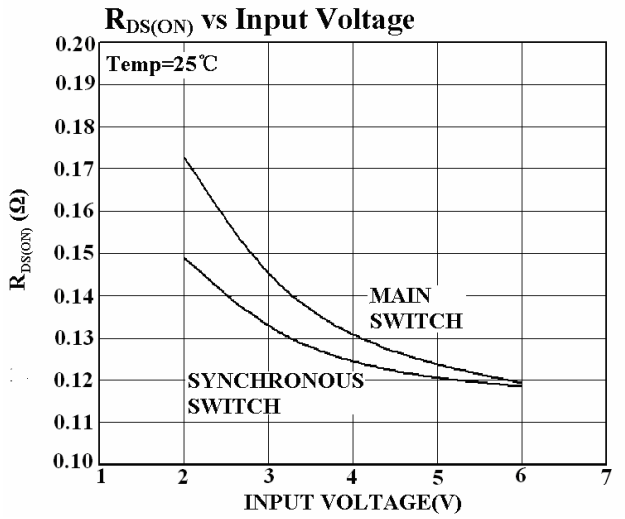


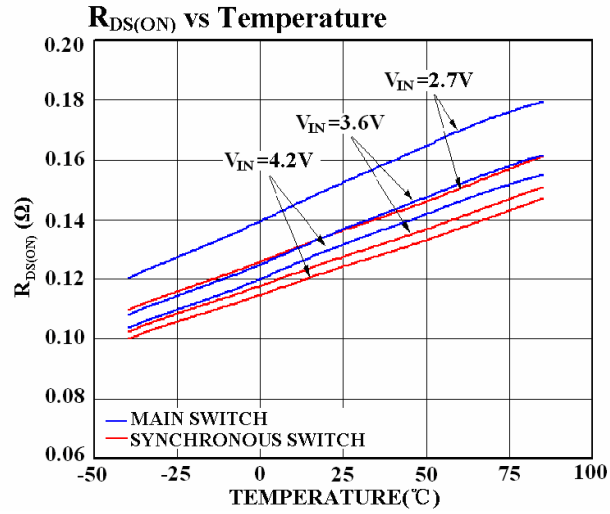


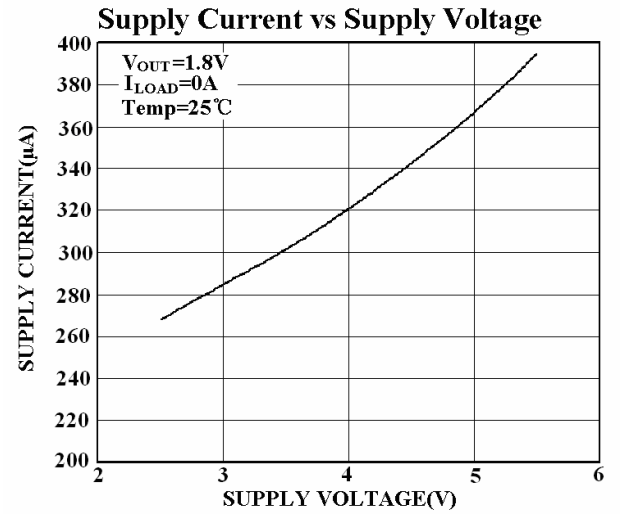


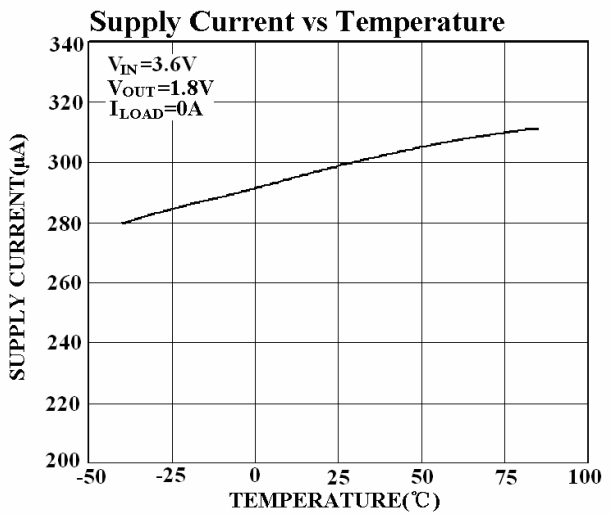


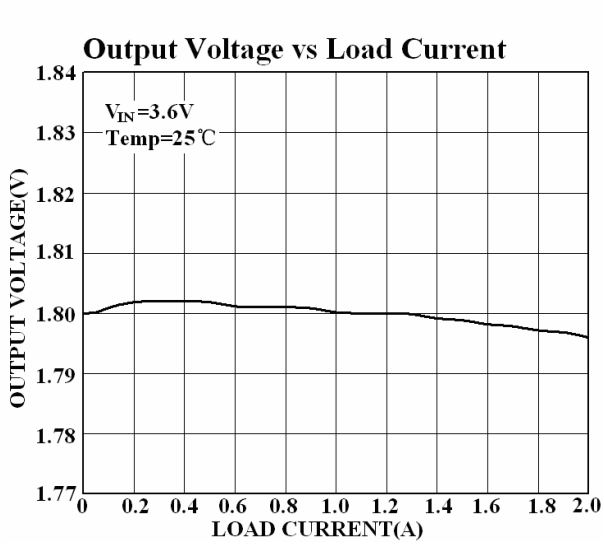
Typical Operating Characteristics (continued)





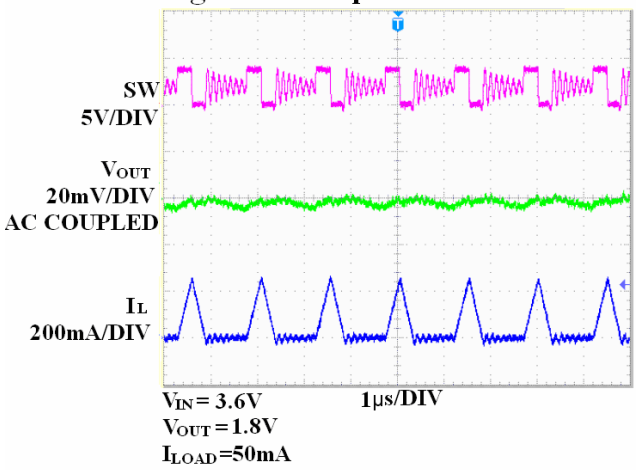




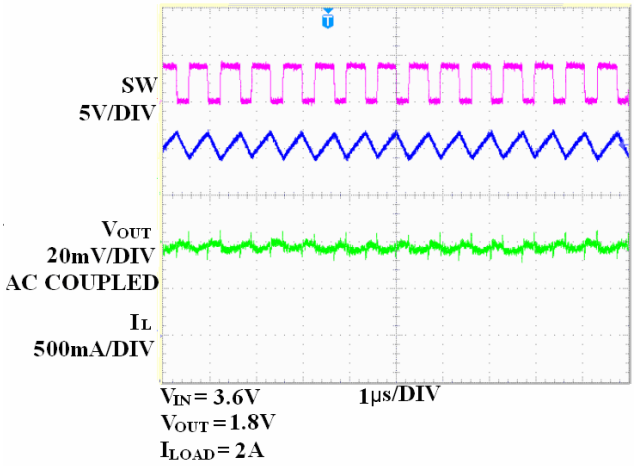


Typical Operating Characteristics (continued)

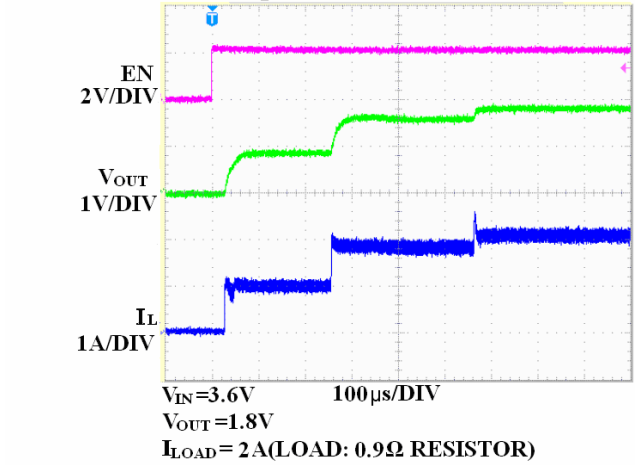
Light Load Operation



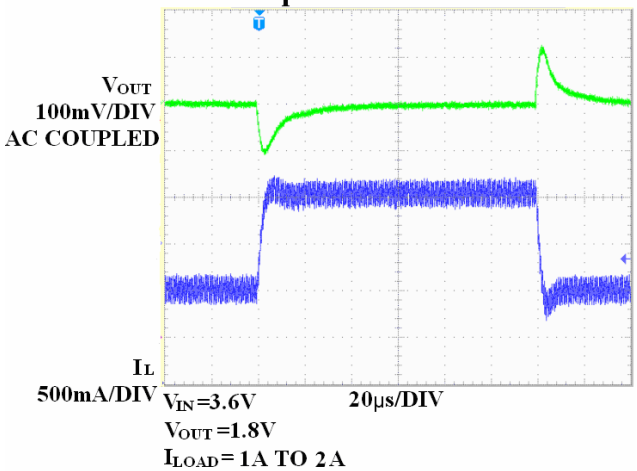
Heavy Load Operation



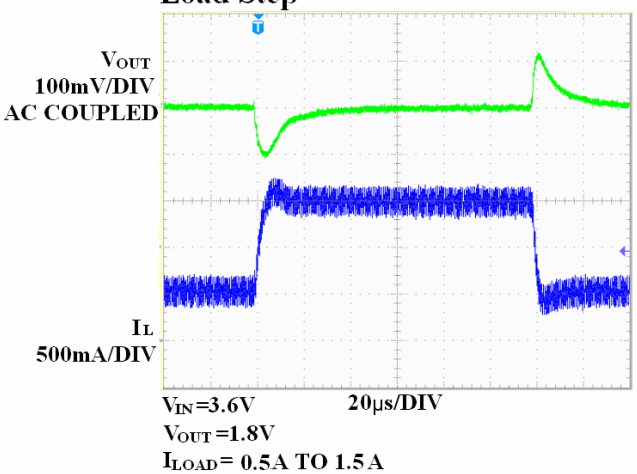
Start-Up from Shutdown



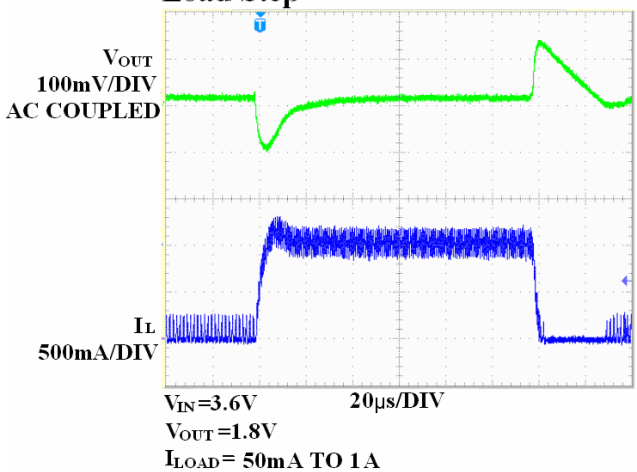
Load Step



Load Step



Load Step



Application Information

The EUP3420 uses a slope-compensated constant frequency, current mode architecture. Both the main (P-Channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the EUP3420 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. The duty cycle is controlled by three weighted differential signals: the output of error amplifier, the main switch sense voltage and the slope-compensation ramp. It modulates output power by adjusting the inductor-peak current during the first half of each cycle. An N-channel, synchronous switch turns on during the second half of each cycle (off time). When the inductor current starts to reverse or when the PWM reaches the end of the oscillator period, the synchronous switch turns off. This keeps excess current from flowing backward through the inductor, from the output capacitor to GND, or through the main and synchronous switch to GND.

Soft-Start

The EUP3420 has an internal soft-start circuit that limits the inrush current and output voltage overshoot during startup. The soft-start is implemented with a digital circuit increasing the switch current in steps.

Short-Circuit Protection

As soon as the output voltage drops below 50% of the nominal output voltage, the converter switching frequency as well as the current limit is reduced to 50% of the nominal value.

Input Undervoltage Lockout

The undervoltage lockout circuit prevents device misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET with undefined conditions.

Inductor Selection

The EUP3420 typically uses a 2.2uH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions.

The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is ΔI_L=800mA (40% of 2A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 2400mA rated inductor should be enough for most applications (2A+400mA).

The DC-resistance of the inductor directely influences the efficiency of the converter. Therefore for better efficiency, choose a low DC-resistance inductor.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3420. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typical value is around 22µF.

The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \times \left(1-\frac{V_O}{V_{IN}}\right)}$$

The output capacitor C_{OUT} has a strong effect on loop stability.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).

ESR is a direct function of the volume of the capacitor; that is, physically larger capacitors have lower ESR. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

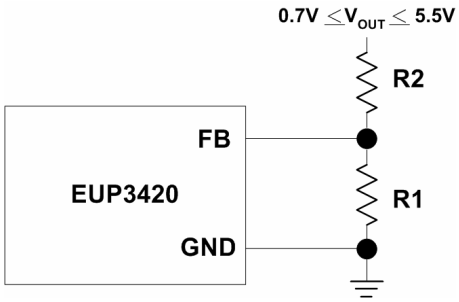
Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.5V\left(1+\frac{R2}{R1}\right)$$

Choose R1 value 50kΩ for most applications.

The external resistive divider is connected to the output, allowing remote voltage sensing as shown below.



Thermal Considerations

To avoid the EUP3420 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R=(P_D)(\theta_{JA})$$

Where $P_D=I_{LOAD}^2 \times R_{DS(ON)}$ is the power dissipated by the regulator ; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J=T_A+T_R$$

Where T_A is the ambient temperature.

T_J should be below the maximum junction temperature of 125°C.

PC Board Layout Checklist

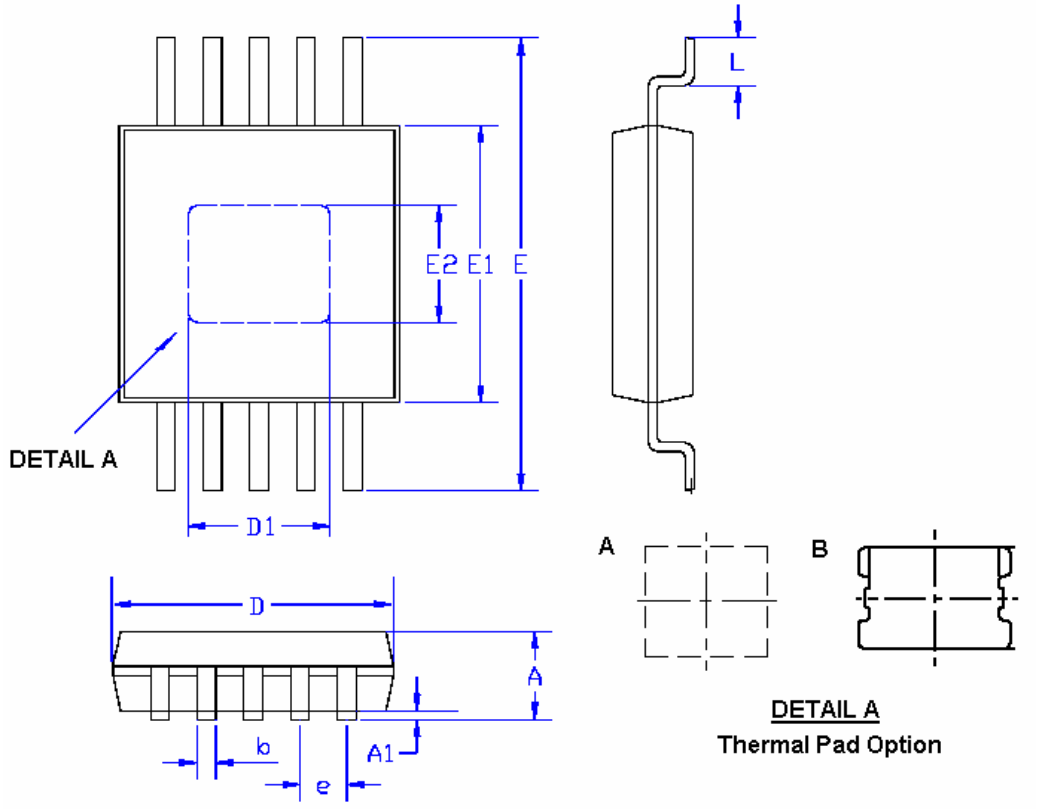
For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3420.

1. The input capacitor C_{IN} should connect to VIN as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
3. The FB pin should connect directly to the feedback resistors. The resistive divider R1/R2 must be connected between the C_{OUT} and ground.
4. Keep the switching node, SW, away from the sensitive FB node.

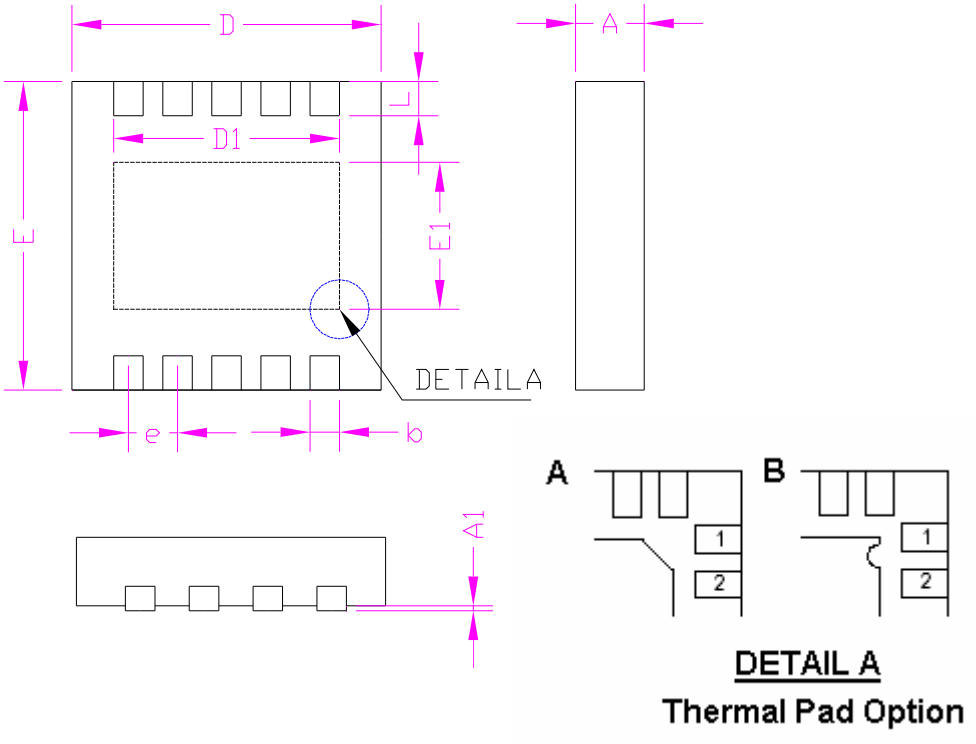
Packaging Information

MSOP-10



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.81	-	1.10	0.032	-	0.043
A1	0.00	-	0.15	0.000	-	0.006
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	1.28	1.80	2.30	0.050	0.071	0.091
E	4.70	4.90	5.10	0.185	0.193	0.201
E1	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.21	1.66	1.73	0.048	0.065	0.068
L	0.40	0.60	0.80	0.016	0.024	0.031
b	0.15	-	0.33	0.006	-	0.013
e	0.50			0.020		

TDFN-10



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.30	2.60	2.65	0.091	0.102	0.104
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.50	1.65	1.75	0.059	0.065	0.069
L	0.30	0.40	0.50	0.012	0.016	0.020
b	0.18	-	0.30	0.007	-	0.012
e	0.50			0.020		