SGM6516
8×16 Analog Crosspoint Switch

GENERAL DESCRIPTION

The SGM6516 is a low power dissipation and high reliability crosspoint switch. The device contains an 8×16 array of crosspoint switches along with a 7 to 128 line decoder and latch circuits. Any one of the 128 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

The SGM6516 is available in Green LQFP-10×10-44L and PLCC-44L packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Internal Control Latches and Address Decoder**
- **Short Set-Up and Hold Times**
- **Wide Operating Voltage: 4.5V to 13.2V**
- **$12V_{PP}$ Analog Signal Capability**
- **R_{ON} = 40Ω (TYP) at V_{DD} = 12V, T_A = +25℃**
- **ΔR_{ON} = 3Ω (TYP) at V_{DD} = 12V, T_A = +25℃**
- **Full CMOS Switch for Low Distortion**
- **Minimum Feedthrough and Crosstalk**
- **Separate Analog and Digital Reference Supplies**
- **Low Power Consumption**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green LQFP-10×10-44L and PLCC-44L Packages**

APPLICATIONS

Key Systems
PBX Systems
Mobile Radio
Test Equipment/Instrumentation
Analog/Digital Multiplexers
Audio/Video Switching

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6516	LQFP-10×10-44L	-40℃ to +85℃	SGM6516YLFB44G/TY	SGM6516 YLFB44 XXXXX	2 Tray (320pcs)
	PLCC-44L	-40℃ to +85℃	SGM6516YPL44G	SGM6516 YPL44 XXXXX	20 Tube (500pcs)

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range

V_{DD} ..... -0.3V to 15V

V_{SS} ..... -0.3V to V_{DD} + 0.3V

Analog Input Voltage (V_{INA}) ..... V_{EE} - 0.3V to V_{DD} + 0.3V

Digital Input Voltage (V_{IN}) ..... V_{SS} - 0.3V to V_{DD} + 0.3V

Current on Any I/O Pin ..... ±15mA

Junction Temperature ..... 150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... 260℃

ESD Susceptibility

HBM 2500V

MM 400V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range

V_{DD} ..... 4.5V to 13.2V

V_{SS} ..... V_{EE} to V_{DD} - 4.5V

Analog Input Voltage (V_{INA}) ..... V_{EE} to V_{DD}

Digital Input Voltage (V_{IN}) ..... V_{EE} to V_{DD}

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

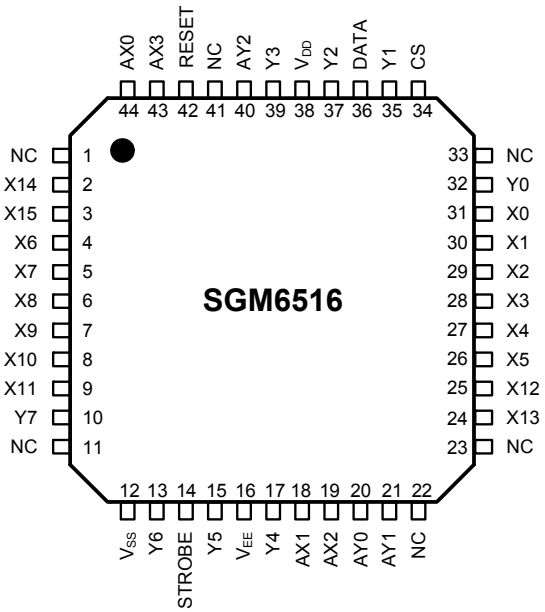
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

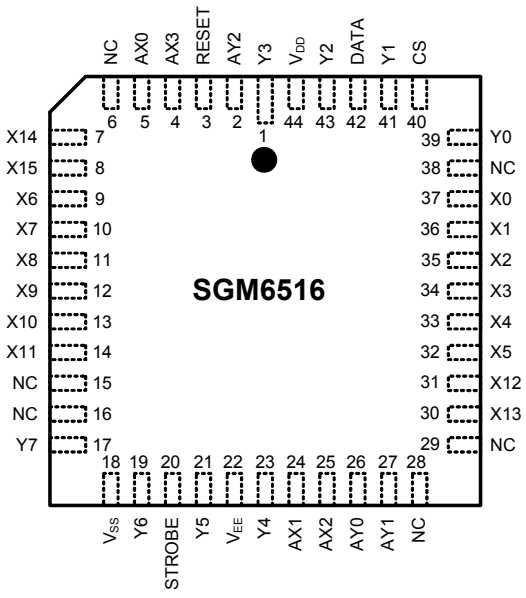
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATIONS (TOP VIEW)



LQFP-10×10-44L



PLCC-44L

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
LQFP-10×10-44L	PLCC-44L			
1, 11, 41	6, 15, 16	NC	–	No Connection.
2, 3	7, 8	X14, X15	I/O	X14 and X15 Analog Pins. These are connected to the X14 and X15 rows of the switch array.
4 - 9	9 - 14	X6 - X11	I/O	X6 - X11 Analog Pins. These are connected to the X6 - X11 rows of the switch array.
10	17	Y7	I/O	Y7 Analog Pin. This is connected to the Y7 column of the switch array.
12	18	V_{SS}	–	Digital Ground Reference.
13	19	Y6	I/O	Y6 Analog Pin. This is connected to the Y6 column of the switch array.
14	20	STROBE	I	STROBE Pin. Enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active high.
15	21	Y5	I/O	Y5 Analog Pin. This is connected to the Y5 column of the switch array.
16	22	V_{EE}	–	Negative Power Supply.
17	23	Y4	I/O	Y4 Analog Pin. This is connected to the Y4 column of the switch array.
18, 19	24, 25	AX1, AX2	I	X1 and X2 Address Line Pins.
20, 21	26, 27	AY0, AY1	I	Y0 and Y1 Address Line Pins.
22, 23, 33	28, 29, 38	NC	–	No Connection.
24, 25	30, 31	X13, X12	I/O	X13 and X12 Analog Pins. These are connected to the X13 and X12 rows of the switch array.
26 - 31	32 - 37	X5 - X0	I/O	X5 - X0 Analog Pins. These are connected to the X5 - X0 rows of the switch array.
32	39	Y0	I/O	Y0 Analog Pin. This is connected to the Y0 column of the switch array.
34	40	CS	I	Chip Select Pin. This is used to select the device. Active high.
35	41	Y1	I/O	Y1 Analog Pin. This is connected to the Y1 column of the switch array.
36	42	DATA	I	DATA Pin. A logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active high.
37	43	Y2	I/O	Y2 Analog Pin. This is connected to the Y2 column of the switch array.
38	44	V_{DD}	–	Positive Power Supply.
39	1	Y3	I/O	Y3 Analog Pin. This is connected to the Y3 column of the switch array.
40	2	AY2	I	Y2 Address Line Pin.
42	3	RESET	I	Master RESET Pin. This is used to turn off all switches regardless of the condition of CS. Active high.
43, 44	4, 5	AX3, AX0	I	X3 and X0 Address Line Pins.

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
DC Electrical Characteristics (Voltages are referenced to V_{EE} = 0V, V_{DD} = 12V, Full = -40℃ to +85℃, typical values are at +25℃, unless otherwise noted.)								
Quiescent Supply Current	I_{DD}	All digital inputs at V_{IN} = V_{SS} or V_{DD}		Full		120	240	μA
		All digital inputs at V_{IN} = 2.4V + V_{SS}, V_{SS} = 7.0V		Full		250	2500	μA
		All digital inputs at V_{IN} = 3.4V		Full		120	280	μA
Off-State Leakage Current	I_{OFF}	I V_{Xi} - V_{Yj} I = V_{DD} - V_{EE}, Test Circuit 1		Full		0.01	2	μA
Input Logic "0" Level	V_{IL}	V_{SS} = 7.5V, V_{EE} = 0V		Full			0.5 + V_{SS}	V
Input Logic "1" Level	V_{IH}	V_{EE} = 0V	V_{SS} = 6.5V	Full	2.2 + V_{SS}			V
			V_{SS} = 0V	Full	2.3			
Input Leakage (Digital Pins)	I_{LEAK}	All digital inputs at V_{IN} = V_{SS} or V_{DD}		Full		2.5	8.5	μA
DC Electrical Characteristics - Switch Resistance (V_{DC} is the external DC offset voltage applied at the analog I/O pins. Full = -40℃ to +85℃, typical values are at +25℃, unless otherwise noted.)								
On-State Resistance	V_{DD} = 12V	R_{ON}	V_{SS} = V_{EE} = 0V, V_{DC} = V_{DD}/2, I V_{Xi} - V_{Yj} I = 0.4V, Test Circuit 2	+25℃		40	65	Ω
				Full			85	
	V_{DD} = 10V			+25℃		45	70	
				Full			95	
	V_{DD} = 5V			+25℃		115	175	
				Full			195	
Difference in On-State Resistance between Two Switches		ΔR_{ON}	V_{DD} = 12V, V_{SS} = V_{EE} = 0V, V_{DC} = V_{DD}/2, I V_{Xi} - V_{Yj} I = 0.4V, Test Circuit 2	+25℃		3	12.5	Ω
				Full			15	
AC Electrical Characteristics - Crosspoint Performance (Voltages are referenced to V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V, typical values are at +25℃, unless otherwise noted.)								
Switch I/O Capacitance		C_S	f = 1MHz	+25℃		65		pF
Feedthrough Capacitance		C_F	f = 1MHz	+25℃		25		pF
-3dB Bandwidth		BW	Switch is "ON", V_{INA} = $2V_{PP}$ sine wave, R_L = 1kΩ, Test Circuit 3	+25℃		45		MHz
Total Harmonic Distortion		THD	Switch is "ON", V_{INA} = $2V_{PP}$ sine wave, R_L = 1kΩ, f = 1kHz	+25℃		0.11		%
Feedthrough Channel "OFF" (FDT = 20LOG(V_{OUT}/V_{Xi}))		FDT	All Switches "OFF", V_{INA} = $2V_{PP}$ sine wave, R_L = 1kΩ, f = 1kHz, Test Circuit 4	+25℃		-101		dB
Crosstalk between Any Two Channels for Switches Xi - Yi and Xj - Yj. (X_{TALK} = 20LOG(V_{OUT}/V_{Xi}))		X_{TALK}	V_{INA} = $2V_{PP}$ sine wave, Test Circuit 5	R_L = 600Ω, f = 1kHz	+25℃		-101		dB
				R_L = 600Ω, f = 10kHz	+25℃		-82		dB
				R_L = 600Ω, f = 20kHz	+25℃		-77		dB
				R_L = 75Ω, f = 6MHz	+25℃		-51		dB
				R_L = 75Ω, f = 10MHz	+25℃		-47		dB
				R_L = 1kΩ, f = 10kHz	+25℃		-81		dB
				R_L = 10kΩ, f = 1kHz	+25℃		-79		dB
Propagation Delay through Switch		t_{PS}	R_L = 1kΩ, C_L = 50pF	+25℃		5		ns

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
AC Electrical Characteristics - Control and I/O Timings (Voltages are referenced to V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V, typical figures are at +25℃, unless otherwise noted.)							
Control Input Crosstalk to Switch (for CS, DATA, STROBE, ADDRESS)	CX_{TALK}	V_{IN} = 3V square wave, R_{IN} = 1kΩ, R_L = 1kΩ, C_L = 50pF, Test Circuit 6	+25℃		840		mV_{PP}
Digital Input Capacitance	C_{DI}	f = 1MHz	+25℃		12		pF
Switching Frequency	f_O		+25℃		5		MHz
STROBE to Switch Status Delay	t_S	R_L = 1kΩ, C_L = 50pF, Test Circuit 7	+25℃		30		ns
DATA to Switch Status Delay	t_D	R_L = 1kΩ, C_L = 50pF, Test Circuit 7	+25℃		32		ns
RESET to Switch Status Delay	t_R	R_L = 1kΩ, C_L = 50pF, Test Circuit 7	+25℃		33		ns
Setup Time DATA to STROBE	t_{DS}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns
Hold Time DATA to STROBE	t_{DH}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns
Setup Time Address to STROBE	t_{AS}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns
Hold Time Address to STROBE	t_{AH}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns
Setup Time CS to STROBE	t_{CSS}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns
Hold Time CS to STROBE	t_{CSH}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns
STROBE Pulse Width	t_{SPW}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns
RESET Pulse Width	t_{RPW}	R_L = 1kΩ, C_L = 50pF	+25℃		100		ns

TIMING DIAGRAM

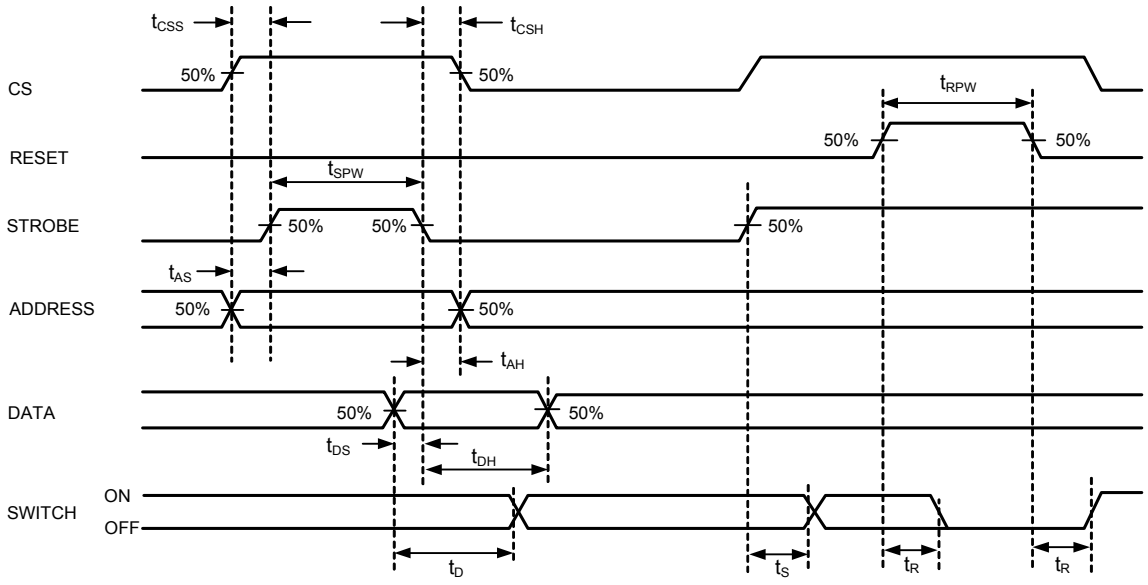
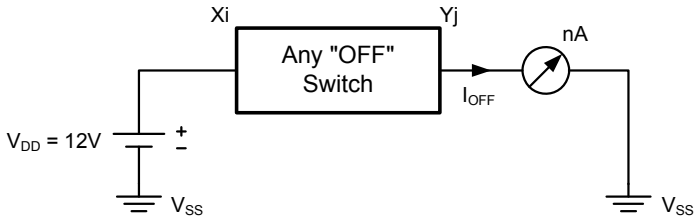


Figure 1. Control Memory Timing Diagram

Table 1. Address Decode Truth Table

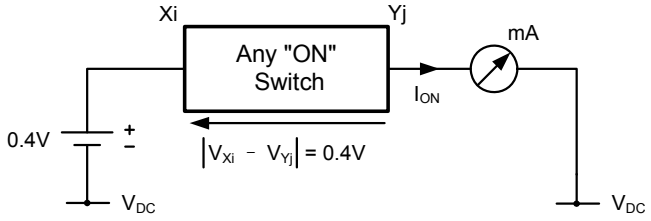
AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	X12-Y0
1	1	1	0	0	0	0	X13-Y0
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	X14-Y0
1	1	1	1	0	0	0	X15-Y0
0	0	0	0	1	0	0	X0-Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	0	X15-Y1
0	0	0	0	0	1	0	X0-Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	0	X15-Y2
0	0	0	0	1	1	0	X0-Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	0	X15-Y3
0	0	0	0	0	0	1	X0-Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	0	1	X15-Y4
0	0	0	0	1	0	1	X0-Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	1	X15-Y5
0	0	0	0	0	1	1	X0-Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	1	X15-Y6
0	0	0	0	1	1	1	X0-Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	1	X15-Y7

TEST CIRCUITS



V_{DD} = 12V, V_{EE} = V_{SS} = 0V.
i can be equal to j.
All other switches are "OFF".
I_{OFF} is also measured on the V_{DD} side.

Test Circuit 1. Off-State Leakage Current (I_{OFF}) Measurement

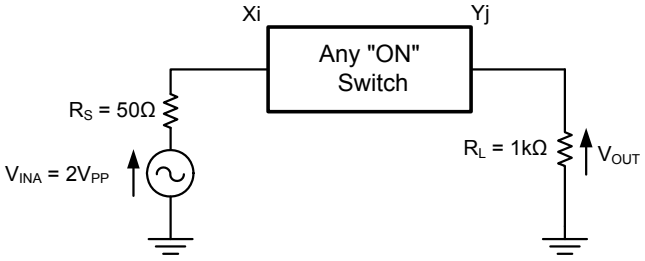


V_{DD} = 12V, V_{EE} = V_{SS} = 0V.
V_{DC} = V_{DD}/2 = voltage centered at the middle of the switch and is w.r.t. V_{EE}.

$$R_{ON} = \frac{|V_{Xi} - V_{Yj}|}{I_{ON}} = \frac{0.4V}{I_{ON}}$$

i can be equal to j.

Test Circuit 2. $R_{ON}/\Delta R_{ON}$ Measurement

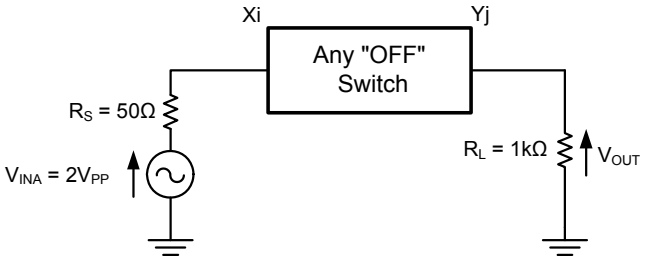


V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V.

$$-3dB = 20LOG\left|\frac{V_{OUT}}{V_{Xi}}\right|$$

i can be equal to j.

Test Circuit 3. Frequency Response (BW) Measurement



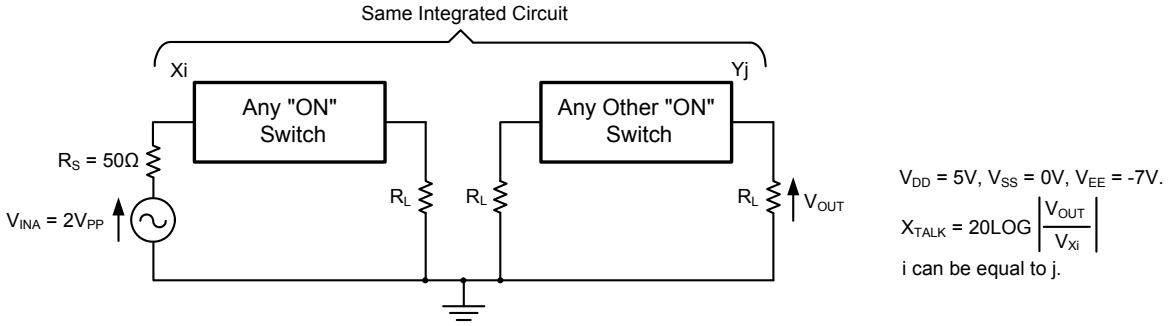
V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V.

$$FDT = 20LOG\left|\frac{V_{OUT}}{V_{Xi}}\right|$$

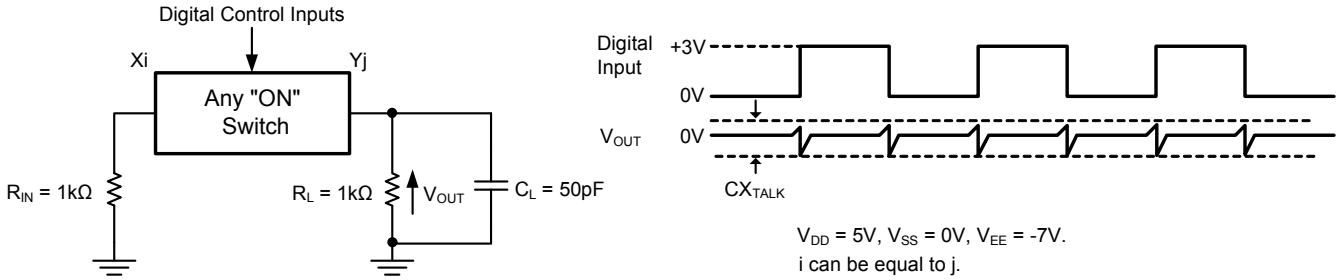
All other switches are "OFF" .
i can be equal to j.

Test Circuit 4. Feedthrough (FDT) Measurement

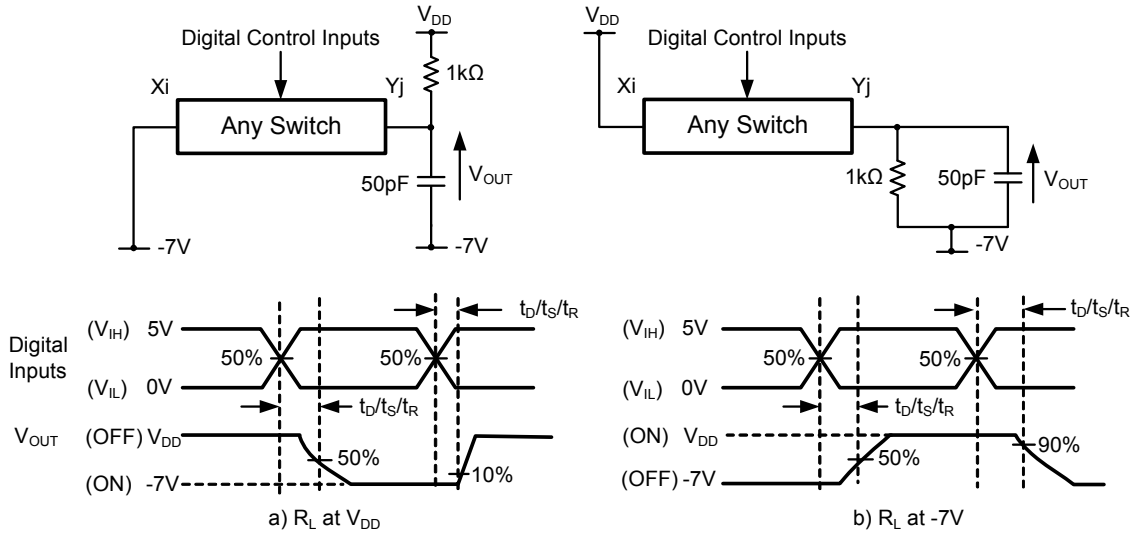
TEST CIRCUITS



Test Circuit 5. Crosstalk (X_{TALK}) Measurement



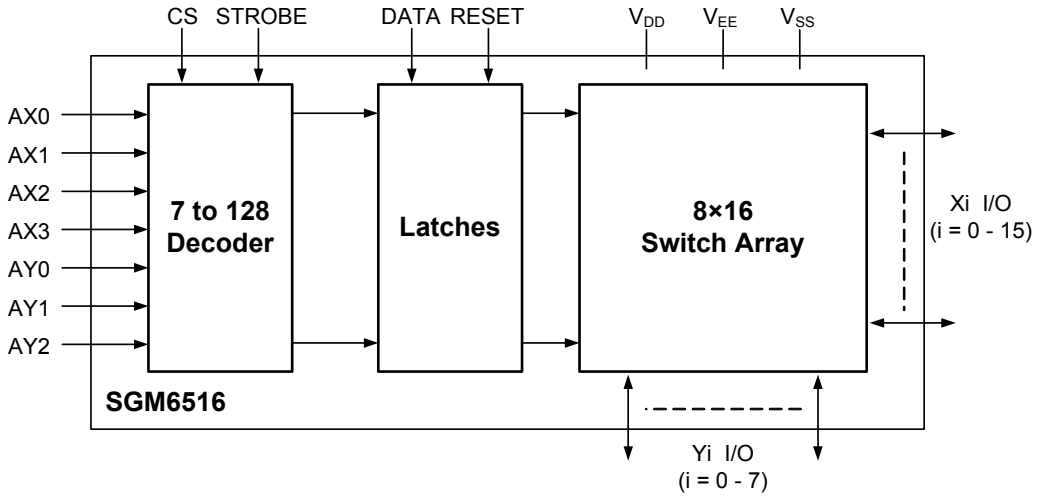
Test Circuit 6. Control Input Crosstalk to Switch (CX_{TALK})



Test Circuit 7. Control Memory Timing Measurements

NOTE:
All Xi and Yj analog I/O pins can be interchanged for all measurements.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Functional Description

The SGM6516 is an analog switch matrix with an array size of 8×16. The switch array is arranged such that there are 8 columns by 16 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 128 bit write-only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint switch off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the SGM6516 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

APPLICATION INFORMATION

Figure 2 shows a typical application circuit of a video surveillance system using analog crosspoint switches which allow multiple video sources to be switched to multiple output devices, e.g., video monitor, video recorder, etc.

Figure 3 illustrates the major components of a video surveillance system. In the center is the SGM6516, an 8×16 analog crosspoint IC. On the left are 16 video input buffers, such as SGM9119, SGM9124, SGM9125, SGM9126, etc. On the right hand side are 8 video output buffers (SGM9124) and each buffer is capable of driving a 75Ω video load directly. BNC connectors are provided for all video inputs and video outputs.

An FT245R USB FIFO from Future Technology Devices International (FTDI) provides a standard USB interface for a PC. Through this USB connection the PC controls the switching of the video signals.

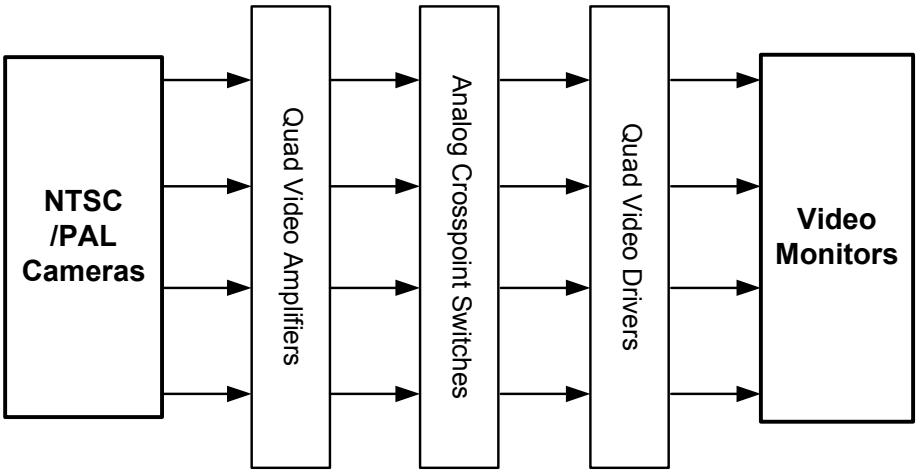


Figure 2. Typical Video Surveillance System

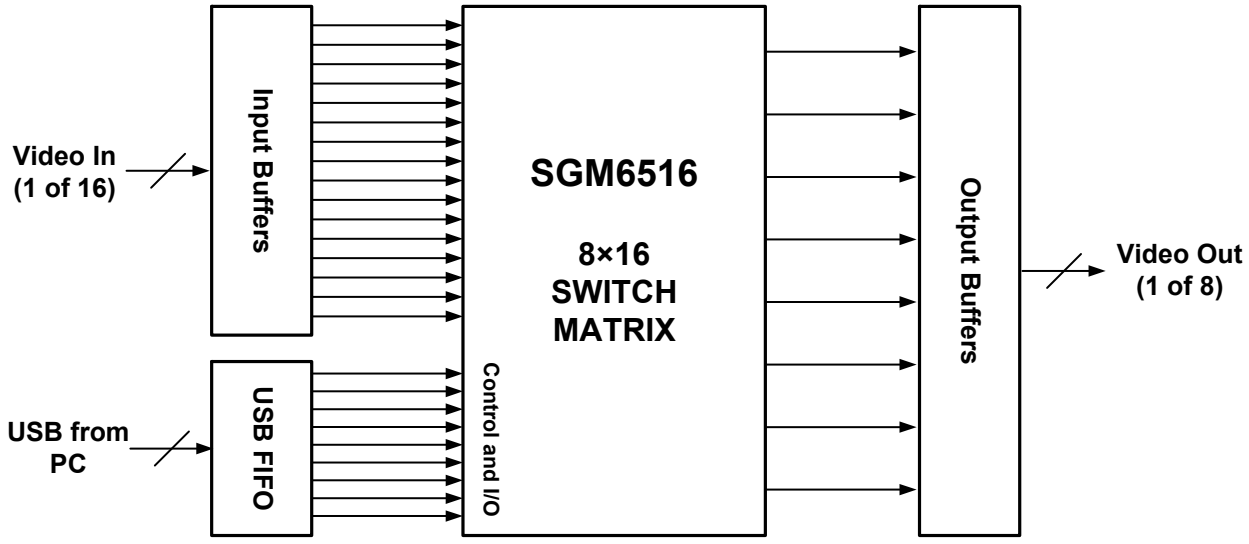
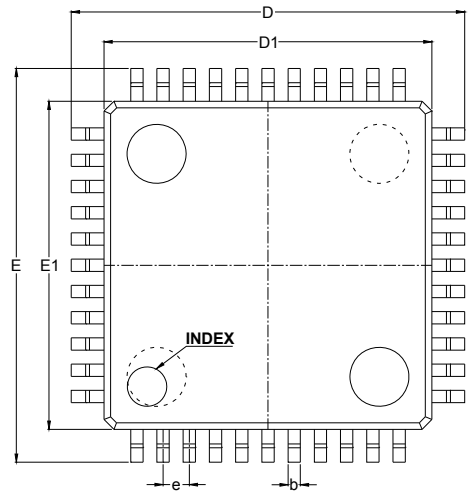


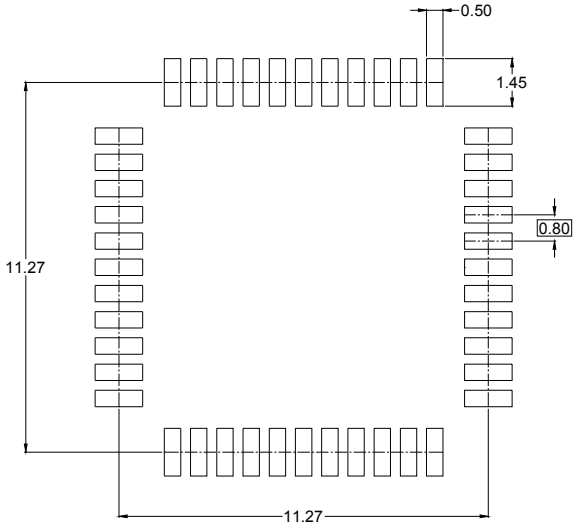
Figure 3. Functional Block Diagram for an 8×16 Video Surveillance System Using SGM6516

PACKAGE OUTLINE DIMENSIONS

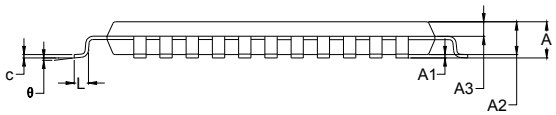
LQFP-10×10-44L



TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

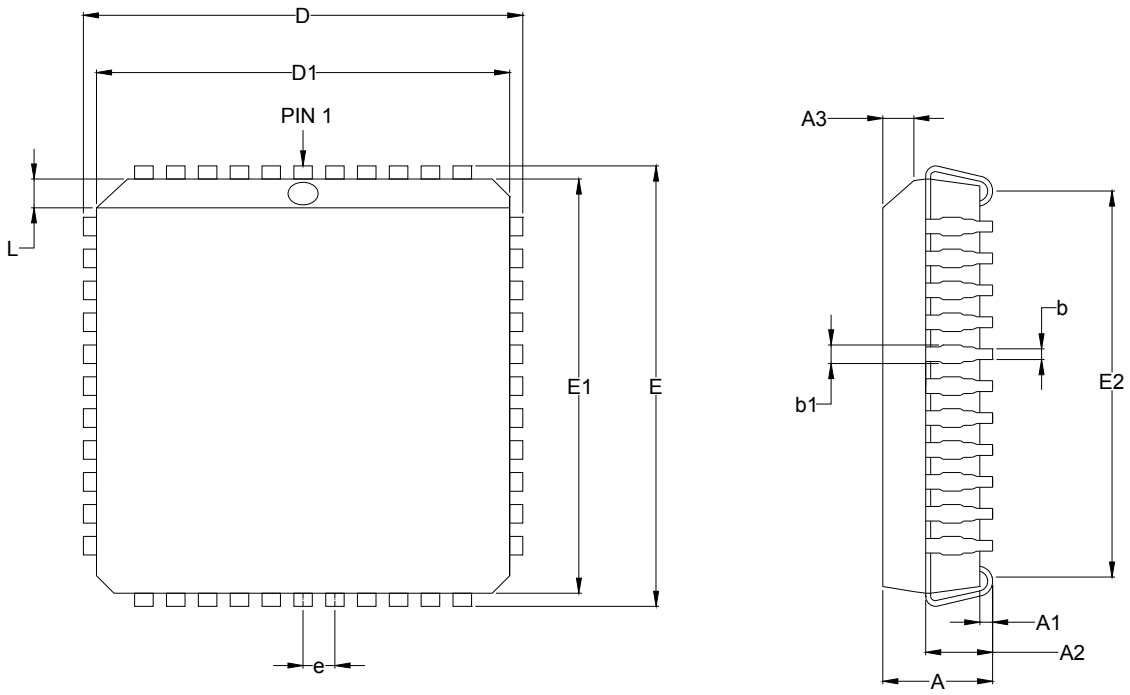


SIDE VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.31		0.44
c	0.13		0.18
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80 BSC		
L	0.45	0.60	0.75
θ	0°	3.5°	7°

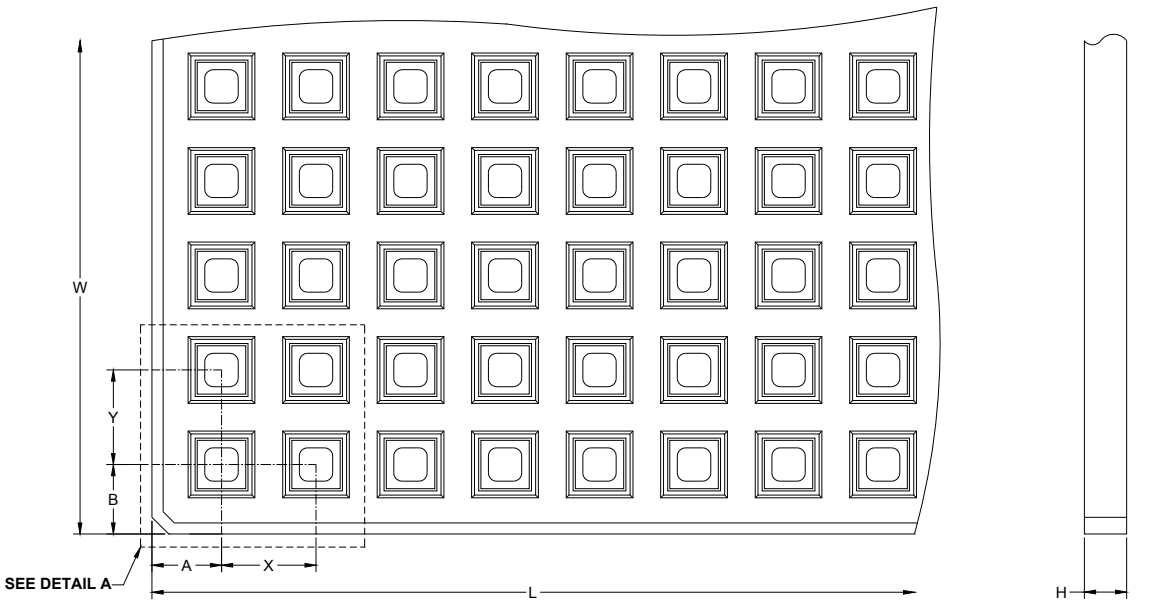
PACKAGE OUTLINE DIMENSIONS

PLCC-44L



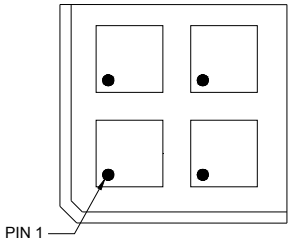
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	4.19	4.57	0.165	0.180
A1	0.51 MIN		0.020 MIN	
A2	2.29	3.05	0.090	0.120
A3	1.07	1.42	0.042	0.056
b	0.33	0.53	0.013	0.021
b1	0.66	0.81	0.026	0.032
D	17.40	17.65	0.685	0.695
D1	16.41	16.56	0.646	0.652
E	17.40	17.65	0.685	0.695
E1	16.41	16.56	0.646	0.652
E2	14.99	16.00	0.590	0.630
e	1.27 TYP		0.050 TYP	
L	1.07	1.22	0.042	0.048

TRAY INFORMATION



TOP VIEW

SIDE VIEW



DETAIL A

Pin 1 is closest to the chamfered corner of the tray.

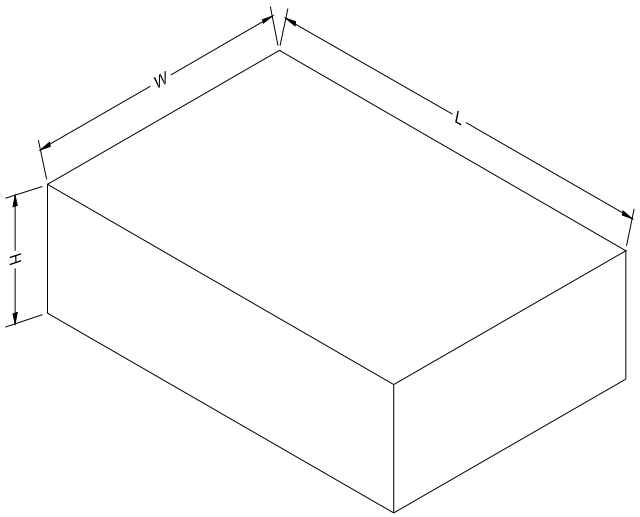
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TRAY

Package Type	A (mm)	B (mm)	X (mm)	Y (mm)	L (mm)	W (mm)	H (mm)	Devices/Tray
LQFP-10×10-44L	13.10	13.00	15.20	15.70	322.6	135.9	7.6	160

DD0003

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Packing Type	Length (mm)	Width (mm)	Height (mm)	Tray/Inner Box	Inner Box/Carton
Tray	560	375	180	2	6

DD0004