SGM4558
Dual SIM/Smart Card Power Supply and Interface

GENERAL DESCRIPTION

The SGM4558 provides the power conversion and signal level translation needed for advanced cellular telephones to interface with 1.8V or 3V subscriber identity modules (SIMs). The device meets all requirements for 1.8V and 3V SIMs and contains two LDO regulators to power 1.8V or 3V SIM cards from a 2.7V to 5.5V input. The output voltages can be set using the two voltage selection pins and up to 250mA of load current can be supplied. A channel select pin determines which channel is open for communication. Separate enable pins for each channel allow both cards to be powered at once and allow for faster transition from one channel to the other.

Internal level translators allow controllers operating with supplies as low as 1.4V to interface with 1.8V or 3V smart cards. Battery life is maximized by a low operating current of 90μA and a shutdown current of less than 2μA when battery voltage is less than 3.3V.

The SGM4558 is available in the Green TQFN-3×3-20L package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Power Management and Control for Two SIM Cards or Smart Cards**
- **Independent 1.8V/3V V_{CC} Control for Both Cards**
- **Two LDOs Support up to 250mA Loading**
- **Supports Simultaneous Powering of Both Cards**
- **Fast Channel Switching**
- **Automatic Level Translation**
- **Fast Signal Rise Times**
- **Built-In Fault Protection Circuitry**
- **Automatic Activation/Deactivation Sequencing Circuitry**
- **Low Operating and Shutdown Current**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green TQFN-3×3-20L Package**

APPLICATIONS

GSM, TD-SCDMA and Other $3G^{+}$ Cellular Phones
Wireless Point-of-Sale Terminals
Multiple SIM Card Interfaces

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM4558	TQFN-3×3-20L	-40℃ to +85℃	SGM4558YTQG20G/TR	SGM 4558QG XXXXX	Tape and Reel, 3000

NOTE: **XXXXX** = Date Code and Vendor Code.

ABSOLUTE MAXIMUM RATINGS

V_{BAT}, DV_{CC}, RSTIN, CLKIN, CLKRUNA, CLKRUNB, ENABLEA, ENABLEB, CSEL, VSELA, VSELB to GND
.....-0.3V to 6V
V_{CCA}, V_{CCB} to GND.....-0.3V to V_{BAT} + 0.3V
DATA to GND.....-0.3V to D_{VCC} + 0.3V
I/OA, CLKA, RSTA to GND..... -0.3V to V_{CCA} + 0.3V
I/OB, CLKB, RSTB to GND..... -0.3V to V_{CCB} + 0.3V
$V_{CCA,B}$ Short-Circuit Duration..... Infinite
Package Thermal Resistance
TQFN-3×3-20L, θ_{JA}.....95℃/W
Operating Temperature Range..... -40℃ to +85℃
Junction Temperature..... 150℃
Storage Temperature Range.....-65℃ to +150℃
Lead Temperature (soldering, 10sec)..... 260℃
ESD Susceptibility
HBM.....4000V
MM.....300V

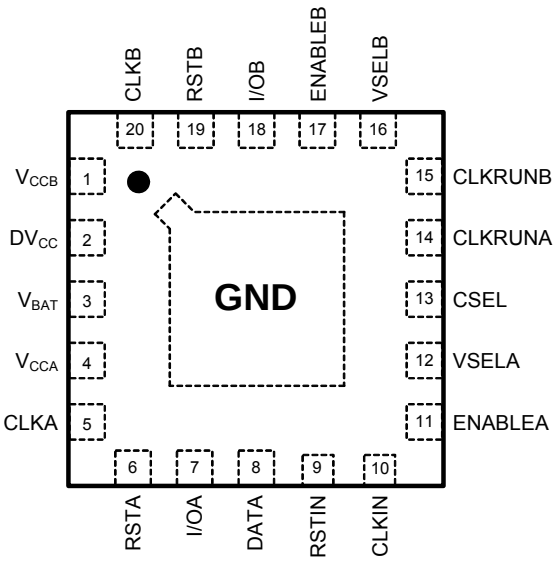
NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATION (TOP VIEW)



TQFN-3×3-20L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 4	V_{CCB}, V_{CCA}	Card Socket. The V_{CCA}, V_{CCB} pins should be connected to the V_{CC} pins of the respective card sockets. The activation of the V_{CCA}, V_{CCB} pins is controlled by ENABLEA and ENABLEB. They can be set to 1.8V or 3V via the VSELA and VSELB inputs.
2	DV_{CC}	Power. Reference voltage for the control logic.
3	V_{BAT}	Power. Supply voltage for the analog sections of the SGM4558.
5, 20	CLKA, CKLB	Card Socket. The CLKA, CKLB pins should be connected to the CLK pins of the respective card sockets. The CLKA, CKLB signals are derived from the CLKIN pin. They provide a level shifted CLKIN signal to the selected card. The CLKA, CKLB pins are gated off until V_{CCA}, V_{CCB} attain their correct values. When a card socket is deselected, its CLK pin may be left active or brought LOW using the CLKRUNA, CLKRUNB pins.
6, 19	RSTA, RSTB	Card Socket. The RSTA, RSTB pins should be connected to the RST pins of the respective card sockets. The RSTA, RSTB signals are derived from the RSTIN pin. When a card is selected, its RST pin follows RSTIN. The RSTA, RSTB pins are gated off until V_{CCA}, V_{CCB} attain their correct values. When a card socket is deselected, the state of its RST pin is latched to its current state.
7, 18	I/OA, I/OB	Card Socket. The I/OA, I/OB pins should be connected to the I/O pins of the respective card sockets. When a card is selected, its I/O pin transmits/receives data to/from the DATA pin. The I/OA, I/OB pins are gated off until V_{CCA}, V_{CCB} attain their correct values.
8	DATA	Input/Output. Microcontroller side data I/O pin. The DATA pin provides the bidirectional communication path to both cards. One of the cards may be selected to communicate via the DATA pin at a time. The pin possesses a weak pull-up current source, allowing the controller to use an open drain output and maintain a HIGH state during shutdown, as long as DV_{CC} is powered.

PIN DESCRIPTION

PIN	NAME	FUNCTION
9	RSTIN	Input. The RSTIN pin supplies the reset signal to the cards. It is level shifted and transmitted directly to the RST pin of the selected card.
10	CLKIN	Input. The CLKIN pin supplies the clock signal to the cards. It is level shifted and transmitted directly to the CLK pin of the selected card. If CLKRUNA,B is HIGH, the clock signal will be transmitted to the CLKA,B pin, regardless of whether that card is selected, as long as that card socket is enabled.
11, 17	ENABLEA, ENABLEB	Inputs. The ENABLEA and ENABLEB pins enable or disable channel A and channel B, respectively.
12, 16	VSELA, VSELB	Inputs. The VSELA and VSELB pins select the voltage level of each set of SIM/Smart Card pins. Bringing either of these pins HIGH will set the output level of its respective channel to 3V. Bringing either of these pins LOW will set the output level of its respective channel to 1.8V.
13	CSEL	Input. The CSEL pin selects which set of SIM/Smart Card pins are active.
14, 15	CLKRUNA, CLKRUNB	Inputs. The CLKRUNA and CLKRUNB inputs are used to select whether the clock signal is always sent to card sockets that are enabled or whether the clock is gated with the CSEL pin.
Exposed Pad	GND	Ground. This ground pad must be soldered directly to a PCB ground plane.

ELECTRICAL CHARACTERISTICS

(V_{BAT} = 3.3V, DV_{CC} = 1.8V, T_A = 25℃, unless otherwise specified.)

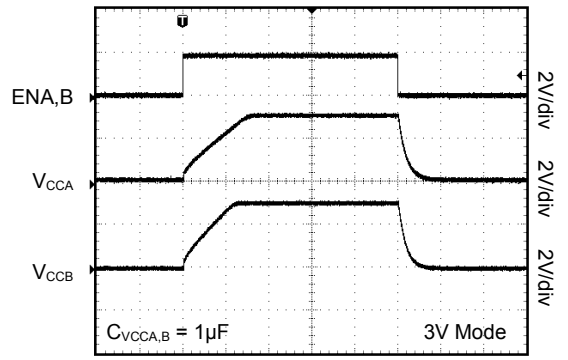
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power Supply					
V_{BAT} Operating Voltage		2.7		5.5	V
V_{BAT} Operating Current	ENABLEA = DV_{CC}, ENABLEB = 0V, V_{CCA} = 3V, I_{CCA} = 0μA		90	170	μA
	ENABLEA = DV_{CC}, ENABLEB = 0V, V_{CCA} = 1.8V, I_{CCA} = 0μA		78	160	
V_{BAT} Shutdown Current	DV_{CC} = 0V		0.01	2	μA
DV_{CC} Operating Voltage		1.4		5.5	V
DV_{CC} Operating Current			5	10	μA
DV_{CC} Shutdown Current			0.01	2	μA
SIM Card Supplies					
$V_{CCA,B}$ Output Voltage	3V Mode, 0mA < $I_{CCA,B}$ < 250mA	2.895	3	3.105	V
	1.8V Mode, 0mA < $I_{CCA,B}$ < 250mA	1.737	1.8	1.863	
$V_{CCA,B}$ Turn-On Time	$I_{CCA,B}$ = 0mA, ENABLEA,B↑ to $V_{CCA,B}$ at 90% Selected Voltage		0.5		ms
Channel Switching Time	ENABLEA = ENABLEB = RSTIN = DV_{CC}, CSEL↑ to RSTB↑		1		μs
CLKA,B (1)					
Low Level Output Voltage (V_{OL})	Sink Current = -200μA			0.15	V
High Level Output Voltage (V_{OH})	Source Current = 200μA	$V_{CCA,B}$ - 0.15			V
Rise/Fall Time	Loaded with 50pF (10% to 90%)		8		ns
CLKA,B Frequency				10	MHz
RSTA,B (1)					
Low Level Output Voltage (V_{OL})	Sink Current = -200μA			0.2	V
High Level Output Voltage (V_{OH})	Source Current = 200μA	$V_{CCA,B}$ - 0.2			V
Rise/Fall Time	Loaded with 50pF (10% to 90%)		80		ns
I/OA,B (1)					
Low Level Output Voltage (V_{OL})	Sink Current = -1mA (V_{DATA} = 0V)			0.3	V
High Level Output Voltage (V_{OH})	Source Current = 20μA (V_{DATA} = DV_{CC})	0.85 × $V_{CCA,B}$			V
Rise/Fall Time	Loaded with 50pF (10% to 90%)		200		ns
Short-Circuit Current	V_{DATA} = 0V		5	12	mA
DATA					
Low Level Output Voltage (V_{OL})	Sink Current = -500μA ($V_{I/OA,B}$ = 0V)			0.3	V
High Level Output Voltage (V_{OH})	Source Current = 20μA ($V_{I/OA,B}$ = $V_{CCA,B}$)	0.8 × DV_{CC}			V
Rise/Fall Time	Loaded with 50pF (10% to 90%)		200		ns
ENABLEA, ENABLEB, RSTIN, CLKIN, CSEL, VSELA, VSELB, CLKRUNA, CLKRUNB					
Low Input Threshold (V_{IL})	T_A = -40℃ to +85℃			0.15 × DV_{CC}	V
High Input Threshold (V_{IH})	T_A = -40℃ to +85℃	0.85 × DV_{CC}			V
Input Current (I_{IH}/I_{IL})		-1		1	μA

NOTE: 1. This specification applies to both Smart Card classes.

TYPICAL PERFORMANCE CHARACTERISTICS

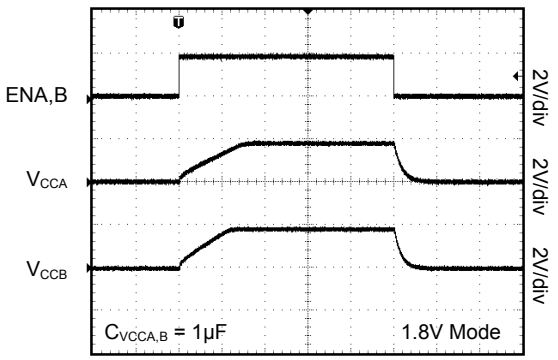
V_{BAT} = 3.3V, DV_{CC} = 1.8V, T_A = 25℃, unless otherwise specified.

$V_{CCA,B}$ Turn On and Turn Off



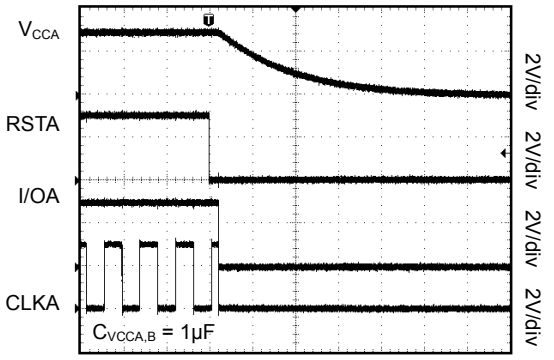
Time (400μs/div)

$V_{CCA,B}$ Turn On and Turn Off



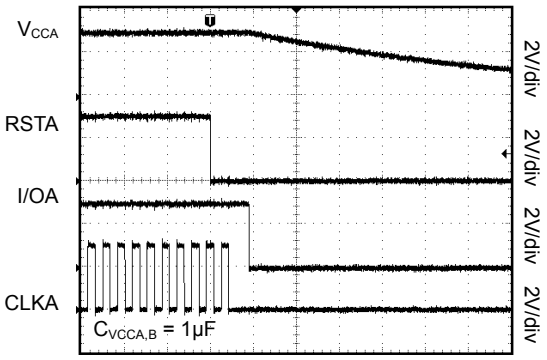
Time (400μs/div)

Deactivation Sequence



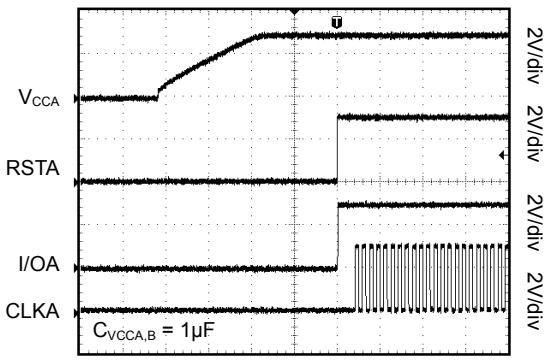
Time (40μs/div)

Deactivation Sequence



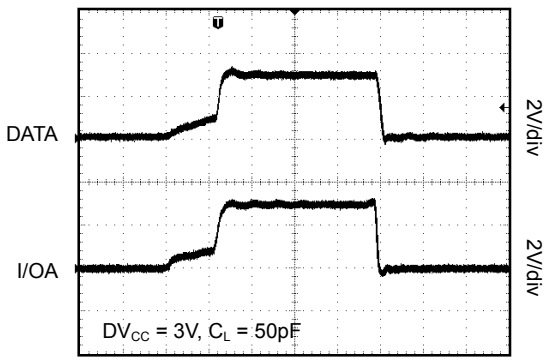
Time (10μs/div)

Activation Sequence



Time (200μs/div)

Bidirectional Data Transfer

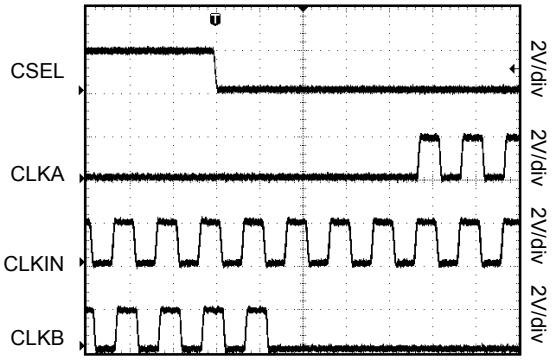


Time (200ns/div)

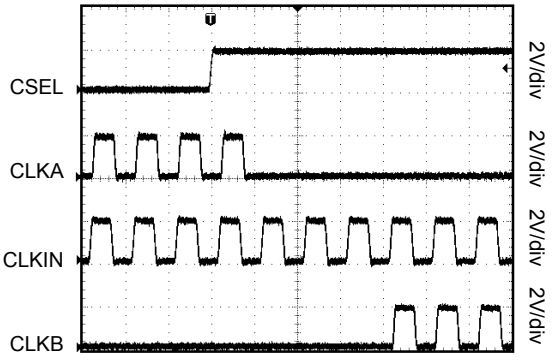
TYPICAL PERFORMANCE CHARACTERISTICS

V_{BAT} = 3.3V, DV_{CC} = 1.8V, T_A = 25℃, unless otherwise specified.

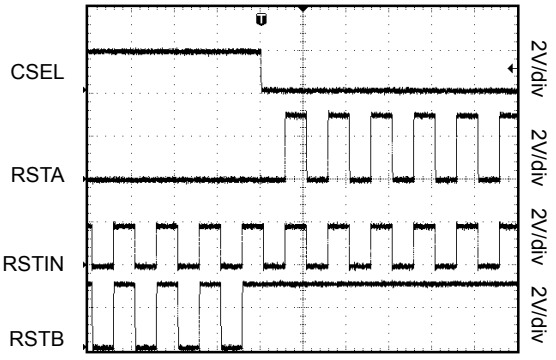
Clock Signal is Transmitted to Channel A



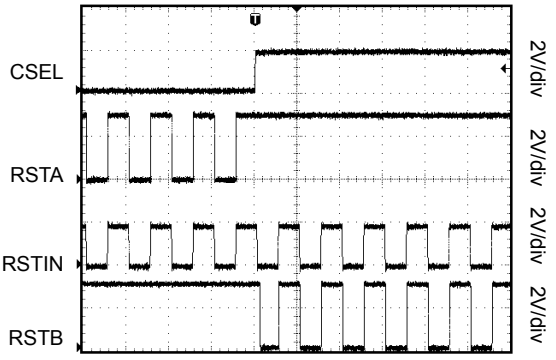
Clock Signal is Transmitted to Channel B



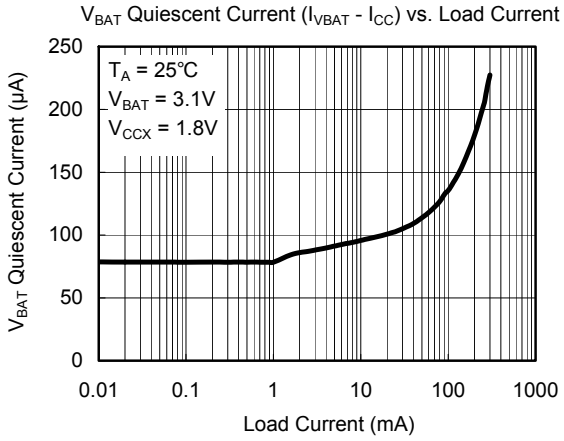
Reset Signal is Transmitted to Channel A

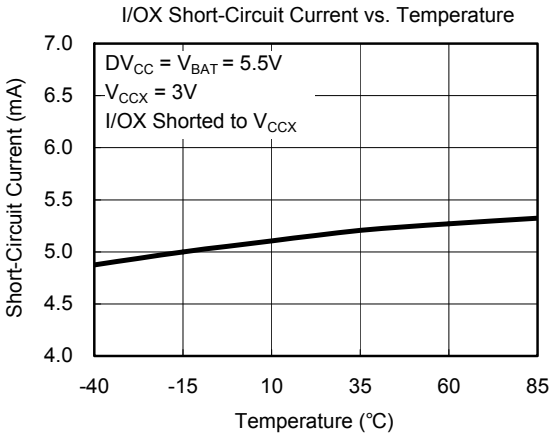


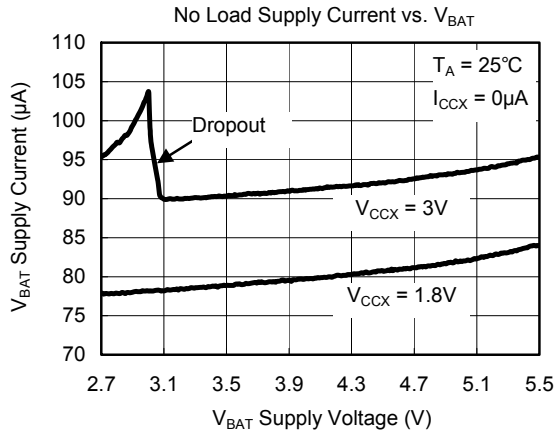
Reset Signal is Transmitted to Channel B



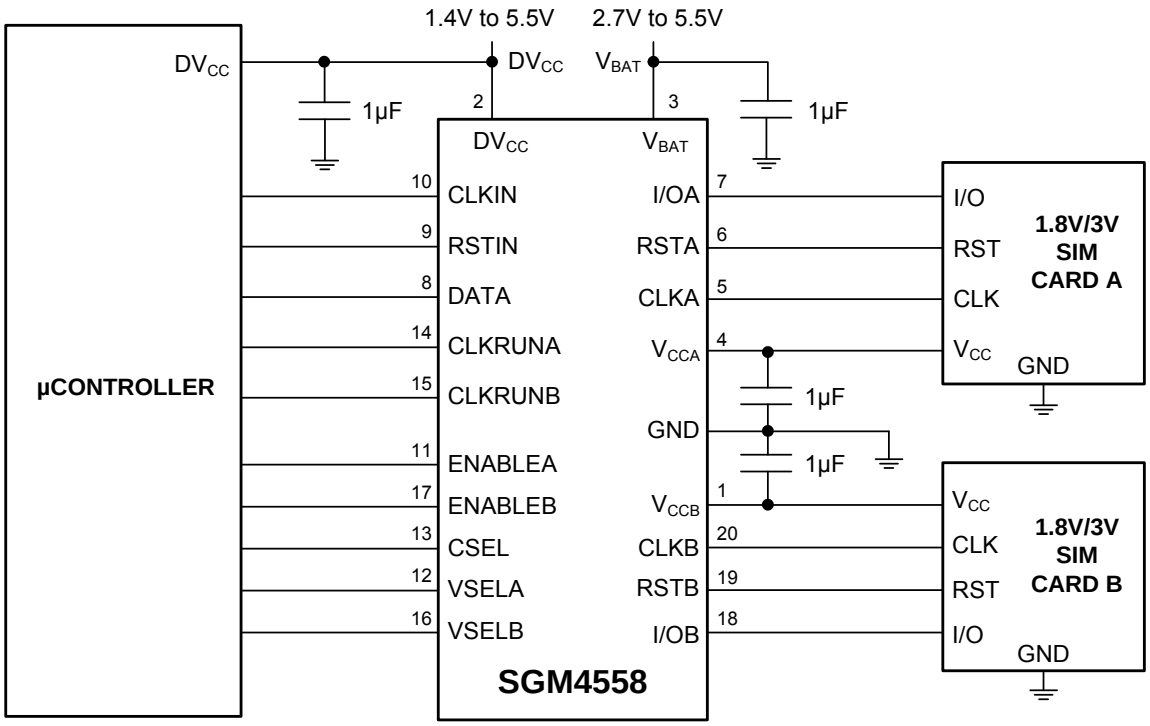
TYPICAL PERFORMANCE CHARACTERISTICS



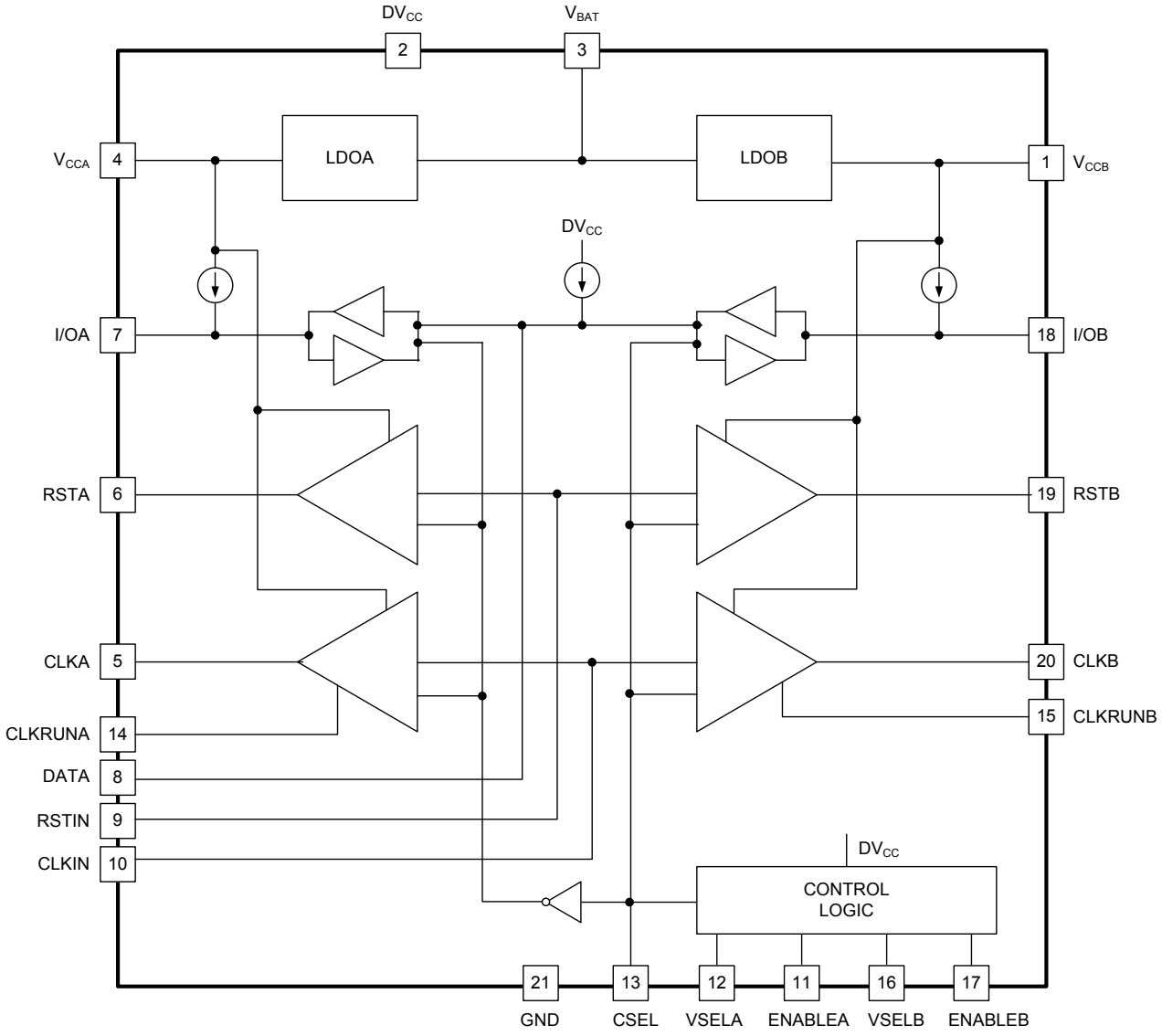




TYPICAL OPERATION CIRCUIT



BLOCK DIAGRAM



OPERATION

The SGM4558 features two independent SIM/Smart Card channels. Only one of these channels may be open for communication at a time, however both channels can be enabled and made ready for communication using the ENABLEA and ENABLEB pins. This allows faster transition from one channel to the other. Each channel is able to produce two voltage levels, 1.8V and 3V. The channel selection and voltage selection are controlled by the CSEL, VSELA and VSELB pins as shown in the table below:

Table 1. Channel and Voltage Truth Table

CSEL	VSELA	VSELB	SELECTED CARD	VOLTAGES	
				A	B
0	0	0	A	1.8V	1.8V
0	0	1	A	1.8V	3V
0	1	0	A	3V	1.8V
0	1	1	A	3V	3V
1	0	0	B	1.8V	1.8V
1	0	1	B	1.8V	3V
1	1	0	B	3V	1.8V
1	1	1	B	3V	3V

Bidirectional Channels

The bidirectional channels are level shifted to the appropriate $V_{CCA,B}$ voltages at the I/OA,B pins. An NMOS pass transistor performs the level shifting. The gate of the NMOS transistor is biased such that the transistor is completely off when both sides have relinquished the channel. If one side of the channel asserts a LOW, then the transistor will convey the LOW to the other side. Note that current passes from the receiving side of the channel to the transmitting side. The low output voltage of the receiving side will be dependent upon the voltage at the transmitting side plus the IR drop of the pass transistor.

When a card socket is selected, it becomes a candidate to drive data on the DATA pin and likewise receive data from the DATA pin. When a card socket is deselected, its I/O pin will be pulled HIGH and communication with the DATA pin will be disabled. If both channels are disabled, a weak pull-up ensures that the DATA pin is held HIGH, as long as DV_{CC} is powered.

Pull-Up Current Sources

The current sources on the bidirectional pins (DATA, I/OA,B) are activated to achieve a fast rise time with a relatively small static current. Once a bidirectional pin is relinquished, a start-up current begins to charge the node.

Reset Channels

When a card is selected, the reset channel provides a level shifted path from the RSTIN pin to the RST pin of the selected card. When a card is deselected, the last state of the RSTA,B pin is latched. This allows a deselected card to remain active, and therefore eliminates delays associated with card initialization.

Clock Run Mode

Various SIM/Smart Cards may have different requirements for the state of the clock pin when the channel is not open for communication. The CLKRUNA,B pins allow the user to select whether the clock is brought LOW after the channel is deselected or allowed to run. If a channel is enabled, bringing its CLKRUN pin HIGH will transmit the clock to the corresponding card socket, whether or not the channel is selected using the CSEL.

APPLICATION INFORMATION

Activation/Deactivation

Activation and deactivation sequencing is handled by built-in circuitry. Each channel may be activated or deactivated independently of the other. The activation sequence for each channel is initiated by bringing the ENABLEA,B pin HIGH. The activation sequence is outlined below:

1. The RSTA,B, CLKA,B and I/OA,B pins are held LOW.
2. $V_{CCA,B}$ is enabled.
3. After $V_{CCA,B}$ is stable at its selected level, the I/OA,B and RSTA,B channels are enabled.
4. The clock channel is enabled on the rising edge of the second clock cycle after the I/OA,B pin is enabled.

The deactivation sequence is initiated by bringing the ENABLEA,B pin LOW. The deactivation sequence is outlined below:

1. The reset channel is disabled and RSTA,B is brought LOW.
2. The clock channel is disabled and the CLKA,B pin is brought LOW two clock cycles after ENABLEA,B is brought LOW. If the clock is not running, the clock channel will be disabled approximately 9μs after the ENABLEA,B pin is brought LOW.
3. The I/O channel is disabled and the I/OA,B pin is brought LOW approximately 9μs after the ENABLEA, B pin is brought LOW.
4. $V_{CCA,B}$ will be depowered after the I/OA,B pin is brought LOW.

The activation or deactivation sequences will take place every time a card channel is enabled or disabled. When a channel is deselected using the CSEL pin, the RSTA,B state is latched, the I/OA,B channel becomes high impedance and CLKA,B is brought LOW after a maximum of two clock cycles.

Fault Detection

The $V_{CCA,B}$, I/OA,B, RSTA,B, CLKA,B and DATA pins are all protected against short-circuit faults. While there are no logic outputs to indicate that a fault has occurred, these pins will be able to tolerate the fault condition until it has been removed.

The $V_{CCA,B}$, I/OA,B, and RSTA,B pins possess fault protection circuitry which will limit the current available to the pins. Each V_{CC} pin is capable of supplying approximately 300mA (TYP) before the output voltage is reduced.

The CLKA,B pins are designed to tolerate faults by reducing the current drive capability of their output stages. After a fault is detected by the internal fault detection logic, the logic waits for a fault detection delay to elapse before reducing the current drive capability of the output stage. The reduced current drive allows the SGM4558 to detect when the fault has been removed.

Capacitor Selection

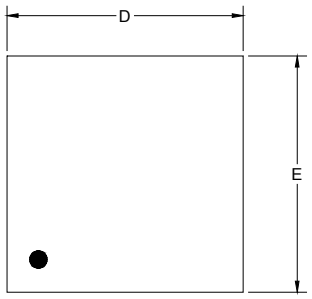
A total of four capacitors is required to operate the SGM4558. V_{BAT} and DV_{CC} should be bypassed with 1μF ceramic capacitors. The $V_{CCA,B}$ outputs should be bypassed to GND with a 1μF capacitor.

ESD Protection

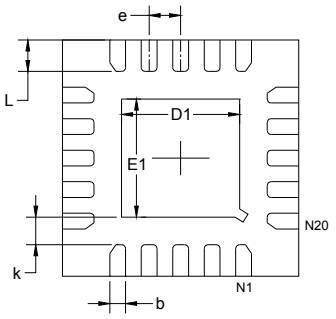
In order to ensure proper ESD protection, careful board layout is required. The GND pin should be tied directly to a ground plane. The $V_{CCA,B}$ capacitors should be located very close to the $V_{CCA,B}$ pins and tied immediately to the ground plane.

PACKAGE OUTLINE DIMENSIONS

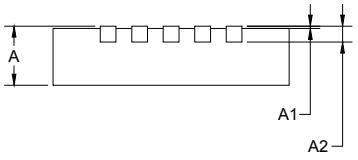
TQFN-3×3-20L



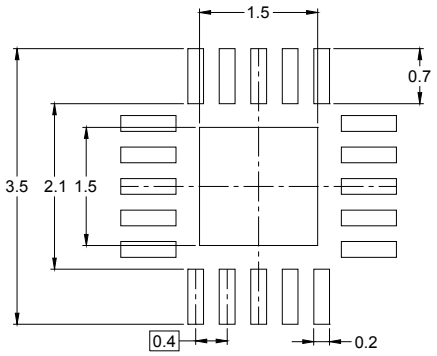
TOP VIEW



BOTTOM VIEW



SIDE VIEW

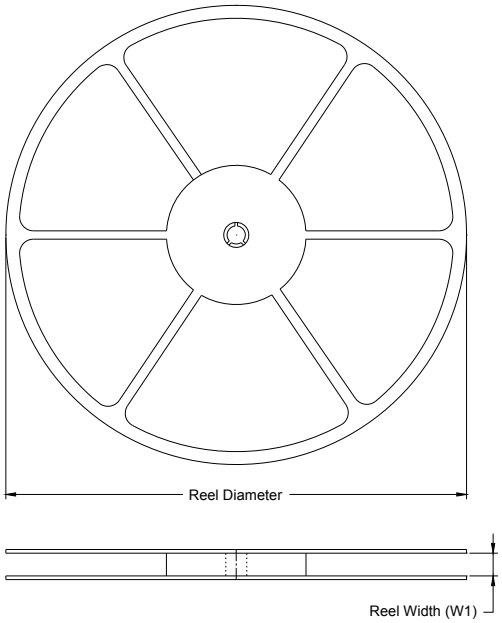


RECOMMENDED LAND PATTERN (Unit: mm)

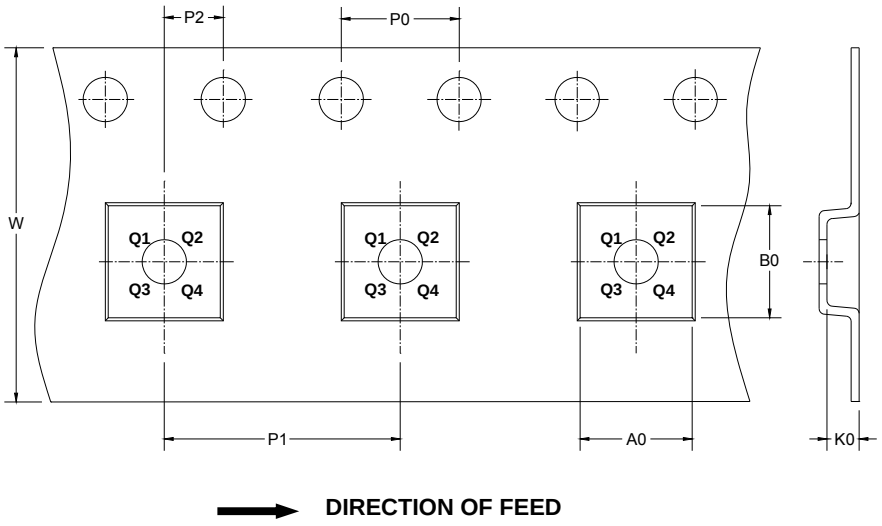
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E	2.924	3.076	0.115	0.121
E1	1.400	1.600	0.055	0.063
k	0.200 MIN		0.008 MIN	
b	0.150	0.250	0.006	0.010
e	0.400 TYP		0.016 TYP	
L	0.324	0.476	0.013	0.019

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

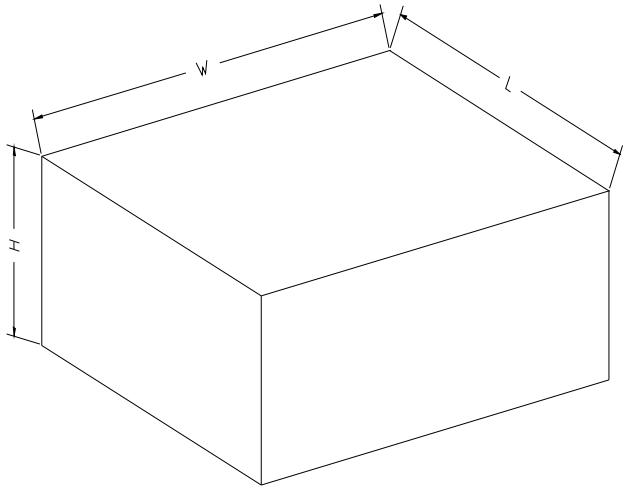


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-20L	13″	12.4	3.3	3.3	1.1	4.0	4.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5