SGM4560
CA Card Power Supply and Level Translator

GENERAL DESCRIPTION

The SGM4560 provides the power conversion and signal level shifting needed for 3.3V or 5.0V CA cards. The part meets all type approval requirements for 3.3V and 5.0V CA cards and contains an LDO linear regulator to power 3.3V or 5.0V CA cards from a 3.3V to 5.5V input. The output voltage is selected with a single pin and up to 200mA of load current can be supplied.

Internal level translators allow controllers operating with supplies as low as 1.6V to interface with 3.3V or 5.0V CA cards. Battery life is maximized by a low operating current of typically 100μA and a shutdown current of typically less than 1μA.

The SGM4560 is available in the Green TSSOP-14 package. It operates over an ambient temperature range of -40℃ to +85℃.

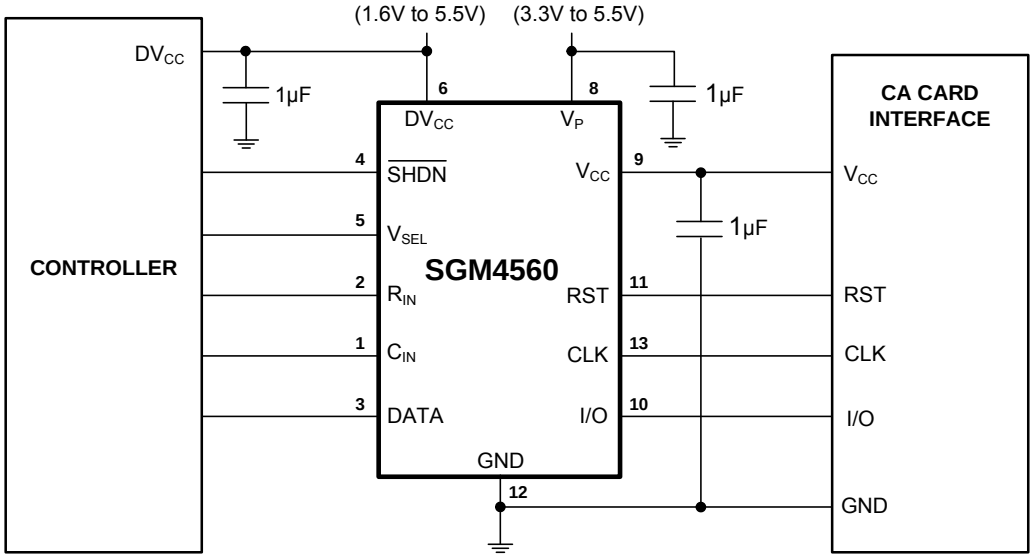
FEATURES

- **CA Card Power Supply: 3.3V/5.0V at 200mA**
- **3.3V to 5.5V Input Voltage Range**
- **1.6V to 5.5V Controller Voltage Range**
- **Fast Signal Rise Times**
- **Built-In Fault Protection Circuitry**
- **Level Translators to 3.3V or 5.0V**
- **Low Operating and Shutdown Current**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green TSSOP-14 Package**

APPLICATIONS

CA Card Interface

TYPICAL APPLICATION



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM4560	TSSOP-14	-40℃ to +85℃	SGM4560YTS14G/TR	SGM4560 YTS14 XXXXX	Tape and Reel, 3000

NOTE: **XXXXX** = Date Code and Vendor Code.

ABSOLUTE MAXIMUM RATINGS

V_P, DV_{CC} to GND.....-0.3V to 6V
V_{CC} to GND.....-0.3V to V_P + 0.3V
$\overline{SHDN}$, V_{SEL}, R_{IN}, C_{IN} to GND.....-0.3V to 6V
CLK, RST, I/O to GND..... -0.3V to V_{CC} + 0.3V
DATA to GND.....-0.3V to DV_{CC}+0.3V
V_{CC} Short-Circuit Duration..... Infinite
Package Thermal Resistance
TSSOP-14, θ_{JA}.....154℃/W
Operating Temperature Range..... -40℃ to +85℃
Junction Temperature..... 150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering, 10sec)..... 260℃
ESD Susceptibility
HBM.....4000V
MM.....400V

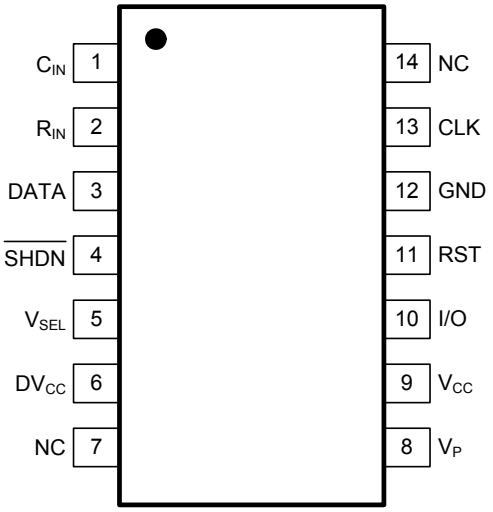
NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute Maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATION (TOP VIEW)



TSSOP-14

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	C_{IN}	Clock Input from the Controller.
2	R_{IN}	Reset Input from the Controller.
3	DATA	Controller Side Data I/O. This pin is used for bidirectional data transfer. A weak pull-up current source ensures that the DATA pin is held HIGH during shutdown, as long as DV_{CC} is powered.
4	$\overline{SHDN}$	Controller Driven Shutdown Pin. This pin should be HIGH (DV_{CC}) for normal operation and LOW to activate a low current shutdown mode.
5	V_{SEL}	V_{CC} Voltage Select Pin. A low level selects V_{CC} = 3.3V while driving this pin to DV_{CC} selects V_{CC} = 5.0V.
6	DV_{CC}	Supply Voltage for the Controller Side I/O Pins (C_{IN}, R_{IN}, DATA). When below 1.2V, the V_{CC} supply is disabled. This pin should be bypassed with a 1μF ceramic capacitor close to the pin.
7, 14	NC	No Connect.
8	V_P	V_{CC} Supply Input. This pin can be between 3.3V and 5.5V for normal operation. V_P quiescent current reduces to 0.4μA (TYP) in shutdown. This pin should be bypassed with a 1μF ceramic capacitor close to the pin.
9	V_{CC}	CA Card V_{CC} Supply. A 1μF low ESR capacitor needs to be connected close to the V_{CC} pin for stable operation. This pin is discharged to GND during shutdown.
10	I/O	CA Card Side Data I/O. This pin is pulled to ground during shutdown.
11	RST	Reset Output Pin for the CA Card. This pin is pulled to ground during shutdown.
12	GND	Ground. Proper grounding and bypassing are required to meet high ESD specifications.
13	CLK	Clock Output Pin for the CA Card. This pin is pulled to ground during shutdown. Fast rising and falling edges necessitate careful board layout for the CLK node.

ELECTRICAL CHARACTERISTICS

(V_P = 5.0V, DV_{CC} = 1.8V, T_A = 25℃, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power Supply					
V_P Operating Voltage		3.3		5.5	V
V_P Operating Current	V_P = 5.5V, I_{VCC} = 0mA		100	195	μA
V_P Shutdown Current	$\overline{SHDN}$ = 0V, V_P = 5.5V		0.4	8	μA
DV_{CC} Operating Voltage		1.6		5.5	V
DV_{CC} Operating Current			5	10	μA
DV_{CC} Shutdown Current	$\overline{SHDN}$ = 0V		0.01	1	μA
DV_{CC} Under-Voltage Lockout		0.8	1.0	1.2	V
V_{CC} Output Voltage	V_{SEL} = DV_{CC}, V_P = 5.0V, I_{VCC} = 200mA		4.88		V
	V_{SEL} = DV_{CC}, V_P = 5.5V, I_{VCC} = 0mA to 200mA	4.825	5.0	5.175	
	V_{SEL} = 0V, V_P = 5.5V, I_{VCC} = 0mA to 200mA	3.185	3.3	3.415	
Controller Inputs/Outputs					
Input Voltage Range	$\overline{SHDN}$, V_{SEL}, R_{IN}, C_{IN}, DATA	0		DV_{CC}	V
High Input Threshold Voltage (V_{IH})	R_{IN}, C_{IN}, T_A = -40℃ to +85℃	0.9 × DV_{CC}			V
Low Input Threshold Voltage (V_{IL})	R_{IN}, C_{IN}, T_A = -40℃ to +85℃			0.1 × DV_{CC}	V
High Input Threshold Voltage (V_{IH})	$\overline{SHDN}$, V_{SEL}, T_A = -40℃ to +85℃	1.55			V
Low Input Threshold Voltage (V_{IL})	$\overline{SHDN}$, V_{SEL}, T_A = -40℃ to +85℃			0.35	V
High Level Input Current (I_{IH})	DATA	-5		5	μA
Low Level Input Current (I_{IL})	DATA			1.75	mA
High Level Output Voltage (V_{OH})	DATA, I_{OH} = 20μA, I/O = V_{CC}	0.9 × DV_{CC}			V
Low Level Output Voltage (V_{OL})	DATA, I_{OL} = -200μA, I/O = 0V			0.2	V
DATA Pull-Up Current	DATA = 1V		200	600	μA

ELECTRICAL CHARACTERISTICS

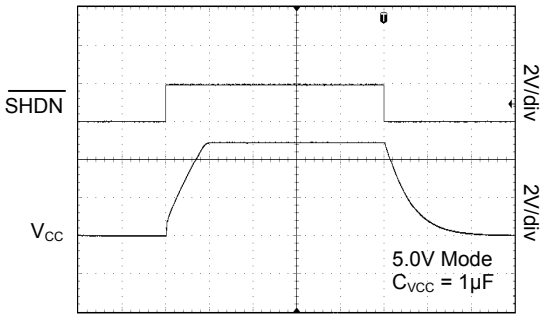
(V_P = 5.0V, DV_{CC} = 1.8V, T_A = 25℃, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CA Card Inputs/Outputs (V_{CC} = 3.3V)					
High Level Output Voltage (V_{OH})	I/O, I_{OH} = 20μA, DATA = DV_{CC}	0.9 × V_{CC}			V
Low Level Output Voltage (V_{OL})	I/O, I_{OL} = -1mA, DATA = 0V			0.3	V
High Level Output Voltage (V_{OH})	CLK, I_{OH} = 20μA	0.9 × V_{CC}			V
Low Level Output Voltage (V_{OL})	CLK, I_{OL} = -200μA			0.15	V
High Level Output Voltage (V_{OH})	RST, I_{OH} = 20μA	0.9 × V_{CC}			V
Low Level Output Voltage (V_{OL})	RST, I_{OL} = -200μA			0.2	V
I/O Pull-Up Current	I/O = 1V		320	850	μA
CA Card Inputs/Outputs (V_{CC} = 5.0V)					
High Level Output Voltage (V_{OH})	I/O, I_{OH} = 20μA, DATA = DV_{CC}	0.9 × V_{CC}			V
Low Level Output Voltage (V_{OL})	I/O, I_{OL} = -1mA, DATA = 0V			0.3	V
High Level Output Voltage (V_{OH})	CLK, I_{OH} = 20μA	0.9 × V_{CC}			V
Low Level Output Voltage (V_{OL})	CLK, I_{OL} = -200μA			0.15	V
High Level Output Voltage (V_{OH})	RST, I_{OH} = 20μA	0.9 × V_{CC}			V
Low Level Output Voltage (V_{OL})	RST, I_{OL} = -200μA			0.2	V
I/O Pull-Up Current	I/O = 1V		400	1000	μA
CA Card Timing Parameters					
CLK Rise/Fall Time	Loaded with 30pF, V_{CC} = 3.3V/5.0V (10% to 90%)		3		ns
RST Rise/Fall Time	Loaded with 30pF, V_{CC} = 3.3V/5.0V (10% to 90%)		30		ns
I/O Rise/Fall Time	Loaded with 30pF, V_{CC} = 3.3V/5.0V (10% to 90%)		150		ns
CLK Frequency	Loaded with 30pF			10	MHz
V_{CC} Turn-On Time	$\overline{SHDN}$ = 1		0.4		ms
V_{CC} Discharge Time to 1V	$\overline{SHDN}$ = 0		0.4		ms

TYPICAL PERFORMANCE CHARACTERISTICS

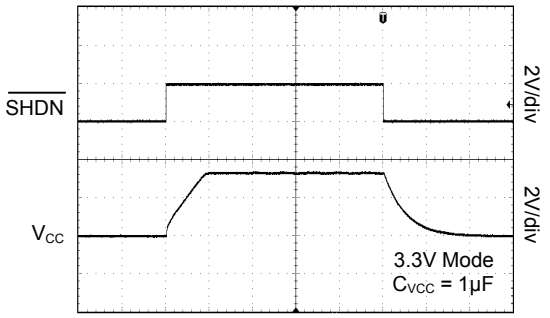
V_P = 5.0V, DV_{CC} = 1.8V, T_A = 25℃, unless otherwise specified.

V_{CC} Turn On and Turn Off



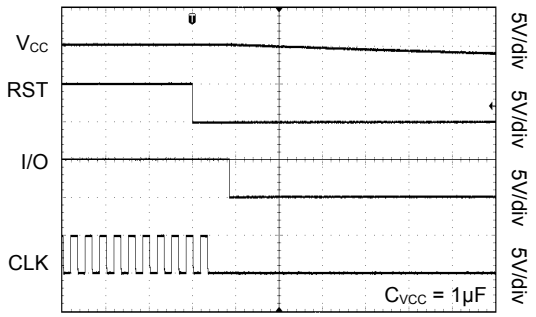
Time (400μs/div)

V_{CC} Turn On and Turn Off



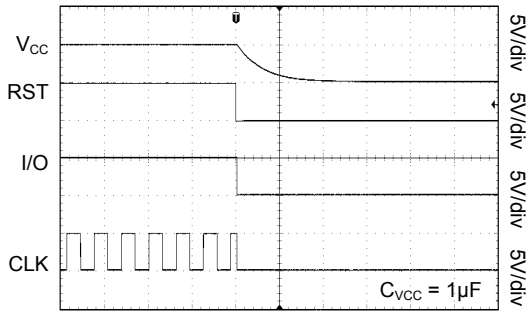
Time (400μs/div)

Deactivation Sequence



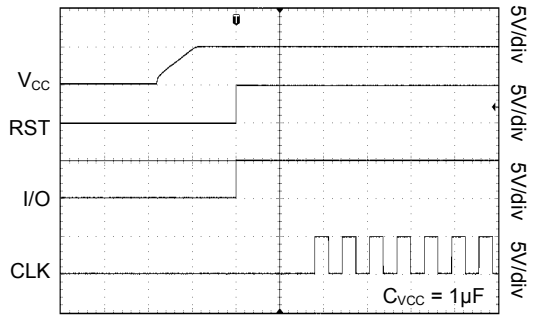
Time (10μs/div)

Deactivation Sequence



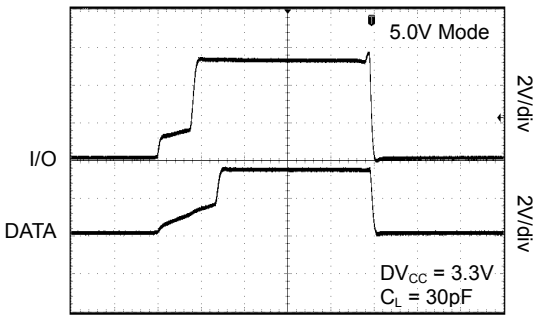
Time (400μs/div)

Activation Sequence



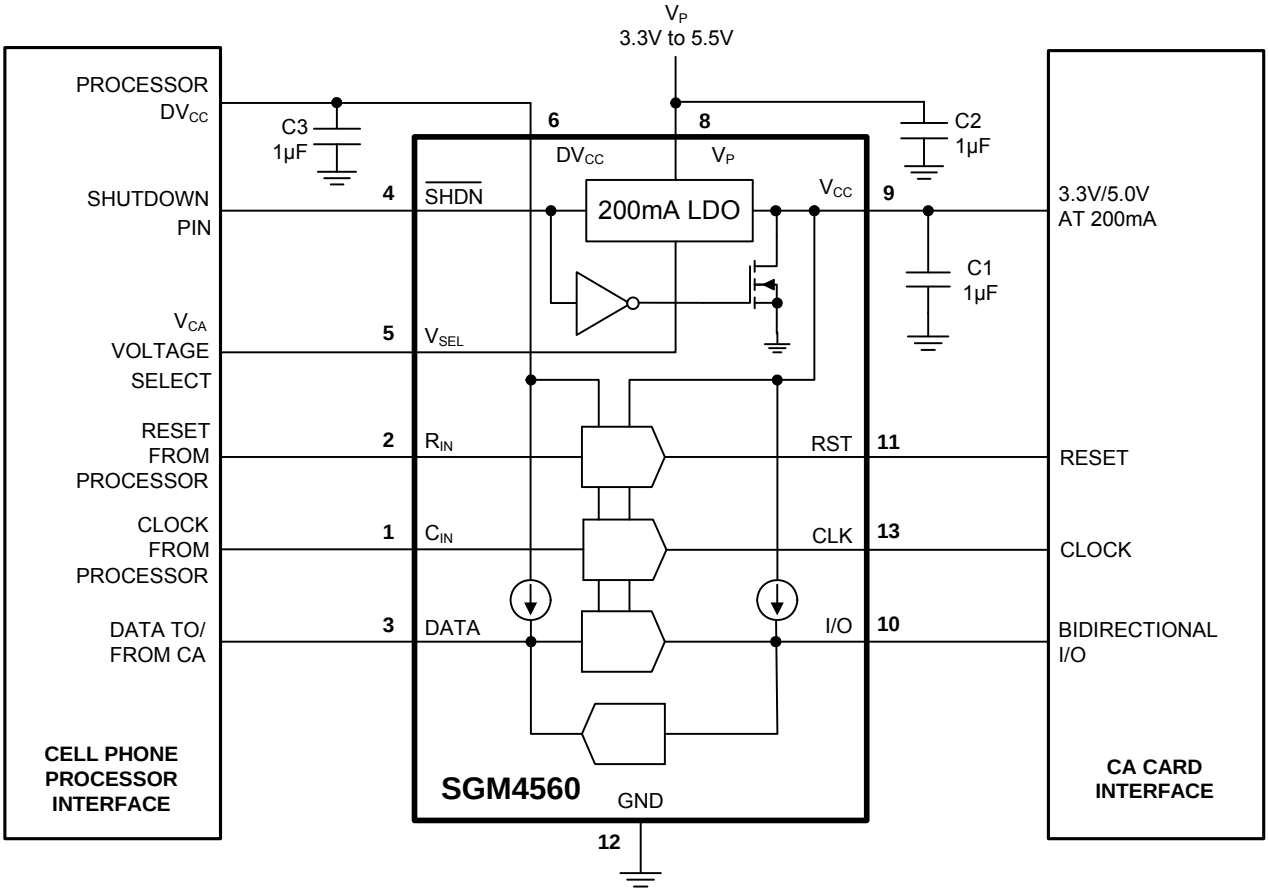
Time (400μs/div)

Bidirectional Data Transfer



Time (200ns/div)

BLOCK DIAGRAM



APPLICATION INFORMATION

The SGM4560 provides both regulated power and internal level translators to allow low voltage controllers to interface with 3.3V or 5.0V CA cards.

V_{CC} Voltage Regulator

The V_{CC} voltage regulator is a 200mA low dropout (LDO) regulator with a digitally selected 3.3V or 5.0V output. The output voltage is selected via the V_{SEL} pin. The V_{CC} output should be bypassed with a 1μF capacitor. V_P should be bypassed with a 1μF ceramic capacitor.

Level Translators

All CA cards contain a clock input, a reset input and a bidirectional data input/output. The SGM4560 provides level translators to allow controllers to communicate with the CA card. The CLK and RST lines to the CA card are level shifted from the controller supply (GND to DV_{CC}) to the CA card supply (GND to V_{CC}). The bidirectional channel is level shifted to the appropriate V_{CC} voltage at the I/O pin. An NMOS pass transistor performs the level shifting. The gate of the NMOS transistor is biased such that the transistor is completely off when both sides have relinquished the channel. If one side of the channel asserts a LOW, then the transistor will convey the LOW to the other side. Note that current passes from the receiving side of the channel to the transmitting side. The low output voltage of the receiving side will be dependent upon the voltage at the transmitting side plus the IR drop of the pass transistor.

Pull-Up Current Sources

The current sources on the bidirectional pins (DATA, I/O) are activated to achieve a fast rise time with a relatively small static current. Once a bidirectional pin is relinquished, a start-up current begins to charge the node.

Activation/Deactivation

Activation and deactivation sequencing is handled by built-in circuitry. The activation sequence for the channel is initiated by bringing the $\overline{SHDN}$ pin HIGH. The activation sequence is outlined below:

1. The RST, CLK and I/O pins are held LOW.
2. V_{CC} is enabled.
3. After V_{CC} is stable at its selected level, the I/O and RST channels are enabled.
4. The clock channel is enabled on the rising edge of the second clock cycle after the I/O pin is enabled.

The deactivation sequence is initiated by bringing the $\overline{SHDN}$ pin LOW. The deactivation sequence is outlined below:

1. The reset channel is disabled and RST is brought LOW.
2. The clock channel is disabled and the CLK pin is brought LOW two clock cycles after $\overline{SHDN}$ is brought LOW. If the clock is not running, the clock channel will be disabled approximately 9μs after the $\overline{SHDN}$ pin is brought LOW.
3. The I/O channel is disabled and the I/O pin is brought LOW approximately 9μs after the $\overline{SHDN}$ pin is brought LOW.
4. V_{CC} will be depowered after the I/O pin is brought LOW.

Fault Detection

The V_{CC}, I/O, RST, CLK and DATA pins are all protected against short-circuit faults. While there are no logic outputs to indicate that a fault has occurred, these pins will be able to tolerate the fault condition until it has been removed.

The V_{CC}, I/O, and RST pins possess fault protection circuitry which will limit the current available to the pins. The V_{CC} pin is capable of supplying approximately 300mA (TYP) before the output voltage is reduced.

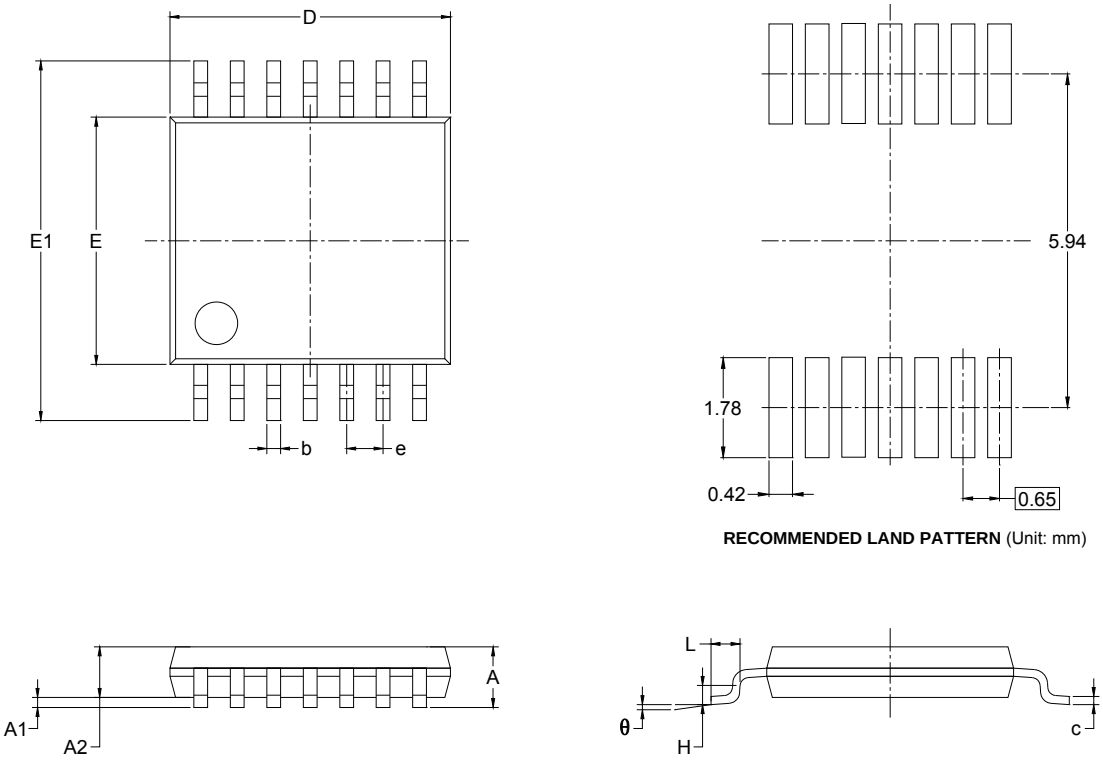
The CLK pin is designed to tolerate faults by reducing the current drive capability of its output stage. After a fault is detected by the internal fault detection logic, the logic waits for a fault detection delay to elapse before reducing the current drive capability of the output stage. The reduced current drive allows the SGM4560 to detect when the fault has been removed.

ESD Protection

In order to ensure proper ESD protection, careful board layout is required. The GND pin should be tied directly to a ground plane. The V_{CC} capacitor should be located very close to the V_{CC} pin and tied directly to the ground plane.

PACKAGE OUTLINE DIMENSIONS

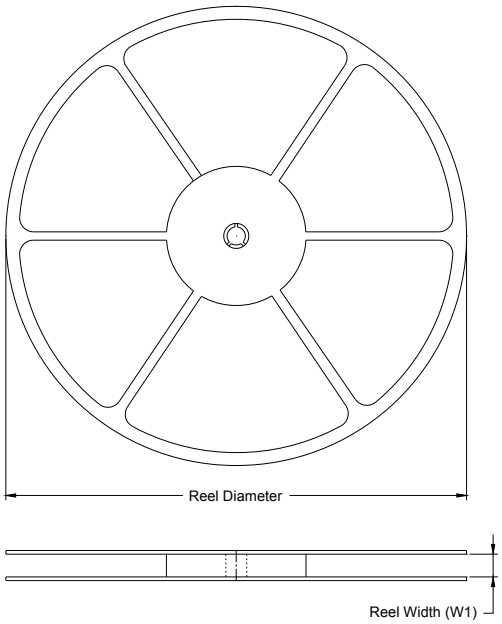
TSSOP-14



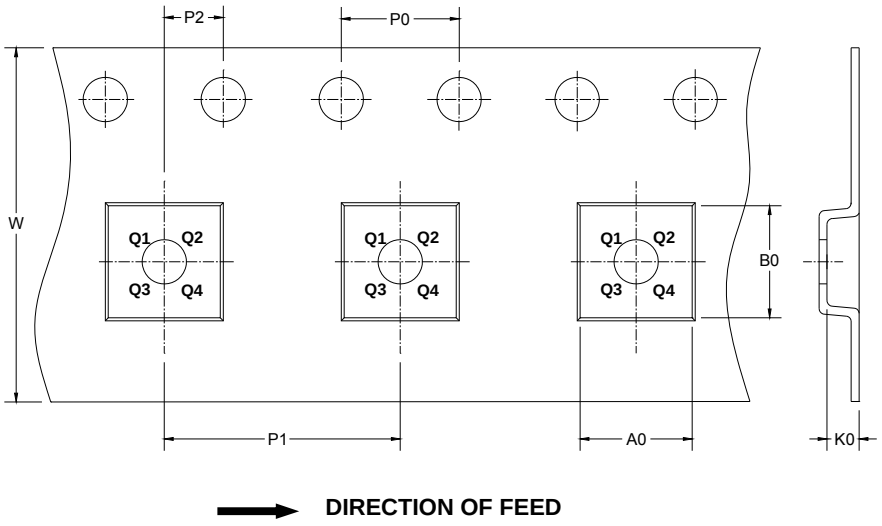
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

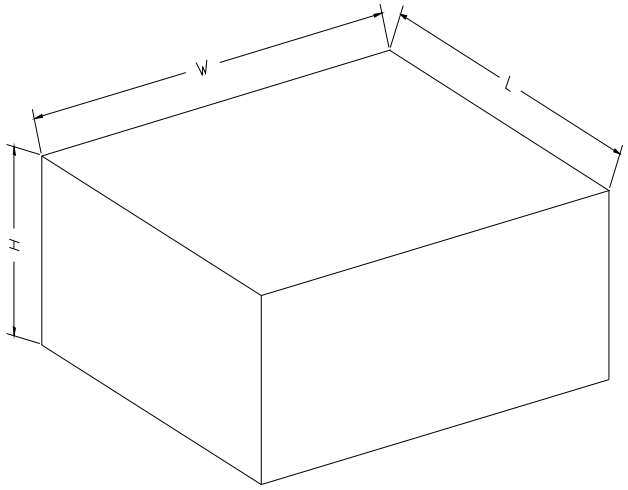


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.6	1.2	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5