SGM4574
4-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

GENERAL DESCRIPTION

This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A ports are designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65V to 5.5V. V_{CCA} must be less than or equal to V_{CCB}. The B ports are designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 2.3V to 5.5V. This allows for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state.

The SGM4574 is designed so that the OE input circuit is supplied by V_{CCA}.

To ensure the high-impedance state during power-up or power-down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SGM4574 is available in Green SOIC-14, UTQFN-1.8×1.8-12L and TQFN-2×2-12L packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **No Direction-Control Signal Needed**
- **Data Rates**
  24Mbps (Push-Pull)
  2Mbps (Open-Drain)
- **1.65V to 5.5V on A ports and 2.3V to 5.5V on B ports ($V_{CCA} \leq V_{CCB}$)**
- **No Power-Supply Sequencing Required**
  Either V_{CCA} or V_{CCB} Can Be Ramped First
- **Available in Green SOIC-14, UTQFN-1.8×1.8-12L and TQFN-2×2-12L Packages**

APPLICATIONS

Handset
Smartphone
Tablet
Desktop PC

TYPICAL APPLICATION

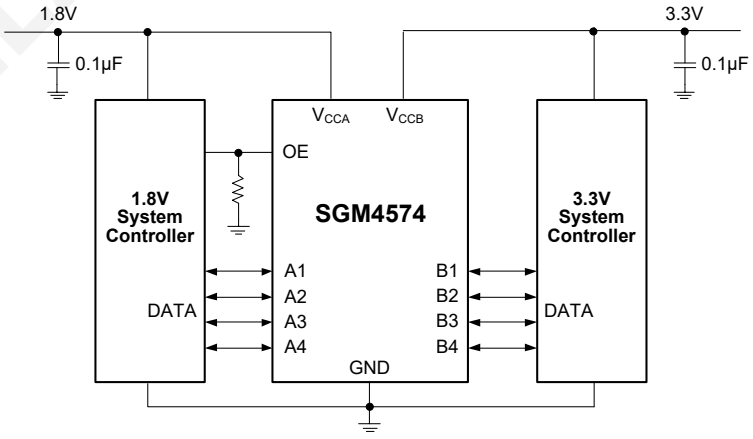


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4574	TQFN-2×2-12L	-40℃ to +85℃	SGM4574YTQM12G/TR	4574 XXXX	Tape and Reel, 3000
	SOIC-14	-40℃ to +85℃	SGM4574YS14G/TR	SGM4574YS14 XXXXX	Tape and Reel, 2500
	UTQFN-1.8×1.8-12L	-40℃ to +85℃	SGM4574YUQN12G/TR	4574 XXXX	Tape and Reel, 3000

NOTE: XXXX = Date Code. XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range
V_{CCA} ..... -0.3V to 6V
V_{CCB} ..... -0.3V to 6V
A Ports, B Ports, OE Input Voltage Range, V_I (1)
..... -0.3V to 6V
Voltage Range Applied to Any Output in the High- Impedance or Power-Off State, V_O (1)
A Ports ..... -0.3V to 6V
B Ports ..... -0.3V to 6V
Voltage Range Applied to Any Output in the High or Low State, V_O (1) (2)
A Ports ..... -0.3V to V_{CCA} + 0.3V
B Ports ..... -0.3V to V_{CCB} + 0.3V
Input Clamp Current, I_{IK} (V_I < 0) ..... -50mA
Output Clamp Current, I_{OK} (V_O < 0) ..... -25mA
Continuous Output Current, I_O ..... ±50mA
Continuous Current through V_{CCA}, V_{CCB}, or GND ..... ±100mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

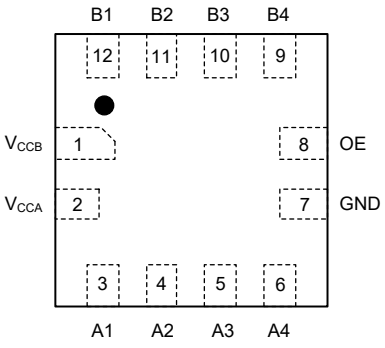
RECOMMENDED OPERATING CONDITIONS (3, 4)

Supply Voltage Range (5)
V_{CCA} ..... 1.65V to 5.5V
V_{CCB} ..... 2.3V to 5.5V
High-Level Input Voltage, V_{IH}
A Port I/Os (V_{CCA} = 1.65V to 1.95V, V_{CCB} = 2.3V to 5.5V)
..... V_{CCI} - 0.1V to V_{CCI}
A Port I/Os (V_{CCA} = 2.3V to 5.5V, V_{CCB} = 2.3V to 5.5V)
..... V_{CCI} - 0.3V to V_{CCI}
B Port I/Os (V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V)
..... V_{CCI} - 0.3V to V_{CCI}
OE Input (V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V)
..... V_{CCA} × 0.8V to 5.5V
Low-Level Input Voltage, V_{IL}
A Port I/Os (V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V)
..... 0V to 0.1V
B Port I/Os (V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V)
..... 0V to 0.1V
OE Input (V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V)
..... 0V to V_{CCA} × 0.2V
Operating Temperature Range ..... -40℃ to +85℃

NOTES:
3. V_{CCI} is the V_{CC} associated with the input ports.
4. V_{CCO} is the V_{CC} associated with the output ports.
5. V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 5.5V.

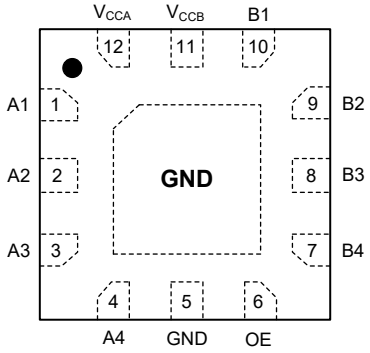
PIN CONFIGURATIONS

(TOP VIEW)



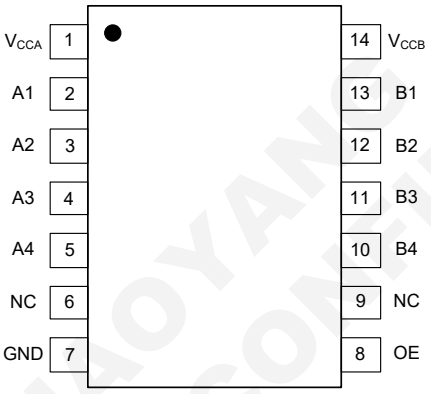
UTQFN-1.8×1.8-12L

(TOP VIEW)



TQFN-2×2-12L

(TOP VIEW)



SOIC-14

PIN DESCRIPTION

PIN			NAME	TYPE	FUNCTION
TQFN-2×2-12L	UTQFN-1.8×1.8-12L	SOIC-14			
1	3	2	A1	I/O	Input/Output A1. Referenced to V_{CCA}.
2	4	3	A2	I/O	Input/Output A2. Referenced to V_{CCA}.
3	5	4	A3	I/O	Input/Output A3. Referenced to V_{CCA}.
4	6	5	A4	I/O	Input/Output A4. Referenced to V_{CCA}.
–	–	6, 9	NC	–	No Connection. Not internally connected.
5	7	7	GND	S	Ground
6	8	8	OE	I	3-State Output-Mode Enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
7	9	10	B4	I/O	Input/Output B4. Referenced to V_{CCB}.
8	10	11	B3	I/O	Input/Output B3. Referenced to V_{CCB}.
9	11	12	B2	I/O	Input/Output B2. Referenced to V_{CCB}.
10	12	13	B1	I/O	Input/Output B1. Referenced to V_{CCB}.
11	1	14	V_{CCB}	S	B Ports Supply Voltage. 2.3V ≤ V_{CCB} ≤ 5.5V.
12	2	1	V_{CCA}	S	A Ports Supply Voltage. 1.65V ≤ V_{CCA} ≤ 5.5V and V_{CCA} ≤ V_{CCB}.
Exposed Pad	–	–	GND	–	Exposed pad should be soldered to PCB board and connected to GND or left floating.

ELECTRICAL CHARACTERISTICS

(V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
A Ports High Level Output Voltage (V_{OHA})		I_{OH} = -20μA, V_{IB} ≥ V_{CCB} - 0.4V			V_{CCA} × 0.8		V
A Ports Low Level Output Voltage (V_{OLA})		I_{OL} = 1mA, V_{IB} ≤ 0.15V			0.2		
B Ports High Level Output Voltage (V_{OHB})		I_{OH} = -20μA, V_{IA} ≥ V_{CCA} - 0.4V			V_{CCB} × 0.8		
B Ports Low Level Output Voltage (V_{OLB})		I_{OL} = 1mA, V_{IA} ≤ 0.15V			0.2		
Input Leakage Current (I_I)	OE				0.5		μA
Power Off Leakage Current (I_{OFF})	A Ports	V_{CCA} = 0V, V_{CCB} = 0V to 5.5V			0.1		μA
	B Ports	V_{CCA} = 0V to 5.5V, V_{CCB} = 0V			0.1		
3-State Output Leakage (I_{OZ})	A or B Ports	OE = 0V			0.1		μA
Quiescent Supply Current (I_{CCA})		V_I = V_O = OPEN, I_O = 0	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		0.1		μA
			V_{CCA} = 5.5V, V_{CCB} = 0V		0.1		
			V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
Quiescent Supply Current (I_{CCB})		V_I = V_O = OPEN, I_O = 0	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		7		μA
			V_{CCA} = 5.5V, V_{CCB} = 0V		0.1		
			V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
Quiescent Supply Current (I_{CCA} + I_{CCB})		V_I = V_O = OPEN, I_O = 0	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		7.1		μA
Quiescent Supply Current (I_{CCZA})		V_I = V_{CCI} or 0V, I_O = 0, OE = 0V	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		0.1		μA
			V_{CCA} = 5.5V, V_{CCB} = 0V		0.1		
			V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
Quiescent Supply Current (I_{CCZB})		V_I = V_{CCI} or 0V, I_O = 0, OE = 0V	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		0.1		μA
			V_{CCA} = 5.5V, V_{CCB} = 0V		0.1		
			V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
OE Input Capacitance (C_I)		V_{CCA} = 3.3V, V_{CCB} = 3.3V			6.4		pF
Input/Output Capacitance A Ports (C_{IO})		V_{CCA} = 3.3V, V_{CCB} = 3.3V			6.3		pF
Input/Output Capacitance B Ports (C_{IO})					6.4		

TIMING REQUIREMENTS

PARAMETER			V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
			TYP	TYP	TYP	
(T_A = +25℃, V_{CCA} = 1.8V, unless otherwise noted.)						
Data Rate	Push-Pull Driving		24	24	24	Mbps
	Open-Drain Driving		2	2	2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs	41	41	41	ns
	Open-Drain Driving		500	500	500	
(T_A = +25℃, V_{CCA} = 2.5V, unless otherwise noted.)						
Data Rate	Push-Pull Driving		24	24	24	Mbps
	Open-Drain Driving		2	2	2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs	41	41	41	ns
	Open-Drain Driving		500	500	500	
(T_A = +25℃, V_{CCA} = 3.3V, unless otherwise noted.)						
Data Rate	Push-Pull Driving			24	24	Mbps
	Open-Drain Driving			2	2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs		41	41	ns
	Open-Drain Driving			500	500	
(T_A = +25℃, V_{CCA} = 5V, unless otherwise noted.)						
Data Rate	Push-Pull Driving				24	Mbps
	Open-Drain Driving				2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs			41	ns
	Open-Drain Driving				500	

SWITCHING CHARACTERISTICS

(T_A = +25℃, V_{CCA} = 1.8V, unless otherwise noted.)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
				TYP	TYP	TYP	
t_{PHL}	A	B	Push-Pull Driving	3.5	3.5	5.1	ns
			Open-Drain Driving	56.2	27.0	27.9	
t_{PLH}			Push-Pull Driving	5.1	4.5	4.4	
			Open-Drain Driving	143	120	92	
t_{PHL}	B	A	Push-Pull Driving	3.0	2.8	3.4	ns
			Open-Drain Driving	25.6	25.3	25.4	
t_{PLH}			Push-Pull Driving	3.7	3.2	2.6	
			Open-Drain Driving	55	49	48	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		28	25	23	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		674	677	671	
t_{rA}	A Ports Rise Time		Push-Pull Driving	7.2	8.1	9.1	ns
			Open-Drain Driving	12	11	10	
t_{rB}	B Ports Rise Time		Push-Pull Driving	7.2	6.1	5.4	ns
			Open-Drain Driving	99	73	37	
t_{fA}	A Ports Fall Time		Push-Pull Driving	5.7	5.9	6.9	ns
			Open-Drain Driving	3.8	3.6	3.6	
t_{fB}	B Ports Fall Time		Push-Pull Driving	7.9	7.8	8.4	ns
			Open-Drain Driving	3.5	8.4	5.0	
Data Rate			Push-Pull Driving	24	24	24	Mbps
			Open-Drain Driving	2	2	2	

SWITCHING CHARACTERISTICS (continued)

(T_A = +25℃, V_{CCA} = 2.5V, unless otherwise noted.)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
				TYP	TYP	TYP	
t_{PHL}	A	B	Push-Pull Driving	4.5	4.5	5.0	ns
			Open-Drain Driving	26.2	27.1	26.2	
t_{PLH}			Push-Pull Driving	3.8	3.3	3.1	
			Open-Drain Driving	111	96	76	
t_{PHL}	B	A	Push-Pull Driving	4.2	4.0	4.1	ns
			Open-Drain Driving	25.8	25.5	25.6	
t_{PLH}			Push-Pull Driving	3.7	3.5	3.6	
			Open-Drain Driving	53	51	50	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		22	17	16	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		689	688	678	
t_{rA}	A Ports Rise Time		Push-Pull Driving	6.4	6.7	6.9	ns
			Open-Drain Driving	10.5	7.7	7.8	
t_{rB}	B Ports Rise Time		Push-Pull Driving	6.2	5.4	4.9	ns
			Open-Drain Driving	67	51	30	
t_{fA}	A Ports Fall Time		Push-Pull Driving	8.6	8.2	7.3	ns
			Open-Drain Driving	3.6	3.3	3.1	
t_{fB}	B Ports Fall Time		Push-Pull Driving	8.5	7.7	8.1	ns
			Open-Drain Driving	3.4	3.9	5.4	
Data Rate			Push-Pull Driving	24	24	24	Mbps
			Open-Drain Driving	2	2	2	

SWITCHING CHARACTERISTICS (continued)

(T_A = +25℃, V_{CCA} = 3.3V, unless otherwise noted.)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
				TYP	TYP	
t_{PHL}	A	B	Push-Pull Driving	4.4	5.0	ns
			Open-Drain Driving	25.5	27.5	
t_{PLH}			Push-Pull Driving	3.5	2.7	
			Open-Drain Driving	52	51	
t_{PHL}	B	A	Push-Pull Driving	4.1	4.4	ns
			Open-Drain Driving	25.8	54.3	
t_{PLH}			Push-Pull Driving	3.1	2.8	
			Open-Drain Driving	50	49	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		16	14	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		699	678	
t_{rA}	A Ports Rise Time		Push-Pull Driving	5.2	6.2	ns
			Open-Drain Driving	6	6	
t_{rB}	B Ports Rise Time		Push-Pull Driving	5.3	4.7	ns
			Open-Drain Driving	8	7	
t_{fA}	A Ports Fall Time		Push-Pull Driving	7.3	7.6	ns
			Open-Drain Driving	3.1	3.0	
t_{fB}	B Ports Fall Time		Push-Pull Driving	7.7	7.3	ns
			Open-Drain Driving	3.8	4.6	
Data Rate			Push-Pull Driving	24	24	Mbps
			Open-Drain Driving	2	2	

SWITCHING CHARACTERISTICS (continued)

(T_A = +25℃, V_{CCA} = 5V, unless otherwise noted.)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 5V	UNITS
				TYP	
t_{PHL}	A	B	Push-Pull Driving	5.3	ns
			Open-Drain Driving	27.4	
t_{PLH}			Push-Pull Driving	2.4	
			Open-Drain Driving	51	
t_{PHL}	B	A	Push-Pull Driving	5.0	ns
			Open-Drain Driving	26.3	
t_{PLH}			Push-Pull Driving	2.2	
			Open-Drain Driving	49	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		23	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		665	
t_{rA}	A Ports Rise Time		Push-Pull Driving	5.3	ns
			Open-Drain Driving	5	
t_{rB}	B Ports Rise Time		Push-Pull Driving	4.9	ns
			Open-Drain Driving	7	
t_{fA}	A Ports Fall Time		Push-Pull Driving	8.5	ns
			Open-Drain Driving	2.8	
t_{fB}	B Ports Fall Time		Push-Pull Driving	7.7	ns
			Open-Drain Driving	4.2	
Data Rate			Push-Pull Driving	24	Mbps
			Open-Drain Driving	2	

FUNCTIONAL BLOCK DIAGRAM

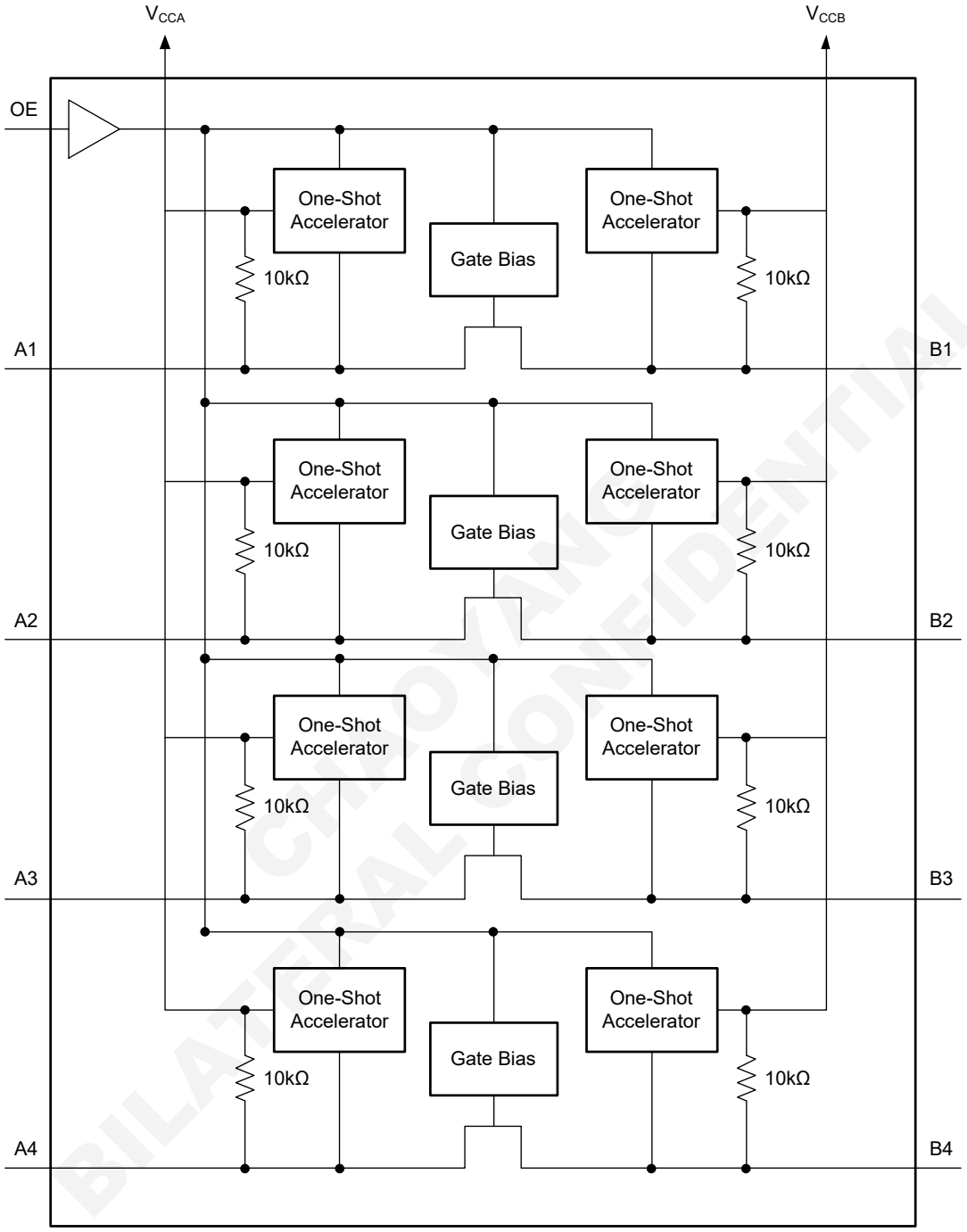
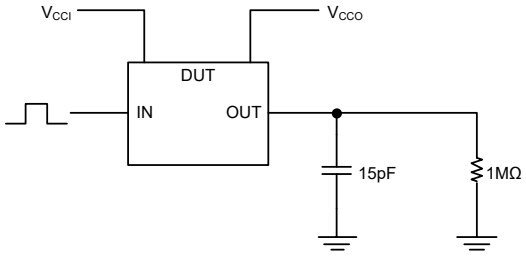
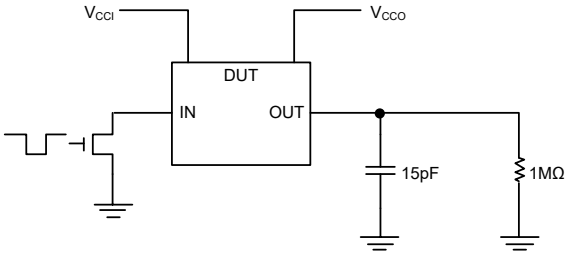


Figure 2. Block Diagram

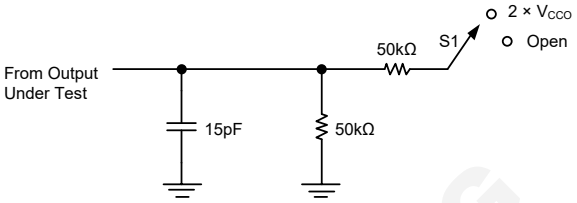
PARAMETER MEASUREMENT INFORMATION



Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using A Push-Pull Driver

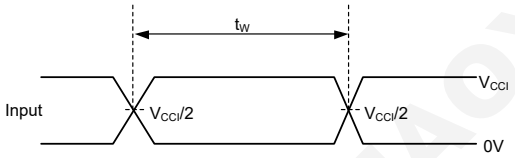


Data Rate (10pF), Pulse Duration (10pF), Propagation Delay, Output Rise-Time and Fall-Time Measurement Using An Open-Drain Driver

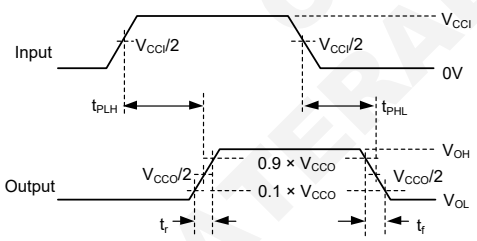


Load Circuit for Enable/Disable Time Measurement

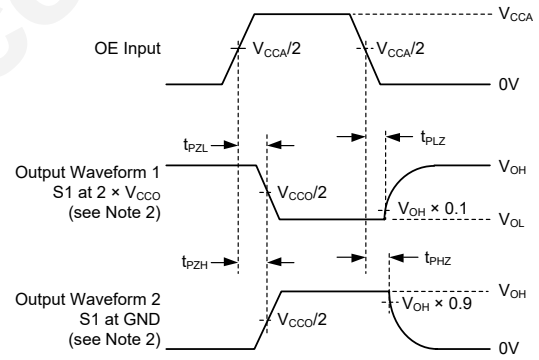
TEST	S1
t_{PZL}/t_{PLZ} (t_{DIS})	2 × V_{CCO}
t_{PHZ}/t_{PZH} (t_{EN})	Open



Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Figure 3. Load Circuits and Voltage Waveforms

NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal such that the output is high, except when OE is high. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, dv/dt ≥ 1V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{DIS}.
6. t_{PZL} and t_{PZH} are the same as t_{EN}.
7. t_{PLH} and t_{PHL} are the same as t_{PD}.
8. V_{CCI} is the V_{CC} associated with the input ports.
9. V_{CCO} is the V_{CC} associated with the output ports.

DETAILED DESCRIPTION

Overview

The SGM4574 is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A ports are able to accept I/O voltages ranging from 1.65V to 5.5V, while the B ports can accept I/O voltages from 2.3V to 5.5V. The device is a pass gate architecture with edge rate accelerators (one-shots) to improve the overall data rate. 10kΩ pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

Feature Description

Architecture

The SGM4574 architecture (see Figure 4) does not require a direction-control signal in order to control the direction of data flow from A to B or from B to A.

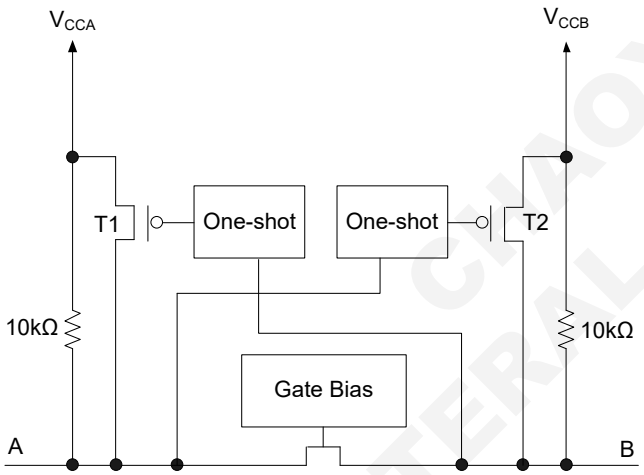


Figure 4. Architecture of a SGM4574 Cell

Each A port I/O has an internal 10kΩ pull-up resistor to V_{CCA}, and each B port I/O has an internal 10kΩ pull-up resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T2) for a short duration which speeds up the low-to-high transition.

Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the SGM4574. Similarly, the t_{PHL} and data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and data rates in the datasheet assume that the output impedance of the external driver is less than 50Ω.

Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

Enable and Disable

The SGM4574 has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{DIS}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{EN}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

Pull-Up and Pull-Down Resistors on I/O Lines

Each A port I/O has an internal 10kΩ pull-up resistor to V_{CCA}, and each B port I/O has an internal 10kΩ pull-up resistor to V_{CCB}. If a smaller value of pull-up resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10kΩ resistors).

Device Functional Modes

The SGM4574 has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

APPLICATION INFORMATION

The SGM4574 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SGM4574 is ideal for use in applications where an open-drain driver is connected to the data I/Os. The SGM4574 can also be used in applications where a push-pull driver is connected to the data I/Os, but the SGM4574 might be a better option for such push-pull applications.

Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	1.65V to 5.5V
Output Voltage Range	2.3V to 5.5V

Detailed Design Procedure

To begin the design process, determine the following:

• Input voltage range

Use the supply voltage of the device that is driving the SGM4574 to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

• Output voltage range

Use the supply voltage of the device that the SGM4574 is driving to determine the output voltage range.

The SGM4574 has 10kΩ internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.

• An external pull-down resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a result of an external pull-down resistor.

$$V_{OH} = V_{CCX} \times R_{PD}/(R_{PD} + 10k\Omega) \quad (1)$$

where,

V_{CCX} is the supply voltage on either V_{CCA} or V_{CCB}.

R_{PD} is the value of the external pull down resistor.

Power Supply Recommendations

The SGM4574 uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 2.3V to 5.5V and V_{CCA} accepts any supply voltage from 1.65V to 5.5V as long as V_S is less than or equal to V_{CCB}. The A ports and B ports are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

The SGM4574 does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \leq V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull-down resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pull-down resistor to ground is determined by the current-sourcing capability of the driver.

Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

• Bypass capacitors should be used on power supplies.

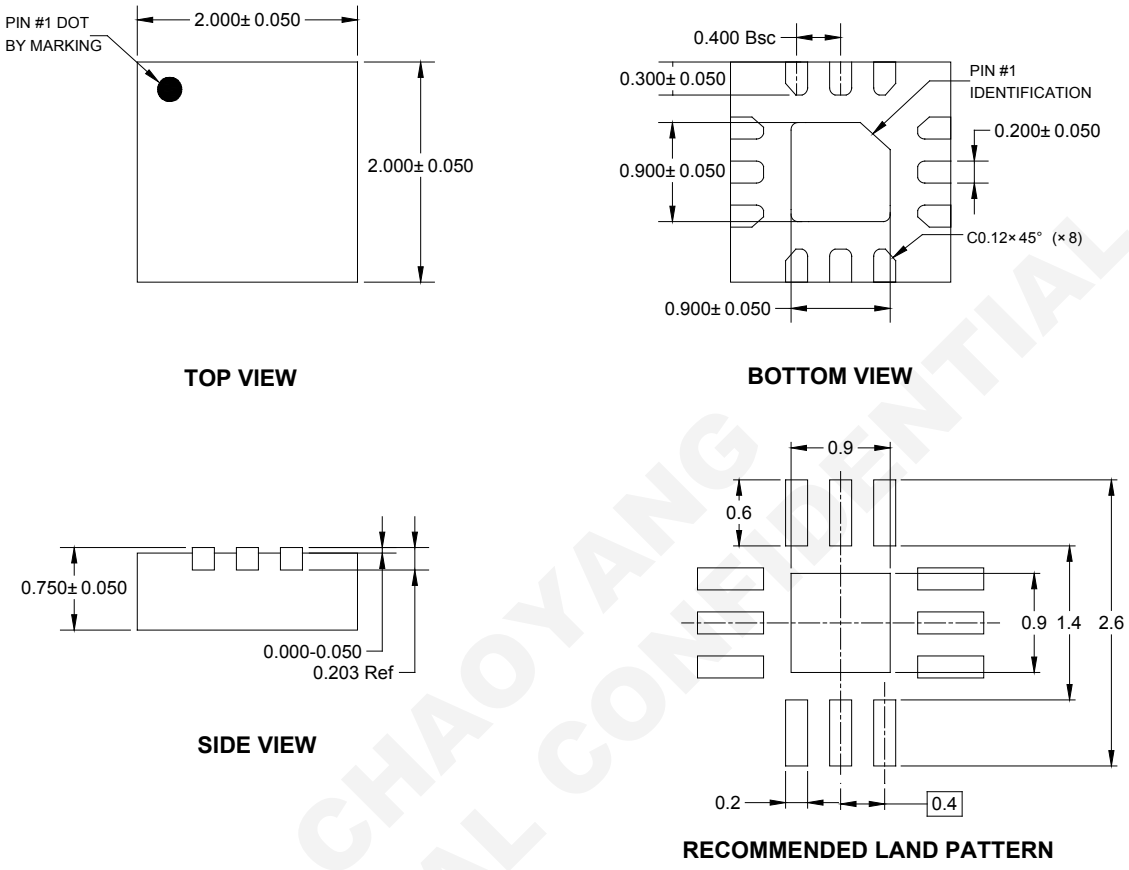
• Short trace lengths should be used to avoid excessive loading.

• PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 30ns, ensuring that any reflection encounters low impedance at the source driver.

• Placing pads on the signal paths for loading capacitors or pull-up resistors to help adjust rise and fall times of signals depending on the system requirements.

PACKAGE OUTLINE DIMENSIONS

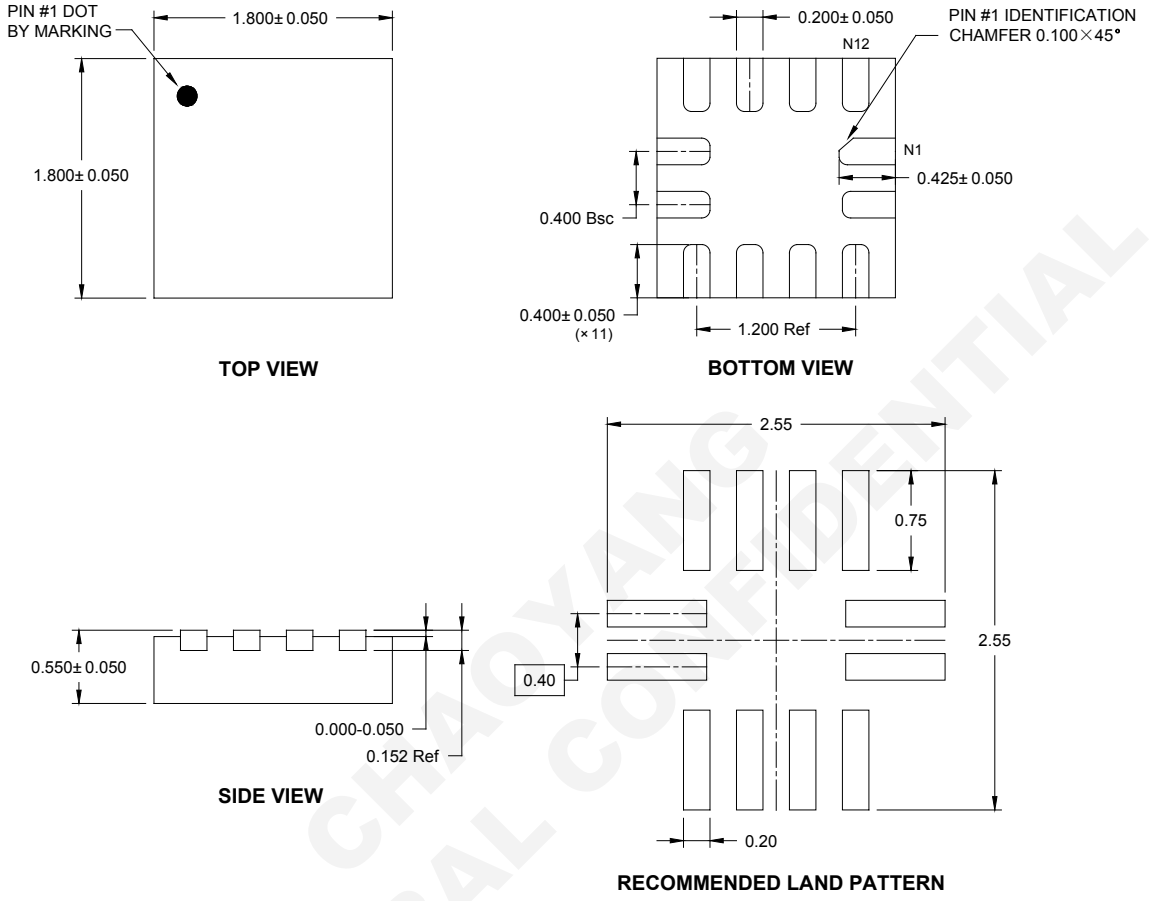
TQFN-2×2-12L



NOTE: All linear dimensions are in millimeters.

PACKAGE OUTLINE DIMENSIONS

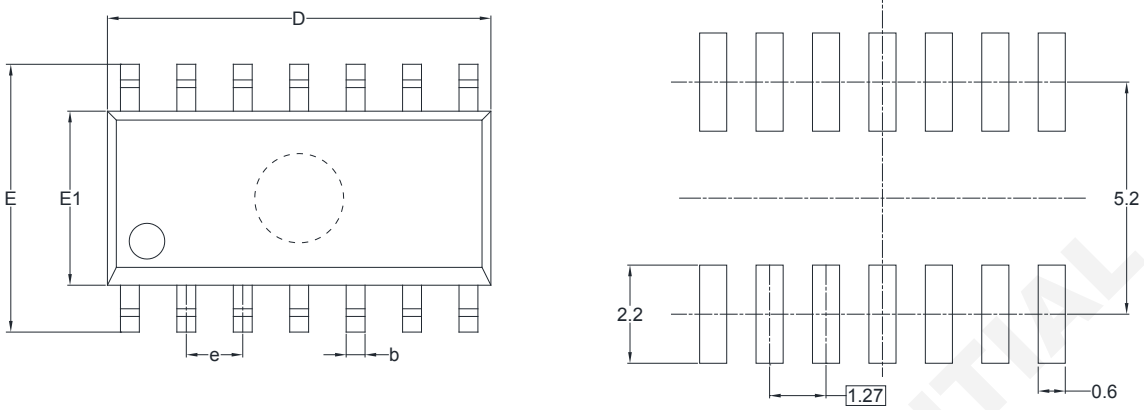
UTQFN-1.8×1.8-12L



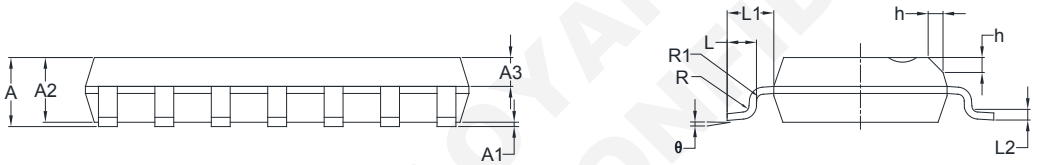
NOTE: All linear dimensions are in millimeters.

PACKAGE OUTLINE DIMENSIONS

SOIC-14



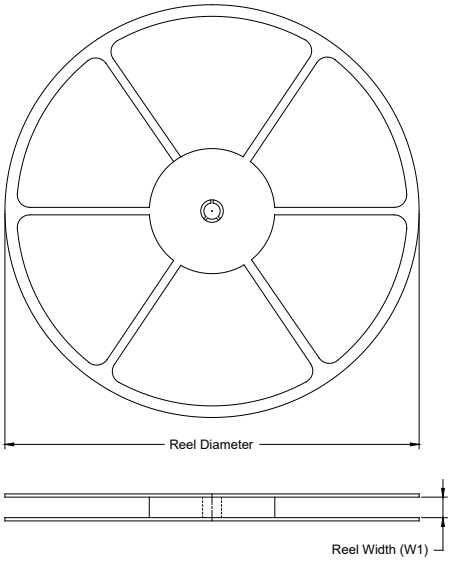
RECOMMENDED LAND PATTERN (Unit: mm)



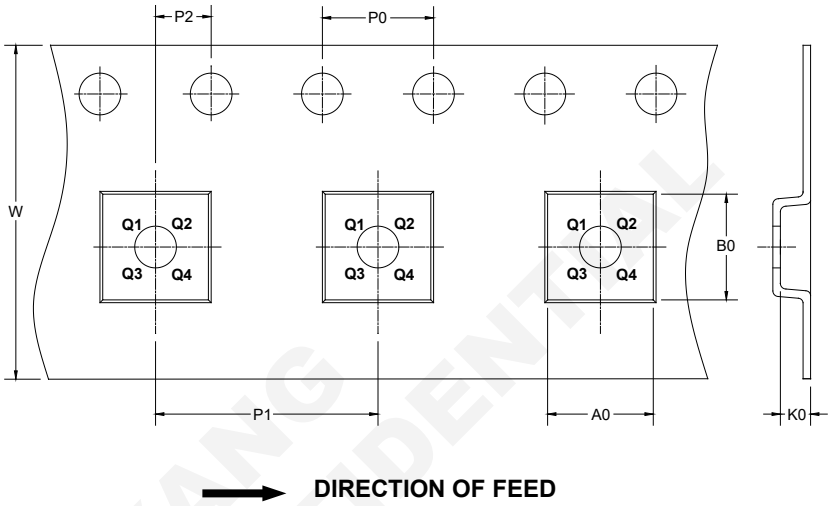
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
A3	0.55	0.75	0.022	0.030
b	0.36	0.49	0.014	0.019
D	8.53	8.73	0.336	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.45	0.80	0.018	0.032
L1	1.04 REF		0.040 REF	
L2	0.25 BSC		0.01 BSC	
R	0.07		0.003	
R1	0.07		0.003	
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



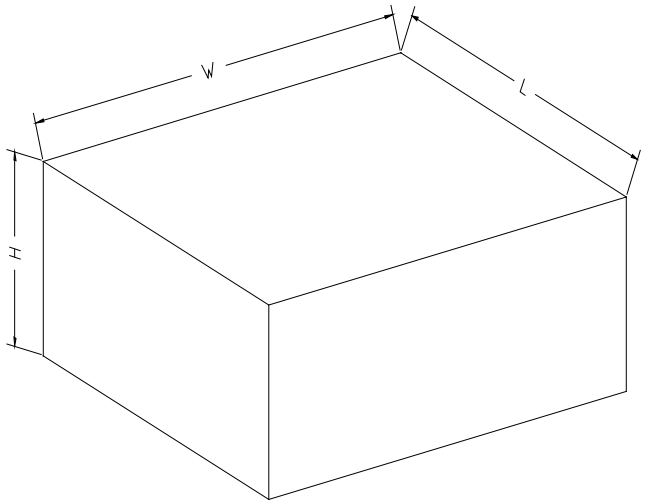
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2-12L	7″	9.5	2.30	2.30	0.90	4.0	4.0	2.0	8.0	Q2
UTQFN-1.8×1.8-12L	7″	9.0	2.10	2.10	0.80	4.0	4.0	2.0	8.0	Q2
SOIC-14	13″	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002