SGM41528
I²C Controlled 2A, 2-Cell Battery Charger with Boost Mode for USB Input

FEATURES

- High Efficiency 2A, 1.5MHz Switch-Mode Boost Charger
  - 92.5% Charge Efficiency at 1A from 7.6V Battery Input
  - Optimized for USB Input and 2-Cell Li-Ion Output
  - Selectable PFM Mode for Light Load Operation with Out-of-Audio Option
- USB On-The-Go (OTG) Support (Buck Mode) with Adjustable Output from 4.5V to 5.5V
  - Buck Converter with up to 2A Output
  - Buck Efficiency of 94.5% at 5V, 1A Output
  - Accurate Constant Current (CC) Limit
  - Output Short Circuit Protection
  - Selectable PFM Mode for Light Load Operation with Out-of-Audio Option
- Single Input for USB Input Adapters
  - 3.9V to 6.2V Operating Input Voltage Range
  - 20V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (IINDPM, 500mA to 3.3A with 100mA Resolution) to Support USB 2.0, USB 3.0 Standard Adapters
  - Maximum Power Tracking by Input Voltage Limit up to 5.5V (VINDPM)
  - Auto-Detect USB SDP, CDP, DCP, and Non-Standard Adapters
- Input Current Optimizer (ICO) to Maximize Input Power without Overloading Adapters
- High Battery Discharge Efficiency with 13mΩ Switch
- Integrated ADC for System Monitoring (BUS Voltage and Current, BAT Voltage, Charge Current, SYS Voltage, and NTC and Die Temperature)
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with No or Highly Depleted Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Flexible Autonomous and I²C Operation Modes for Optimal System Performance
- Fully Integrated All MOSFETs, Current Sense and Loop Compensation
- High Accuracy
  - ±0.4% Charge Voltage Regulation
  - ±7.5% Charge Current Regulation
  - ±7.5% Input Current Regulation
- Safety
  - Battery Temperature Sensing (Charge/OTG Buck Modes)
  - Thermal Regulation and Thermal Shutdown

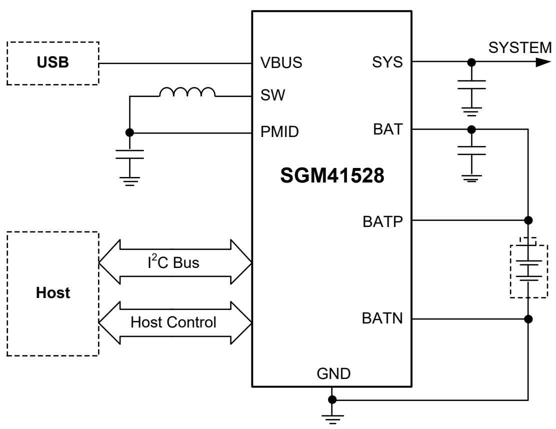
APPLICATIONS

Wireless Speaker
Digital Camera (DSC, DVC)
Mobile Printer
Tablet
Electronic Point of Sales (ePOS)
Portable Electronic Devices

GENERAL DESCRIPTION

The SGM41528 is a battery charger and system power path management device with integrated converter and power switches for use with 2-cell Li-Ion or Li-polymer batteries. I²C programming makes it a very flexible powering and charger design solution.

SIMPLIFIED SCHEMATIC

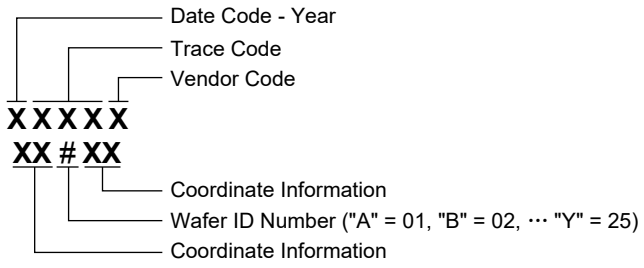


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41528	WLCSP-2.1×2.1-25B	-40℃ to +85℃	SGM41528YG/TR	41528 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VBUS (Converter Not Switching) ..... -0.3V to 20V
- PMID (Converter Not Switching) ..... -0.3V to 8.5V
- BAT, SYS (Converter Not Switching) ..... -0.3V to 12V
- SW ..... -0.6V (1) to 13V
- BTST ..... -0.3V to 19V
- BATP ..... -0.3V to 12V
- BATN, REGN, SDA, SCL, nINT, nCE, TS, D+, D-, nPG ..... -0.3V to 6V
- ILIM ..... -0.3V to 5V
- BTST to SW ..... -0.3V to 6V
- SYS to BAT ..... -0.3V to 8.5V

Output Sink Current
- nINT, nPG 6mA

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} ..... 3.9V to 6.2V
Average Input Current (VBUS), I_{VBUS} ..... 3.3A (MAX)
Average Charge Current (BAT), I_{BAT} ..... 2.2A (MAX)
Battery Voltage (BATP - BATN), V_{BAT} ..... 9.2V (2) (MAX)
RMS Discharging Current with Internal MOSFET, I_{BAT_RMS} ..... 4A (MAX)
Peak Discharging Current with Internal MOSFET, I_{BAT_PK} ..... 8A (MAX)
Operating Temperature Range ..... -40℃ to +85℃

NOTES:
1. -2V for 50ns.
2. The inherent switching noise voltage spikes should not exceed the absolute maximum rating on SW pins. A tight layout minimizes switching noise.

OVERSTRESS CAUTION

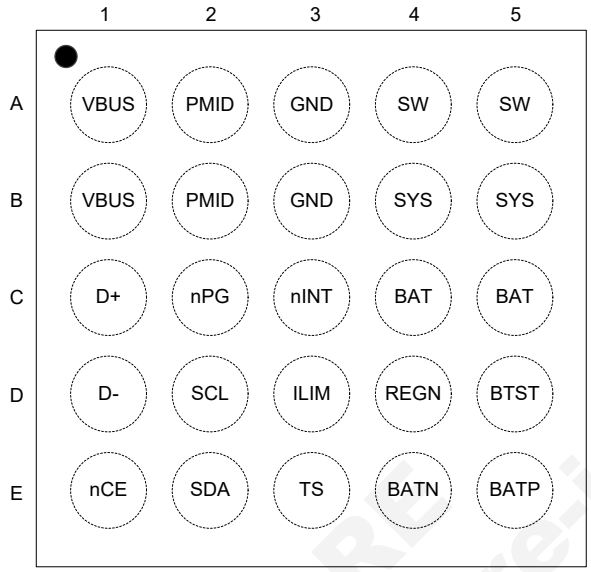
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.1×2.1-25B

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
A1, B1	VBUS	P	Charger Input (V_{IN}). VBUS is connected to the external DC supply. Place a 1μF ceramic capacitor from VBUS pin to GND close to the device.
A2, B2	PMID	P	PMID Pin. Blocking MOSFET connection. Given the total input capacitance. Connect a 10μF ceramic capacitor from PMID pin to GND.
A3, B3	GND	-	Ground Pin of the Device.
A4, A5	SW	P	Switching Node Output. Connect SW pin to the output inductor.
B4, B5	SYS	P	System Connection. The internal BATFET is connected between SYS pin and BAT pin. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect a 44μF ceramic capacitor between SYS pin and GND close to the device.
C1	D+	AIO	Positive Line of the USB Data Line Pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
C2	nPG	DO	Open-Drain Active Low Input Power Good Indicator. Use a 10kΩ pull-up to the logic high rail. A low state indicates a good input if the input voltage is within V_{VBUS_OP}, and can provide more than I_{BAD_SRC}.
C3	nINT	DO	Open-Drain Active Low Interrupt Output. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform host about a new charger status update or a fault.
C4, C5	BAT	P	Battery Positive Terminal Pin. Use a 10μF capacitor between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
D1	D-	AIO	Negative Line of the USB Data Line Pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
D2	SCL	DI	I²C Clock Signal. Use a 10kΩ pull-up to the logic high rail.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE (1)	FUNCTION
D3	ILIM	AI	Input Current Limit. ILIM pin sets the maximum input current and can be used to monitor input current. IINDPM loop regulates ILIM pin voltage at 0.8V. When ILIM pin is less than 0.8V, the input current limit can be calculated by $I_{IN} = K_{ILIM} \times V_{ILIM}/(R_{ILIM} \times 0.8V)$. A resistor connected from ILIM pin to ground sets the current limit as $I_{INMAX} = K_{ILIM}/R_{ILIM}$. The actual input current limit is the lower limit set by ILIM pin (when EN_ILIM bit is high) or IINDPM[4:0] register bits. Input current limit less than 500mA is not supported on ILIM pin. The ILIM pin function can be disabled when EN_ILIM bit is 0.
D4	REGN	P	Gate Drive Supply. Bias supply for internal MOSFETs driver and IC. Connect a 4.7μF ceramic capacitor from REGN pin to GND. The capacitor should be placed close to the IC.
D5	BTST	P	PWM High-side Driver Supply. It is internally connected to the bootstrap diode cathode. Use a 47nF bootstrap capacitor from SW pin to BTST pin.
E1	nCE	DI	Charge Enable Input Pin (Active Low). Battery charging is enabled when EN_CHG bit is 1 and nCE pin is pulled low. nCE pin must be pulled high or low, do not leave floating.
E2	SDA	DIO	I²C Data Signal. Use a 10kΩ pull-up to the logic high rail.
E3	TS	AI	Temperature Qualification Voltage Input. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN and GND. Charge suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor.
E4	BATN	AI	Negative Battery Sense Terminal. Kelvin connects as close as possible to negative battery terminal.
E5	BATP	AI	Positive Battery Sense Terminal. Kelvin connects as close as possible to positive battery terminal.

NOTE:

1. AI = Analog Input, AO = Analog Output, AIO = Analog Input and Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input and Output, P = Power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Currents							
Battery Discharge Current (BATP, BAT, SYS)	I_{BAT}	V_{BAT} = 9V, no VBUS, SCL, SDA = 0V or 1.8V, ADC disabled	T_J = +25℃		12		μA
			T_J < +85℃		12		
Input Supply Current (VBUS) in HIZ	I_{VBUS_HIZ}	V_{VBUS} = 5V, HIZ mode, no battery, ADC disabled	T_J = +25℃		15		μA
			T_J < +85℃		15		
Input Supply Current (VBUS)	I_{VBUS}	V_{VBUS} = 5V, V_{BAT} = 7.6V, converter not switching			1.5		mA
		V_{VBUS} = 5V, V_{BAT} = 7.6V, converter switching, I_{SYS} = 0A			3		
Battery Discharge Current in OTG Mode	I_{BAT_OTG}	V_{BAT} = 8.4V, OTG buck mode, I_{VBUS} = 0A, converter switching			3		mA
VBUS Pin and BAT Pin Power-Up							
VBUS Operating Range	V_{VBUS_OP}			3.9		6.2	V
VBUS UVLO to Have Active I²C (with No Battery)	V_{VBUS_UVLOZ}	V_{VBUS} rising			3.2		V
V_{VBUS} Minimum (as One of the Conditions) to Turn on REGN	$V_{VBUS\_PRESENT}$	V_{VBUS} rising			3.6		V
VBUS Over-Voltage Rising Threshold	V_{VBUS_OV}	V_{VBUS} rising			6.4		V
VBUS Over-Voltage Falling Threshold		V_{VBUS} falling			6.15		V
BAT Voltage to Have Active I²C (No Source on VBUS)	V_{BAT_UVLOZ}	V_{BAT} rising			3.53		V
Bad Adapter Detection Threshold	V_{BAD_SRC}				3.6		V
Bad Adapter Detection Current Source	I_{BAD_SRC}				15		mA
Power Path Management							
System Regulation Voltage	V_{SYS}	I_{SYS} = 0A, V_{BAT} = 8.8V, V_{BAT} > SYS_MIN[3:0], charge disabled (EN_CHG = 0), offset above V_{BAT}			100		mV
		I_{SYS} = 0A, V_{BAT} < SYS_MIN[3:0], charge disabled (EN_CHG = 0), offset above V_{SYS_MIN}			300		
Minimum DC System Voltage Output	V_{SYS_MIN}	V_{BAT} < SYS_MIN[3:0] = 1010, charge disabled (EN_CHG = 0)			7.3		V
Blocking MOSFET On-Resistance between VBUS and PMID - Q1	R_{ON_QBLK}	T_J = +25℃			20		mΩ
		T_J = -40℃ to +85℃			20		
High-side Switching MOSFET On-Resistance between SW and SYS - Q2	R_{ON_QHS}	T_J = +25℃			28		mΩ
		T_J = -40℃ to +85℃			28		
Low-side Switching MOSFET On-Resistance between SW and GND - Q3	R_{ON_QLS}	T_J = +25℃			40		mΩ
		T_J = -40℃ to +85℃			40		

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Charger						
Charge Voltage Program Range	$V_{BAT\_REG\_RANGE}$		6.8		9.2	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$			10		mV
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 8.4V, T_J = -40℃ to +85℃		8.4		V
		V_{BAT_REG} = 8.7V, T_J = -40℃ to +85℃		8.7		
		V_{BAT_REG} = 8.8V, T_J = -40℃ to +85℃		8.8		
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$		0		2200	mA
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$			50		mA
Fast Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	I_{CHG} = 250mA, V_{BAT} = 6.2V or 7.6V, T_J = -20℃ to +85℃		±25		%
		I_{CHG} = 500mA, V_{BAT} = 6.2V or 7.6V, T_J = -20℃ to +85℃		±10		
		I_{CHG} = 1000mA, V_{BAT} = 6.2V or 7.6V, T_J = -20℃ to +85℃		±7.5		
Pre-Charge Current Range	I_{PRECHG_RANGE}		50		800	mA
Typical Pre-Charge Current Step	I_{PRECHG_STEP}			50		mA
Pre-Charge Current Accuracy	I_{PRECHG_ACC}	V_{BAT} = 5.2V, I_{PRECHG} = 200mA, T_J = -20℃ to +85℃		±20		%
Termination Current Range	I_{TERM_RANGE}		50		800	mA
Typical Termination Current Step	I_{TERM_STEP}			50		mA
Termination Current Accuracy	I_{TERM_ACC}	I_{CHG} = 1.5A, I_{TERM} = 50mA, T_J = -40℃ to +85℃		±40		%
		I_{CHG} = 1.5A, I_{TERM} = 150mA, T_J = -40℃ to +85℃		±20		
Battery Short Voltage Rising Threshold to Start Pre-Charging	V_{BAT_SHORT}	V_{BAT} rising		4.4		V
Battery Short Voltage Falling Threshold to Stop Pre-Charging	$V_{BAT\_SHORT\_HYS}$	V_{BAT} falling		4.0		V
Battery Short Voltage Trickle Charging Current	I_{SHORT}	V_{BAT} < 4.4V		70		mA
Battery LOW Rising Threshold to Start Fast-Charging	V_{BAT_LOW}	V_{BAT} rising, V_{BATLOW} = 6V		6		V
Battery LOW Falling Threshold to Stop Fast-Charging		V_{BAT} falling, V_{BATLOW} = 6V		5.6		V
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, VRECHG[1:0] = 01		220		mV
		V_{BAT} falling, VRECHG[1:0] = 10		320		
MOSFET On-Resistance between SYS and BAT (Q4)	R_{ON_QBAT}	T_J = +25℃		13		mΩ
		T_J = -40℃ to +85℃		13		
BATP Input Resistance	R_{BATP}	V_{BAT} = 8V, V_{VBUS} = 5V, EN_HIZ = 1, ADC disabled		8		MΩ
BATN Input Resistance	R_{BATN}	V_{BAT} = 8V, V_{VBUS} = 5V, EN_HIZ = 1, ADC disabled		8		MΩ

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage and Current Regulation (DPM: Dynamic Power Management)						
Input Voltage Regulation Range	V_{INDPM_RANGE}		3.9		5.5	V
Input Voltage Regulation Step	V_{INDPM_STEP}			100		mV
Input Voltage Regulation Limit	V_{INDPM}	V_{INDPM} = 3.9V		3.9		V
		V_{INDPM} = 4.4V		4.4		
Input Current Regulation Range	I_{INDPM_RANGE}		500		3300	mA
Input Current Regulation Step	I_{INDPM_STEP}			100		mA
Input Current Regulation Limit	I_{INDPM_ACC}	I_{INDPM} = 500mA		470		mA
		I_{INDPM} = 900mA		832.5		
		I_{INDPM} = 2500mA		2312.5		
		I_{INDPM} = 3000mA		2775		
Charge Current Setting Ratio	K_{ILIM}	$I_{INMAX} = K_{ILIM}/R_{ILIM}$, input current regulation by ILIM pin = 1.5A		1080		A × Ω
D+/D- Detection						
D+/D- Voltage Source (600mV)	$V_{D+D-\_600MVSRC}$			600		mV
D+ Current Source (10μA)	$I_{D+\_10UASRC}$			12		μA
D+/D- Current Sink (100μA)	$I_{D+D-\_100UASNK}$			130		μA
D+/D- Comparator Threshold for Secondary Detection	V_{D+D-_0P325}			350		mV
D+ Comparator Threshold for Data Contact Detection	V_{D+_0P8}			900		mV
D- Resistor to Ground (19kΩ)	R_{D-_19K}			19.6		kΩ
D+/D- Threshold for Non-Standard Adapter	V_{D+D-_1P2}		1.05		1.35	V
	V_{D+D-_2P0}		1.85		2.15	
	V_{D+D-_2P8}		2.55		2.85	
D+/D- Leakage Current	I_{D+D-_LKG}	HIZ mode		0.1		μA
Battery Over-Voltage Protection						
Battery Over-Voltage Rising Threshold	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{BAT_REG}		104		%
Battery Over-Voltage Falling Threshold		V_{BAT} falling, as percentage of V_{BAT_REG}		102		%
Thermal Regulation and Thermal Shutdown						
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	TREG[1:0] = 11 (120℃)		120		℃
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature increasing		150		℃
Thermal Shutdown Falling Temperature		Temperature decreasing		120		℃
JEITA Thermistor Comparator (Boost Mode)						
T1 (0℃) Threshold	V_{T1}	Charge suspended below this temperature, as percentage of V_{REGN}		73.25		%
	V_{T1_HYS}	Charge re-enabled to I_{CHG}/2 and V_{REG} above this temperature, as percentage of V_{REGN}		1.2		%
T2 (10℃) Threshold	V_{T2}	Charge back to I_{CHG}/2 and V_{REG} below this temperature, as percentage of V_{REGN}		68.25		%
	V_{T2_HYS}	Charge back to I_{CHG} and V_{REG} above this temperature, as percentage of V_{REGN}		1.25		%
T3 (45℃) Threshold	V_{T3}	Charge back to I_{CHG} and 8.1V above this temperature, as percentage of V_{REGN}		44.8		%
	V_{T3_HYS}	Charge back to I_{CHG} and V_{REG} below this temperature, as percentage of V_{REGN}		1		%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
T4 (60℃) Threshold	V_{T4}	Charge suspended above this temperature, as percentage of V_{REGN}		34.45		%
	V_{T4_HYS}	Charge back to I_{CHG} and 8.1V below this temperature, as percentage of V_{REGN}		1.2		%
Cold/Hot Thermistor Comparator (OTG Buck Mode)						
Cold Temperature Threshold 0 (TS Pin Voltage Rising Threshold)	V_{BCOLD0}	As percentage of V_{REGN}, BCOLD = 0 (approx. -10℃ w/103AT)		77		%
Cold Temperature Threshold 0 (TS Pin Voltage Falling Threshold)	V_{BCOLD0_HYS}	As percentage of V_{REGN}		1		%
Cold Temperature Threshold 1 (TS Pin Voltage Rising Threshold)	V_{BCOLD1}	As percentage of V_{REGN}, BCOLD = 1 (approx. -20℃ w/103AT)		80		%
Cold Temperature Threshold 1 (TS Pin Voltage Falling Threshold)	V_{BCOLD1_HYS}	As percentage of V_{REGN}		1		%
Hot Temperature Threshold 0 (TS Pin Voltage Falling Threshold)	V_{BHOT0}	As percentage of V_{REGN}, BHOT[1:0] = 01 (approx. 55℃ w/103AT)		37.75		%
Hot Temperature Threshold 0 (TS Pin Voltage Rising Threshold)	V_{BHOT0_HYS}	As percentage of V_{REGN}		3		%
Hot Temperature Threshold 1 (TS Pin Voltage Falling Threshold)	V_{BHOT1}	As percentage of V_{REGN}, BHOT[1:0] = 00 (approx. 60℃ w/103AT)		34.45		%
Hot Temperature Threshold 1 (TS Pin Voltage Rising Threshold)	V_{BHOT1_HYS}	As percentage of V_{REGN}		3.2		%
Hot Temperature Threshold 2 (TS Pin Voltage Falling Threshold)	V_{BHOT2}	As percentage of V_{REGN}, BHOT[1:0] = 10 (approx. 65℃ w/103AT)		31.35		%
Hot Temperature Threshold 2 (TS Pin Voltage Rising Threshold)	V_{BHOT1_HY2}	As percentage of V_{REGN}		3		%
Boost Mode Converter						
PWM Switching Frequency	f_{SW}	Oscillator frequency		1.5		MHz
OTG Buck Mode Converter						
Battery Voltage Exiting OTG Mode	V_{OTG_BAT}	V_{BAT} falling		6		V
Typical OTG Buck Mode Voltage Regulation Range	V_{OTG_RANGE}		4.5		5.5	V
Typical OTG Buck Mode Voltage Regulation Step	V_{OTG_STEP}			100		mV
OTG Buck Mode Voltage Regulation Accuracy	V_{OTG_ACC}	I_{VBUS} = 0A, OTG_VLIM = 5V		±3		%
Typical OTG Buck Mode Current Regulation Range	I_{OTG_RANGE}		0.5		2	A
Typical OTG Buck Mode Current Regulation Step	I_{OTG_STEP}			100		mA
OTG Buck Mode Current Regulation Accuracy	I_{OTG_ACC}	OTG_ILIM = 1A		±10		%
OTG Buck Mode Over-Voltage Threshold	V_{OTG_OVP}			6		V
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 5V, I_{REGN} = 20mA		4.95		V
REGN LDO Current Limit	I_{REGN}	V_{VBUS} = 5V, V_{REGN} = 3.8V		45		mA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog-to-Digital Converter (ADC)						
Conversion Time, Each Measurement	t_{ADC_CONV}	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		
		ADC_SAMPLE[1:0] = 10		6		
		ADC_SAMPLE[1:0] = 11		3		
Effective Resolution	ADCRES	ADC_SAMPLE[1:0] = 00		15		bits
		ADC_SAMPLE[1:0] = 01		14		
		ADC_SAMPLE[1:0] = 10		13		
		ADC_SAMPLE[1:0] = 11		11		
ADC Measurement Ranges and LSB						
ADC BUS Current Range	$I_{BUS\_ADC\_RANGE}$		0		4	A
ADC BUS Current LSB	$I_{BUS\_ADC\_LSB}$			1		mA
ADC BAT Current Range	$I_{BAT\_ADC\_RANGE}$		0		4	A
ADC BAT Current LSB	$I_{BAT\_ADC\_LSB}$			1		mA
ADC BUS Voltage Range	$V_{BUS\_ADC\_RANGE}$		0		6.5	V
ADC BUS Voltage LSB	$V_{BUS\_ADC\_LSB}$			1		mV
ADC SYS Voltage Range	$V_{SYS\_ADC\_RANGE}$		0		10	V
ADC SYS Voltage LSB	$V_{SYS\_ADC\_LSB}$			1		mV
ADC BAT Voltage Range	$V_{BAT\_ADC\_RANGE}$		0		10	V
ADC BAT Voltage LSB	$V_{BAT\_ADC\_LSB}$			1		mV
ADC TS Voltage Range	$V_{TS\_ADC\_RANGE}$		20		80	%
ADC TS Voltage LSB	$V_{TS\_ADC\_LSB}$			0.098		%
ADC Die Temperature Range	$V_{TDIE\_ADC\_RANGE}$		0		150	℃
ADC Die Temperature LSB	$V_{TDIE\_ADC\_LSB}$			1		℃
I²C Interface Characteristics (SCL, SDA)						
Input High Threshold (SDA and SCL)	V_{IH}	Pull up rail 1.8V	1.3			V
Input Low Threshold	V_{IL}	Pull up rail 1.8V			0.4	V
Output Low Threshold	V_{OL}	Sink current = 5mA		0.2		V
High-Level Leakage Current	I_{BIAS}	Pull up rail 1.8V		0.1		μA
Logic I/O Pin Characteristics (nCE, PSEL)						
Input High Threshold	V_{IH}		1.3			V
Input Low Threshold	V_{IL}				0.4	V
High-Level Leakage Current	I_{IN_BIAS}	Pull up rail 1.8V		0.1		μA
Logic Output Pin Characteristics (nINT, nPG, STAT)						
Output Low Threshold	V_{OL}	Sink current = 5mA		0.2		V
High-Level Leakage Current	I_{OUT_BIAS}	Pull up rail 1.8V		0.1		μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} Power-Up						
VBUS OVP Reaction Time	t_{VBUS_OV}	V_{VBUS} rising above V_{VBUS_OV} threshold to turn off the converter		200		ns
Wait Window for Bad Adapter Detection	t_{BADSRC}			30		ms
Battery Charger						
Deglitch Time for Charge Termination	t_{TERM_DGL}	Charge current falling below I_{TERM}		250		ms
Deglitch Time for Recharge Threshold	t_{RECGH_DGL}	BAT voltage falling below V_{RECHG} = 100mV		250		ms
Deglitch Time for Battery Over-Voltage to Disable Charge	$t_{BAT\_OVP\_DGL}$			1		μs
Typical Top-Off Timer Range	t_{TOP_OFF}	TOPOFF_TIMER[1:0] = 10 (30min)		30		min
Charge Safety Timer Range	t_{SAFETY}	CHG_TIMER[1:0] = 10 (16.5 hours)		16.5		hr
Digital Clock and Watchdog Timer						
Digital Clock Frequency in Low Power	f_{LPDIG}	REGN LDO disabled		30		kHz
Digital Clock Frequency	f_{DIG}	REGN LDO enabled		1.5		MHz
Watchdog Reset Time	t_{WDT}	WATCHDOG[1:0] = 11 (160s), REGN LDO disabled		160		s
		WATCHDOG[1:0] = 11 (160s), REGN LDO enabled		160		
I²C Interface						
SCL Clock Frequency	f_{SCL}				1	MHz

TYPICAL APPLICATION CIRCUIT

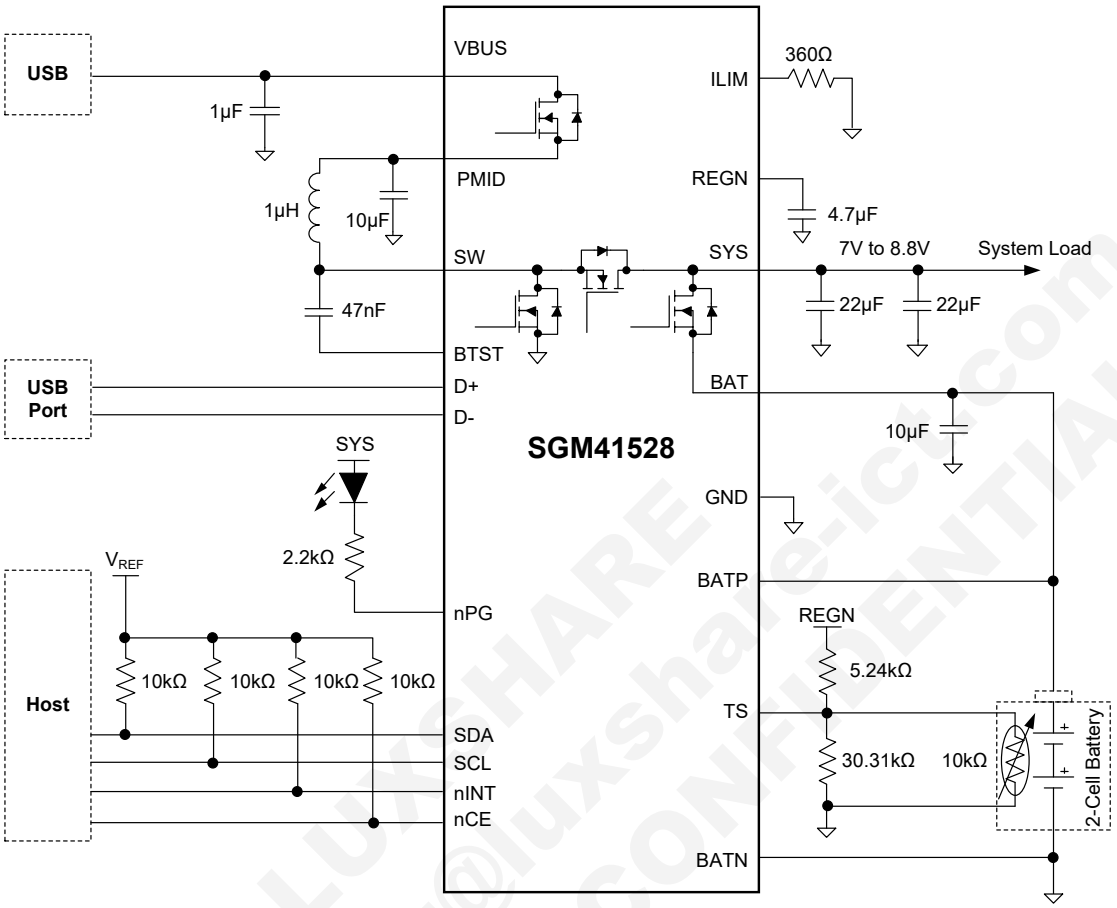


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

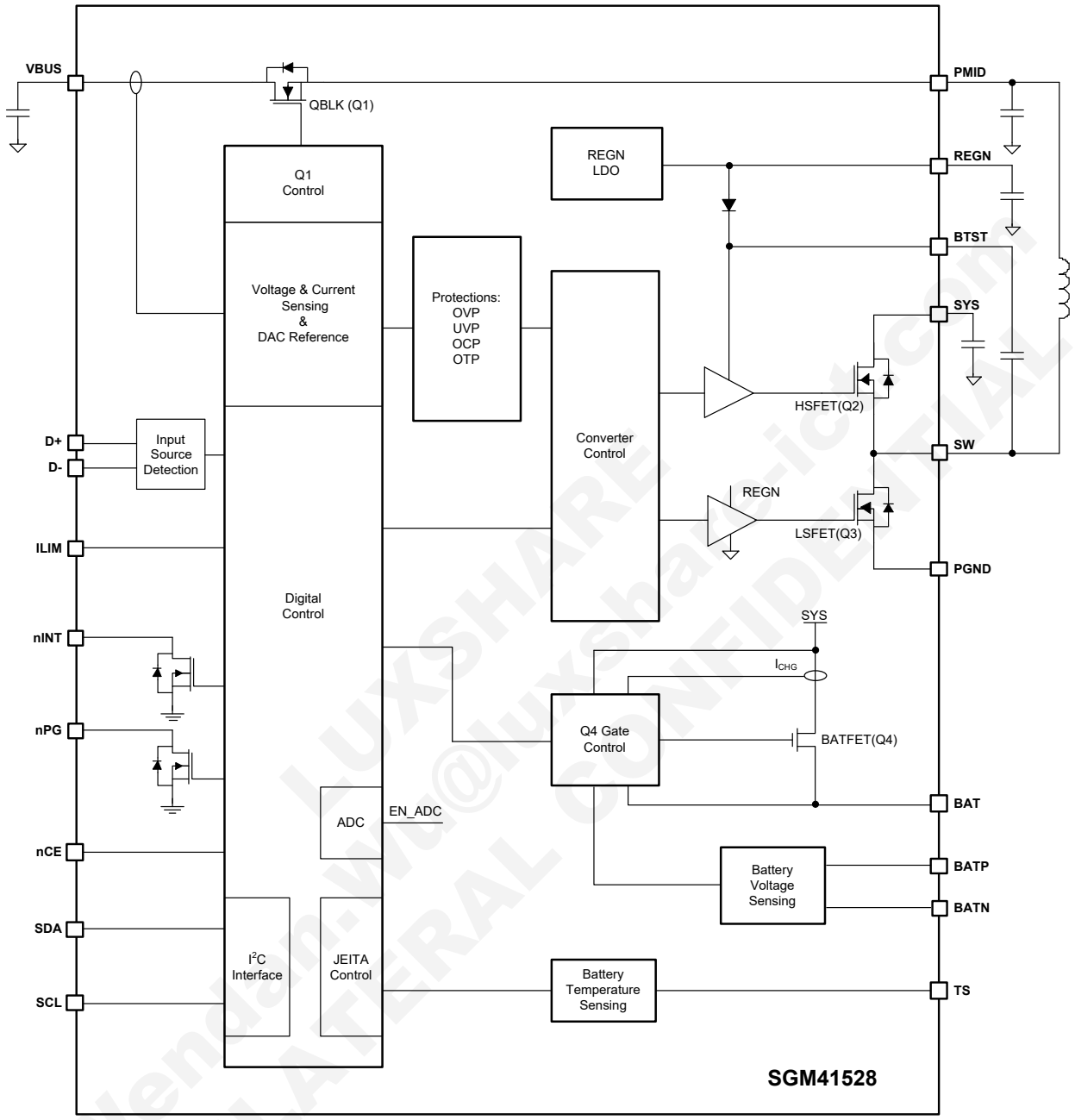


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The device is a highly integrated 2A switch-mode battery charger for 2-cell Li-Ion or Li-polymer batteries. The device includes four main power switches: input blocking FET (Q1, QBLK), high-side switching FET (Q2, QHS), low-side switching FET (Q3, QLS), and battery FET (Q4, QBAT). The device also integrates the bootstrap diode for high-side gate drive.

Power-On Reset (POR)

The internal circuit of the device is powered from the greater voltage between V_{VBUS} and V_{BAT}. When the voltage of the selected source goes above its UVLO level (V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}), a POR happens and activates the BATFET driver. Upon activation, the I^2C interface will also be ready for communication and all registers reset to their default values.

Power-Up from Battery Only (No Input Source)

When only the battery is presented as a source and its voltage is above UVLO threshold (V_{BAT_UVLOZ}), the BATFET turns on and connects the battery to the system. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time. The discharge current through BATFET is continuously monitored.

Power-Up Process from the Input Source

Upon connection of an input source (VBUS), the input source from VBUS pin is checked to turn on the internal REGN LDO regulator and the bias circuits (no matter if the battery is present or not). The input current limit is determined and set before the boost converter is started. The sequences of actions when VBUS as input source is powered up are:

1. Poor source detection (qualification).
2. Input source type detection. (Based on D+/D- input. It is used to set the default input current limit (IINDPM[4:0]).)
3. REGN LDO power-up.
4. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

Poor Source Detection (Qualification)

When valid VBUS is plugged in, the input source (adaptor) is checked for its type and current capacity. To start the boost converter, the input (VBUS) must meet the following conditions:

1. V_{VBUS} < V_{VBUS_OVP}.
2. V_{VBUS} > V_{BAD_SRC} during t_{BADSRC} test period (30ms TYP) in which the I_{BAD_SRC} (15mA TYP) current is pulled from VBUS.

If V_{VBUS_OVP} is detected (condition 1 above), the device automatically retries detection once the over-voltage fault goes away. If a poor source is detected (condition 2 above), the device repeats poor source qualification routine every 2 seconds. After 7 consecutive failures, the device sets EN_HIZ = 1, and goes to HIZ mode. The battery powers up the system when the device is in HIZ. Adapter re-plugin and/or EN_HIZ bit toggle is required to restart device operation. The EN_HIZ bit is cleared automatically when the adapter is plugged in.

DETAILED DESCRIPTION (continued)

Input Source Type Detection

The input source detection will run through the D+/D- lines after the adaptor pass the poor source qualification when AUTO_INDET_EN bit is set. The SGM41528 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/CDP/DCP) and non-standard adapter through USB D+/D- lines. When the input source type detection is completed, some registers and pins are updated as detailed below:

1. Input current limit register (the value in the IINDPM[4:0]) is changed to set current limit.
2. Input Voltage Limit (VINDPM[4:0]) register is changed to set default limit (if EN_VINDPM_RST = 1, otherwise VINDPM value remains unchanged).
3. VBUS_STAT[2:0] bits change to reflect the detected source.
4. nINT pin pulses to notify the host.
5. nPG pin is pulled low, and PG_STAT bit is set to 1.

The input current or the input voltage is always limited by the IINDPM[4:0] or VINDPM[4:0] register and the limit can be updated by the host if needed. The charger input current is always limited by the lower of IINDPM[4:0] register or ILIM pin at all-times regardless of input current optimizer (ICO) setting.

When AUTO_INDET_EN is disabled, the input source type detection is bypassed, and the input current limit (IINDPM[4:0]) register remains unchanged from previous value. When EN_VINDPM_RST is disabled, the input voltage limit (VINDPM[4:0]) register remains unchanged from previous value.

Input Current Limit by D+/D- Detection

The SGM41528 integrates a D+/D- based input source detection to set the input current limit. The D+/D- detection has three major steps: Data Contact Detect (DCD), Primary Detection, and Secondary Detection. Please refer to Figure 3.

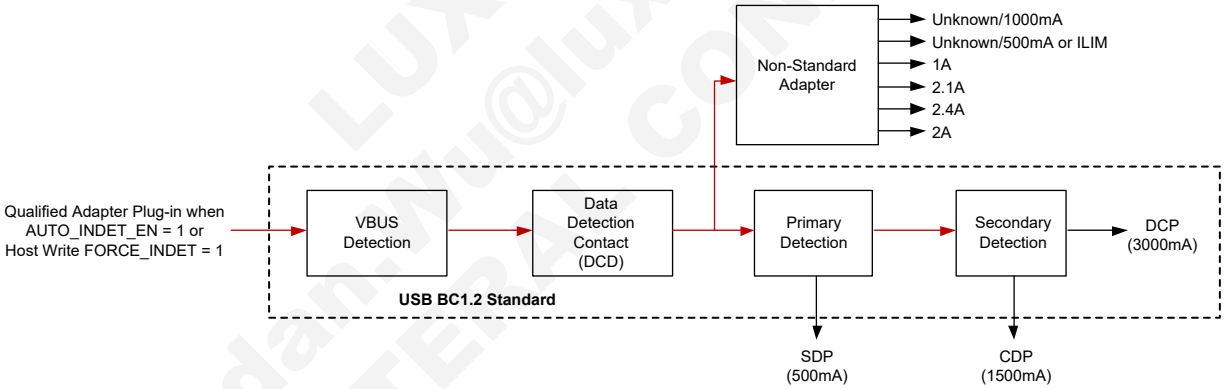


Figure 3. D+/D- Detection Flow

Table 1. Non-Standard Adapter Detection

Non-Standard Adapter	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P0_VTH}	2.1
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P8_VTH}	1
Divider 4	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P8_VTH}	2.4
Unknown 2	V_{D+} = 1MΩ to 0V	V_{D-} = 3.3V	1

After the input source type detection is done, an INT pulse is asserted to the host. In addition, the following registers including input current limit register (IINDPM[4:0]), and VBUS_STAT[2:0] register are updated as below:

DETAILED DESCRIPTION (continued)

Table 2. Input Current Limit Setting from D+/D- Detection

D+/D- Detection	Input Current Limit (I_{INDPM})	VBUS_STAT[2:0]
USB SDP (USB500)	500mA	001
USB CDP	1.5A	010
USB DCP	3.0A	011
Divider 3	1A	110
Divider 1	2.1A	110
Divider 4	2.4A	110
Unknown 5V Adapter (1)	500mA	101
Unknown 5V Adapter (2)	1000mA	101

Force Input Current Limit Detection

In host mode, the host can force the device to run input current limit detection by setting FORCE_INDET bit. After the detection is completed, FORCE_INDET bit returns to 0 by itself and input result is updated. After the detection is completed, the input current limit (I_{INDPM}), and the VBUS_STAT[2:0] bits may be changed by the device due to the detection result.

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers and TS rail (thermistor pin). The nPG pin can also be pulled up to REGN. The REGN enables when the following 3 conditions are satisfied and remain valid for a 220ms delay time, otherwise the device stays in high impedance mode (HIZ) with REGN LDO off.

1. V_{VBUS} > V_{VBUS_UVLOZ} (in the boost mode) or V_{VBUS} < V_{VBUS_UVLOZ} (in buck mode).
2. Poor Source Detection (Qualification) detects a valid input source.
3. Input Source Type Detection completes and sets appropriate input current limit.

In HIZ state, the quiescent current drawn from VBUS is very small (less than I_{VBUS_HIZ}). System is only powered by the battery in HIZ mode.

DC/DC Converter Power-Up

When the input current limit is set, the nPG pin is pulled low, the PG_STAT and VBUS_STAT[2:0] bits are changed, and the 1.5MHz switching converter composed of LSFET and HSFET is enabled and can start switching. Converter is initiated with a soft start when the system voltage is ramped up.

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

Before charging begins, the battery discharge source (I_{BAT_DISCHG}) is enabled automatically to detect the presence of battery. The host can enable I_{BAT_DISCHG} via the EN_BAT_DISCHG bit at any point during operation, including in battery only or HIZ modes.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS. PFM operation may be disabled by the host using the PFM_DIS bit. PFM operation also includes an out-of-audio (OOA) feature to prevent the converter from switching within the audible range (< 20kHz) at no load conditions. This feature may be disabled by the host using the PFM_OOA_DIS bit.

DETAILED DESCRIPTION (continued)

Input Current Optimizer (ICO)

The SGM41528 provides innovative input current optimizer (ICO) to identify maximum power point without overloading the input source. The algorithm automatically identifies maximum input current limit of a power source without staying in VINDPM to avoid input source overload.

This feature is enabled by default (EN_ICO = 1) and can be disabled by setting EN_ICO bit to 0. After DCP type input source is detected based on the procedures describe above (input source type detection), the algorithm runs automatically when EN_ICO bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected (EN_ICO = 1 is required for FORCE_ICO to work).

Table 3. Input Current Optimizer Automatic Operation

Device	Input Source	Input Current Limit (I_{INDPM})	Automatic Start ICO Algorithm when EN_ICO = 1
SGM41528 (D+/D-)	USB SDP (USB500)	500mA	Disable
	USB CDP	1.5A	Disable
	USB DCP	3.0A	Enable
	Divider 3	1A	Disable
	Divider 1	2.1A	Disable
	Divider 4	2.4A	Disable
	Unknown 5V Adapter (1)	500mA	Disable
	Unknown 5V Adapter (2)	1000mA	Disable

The actual input current limit used by the dynamic power management is reported in ICO_ILIM[4:0] register while input current optimizer is enabled (EN_ICO = 1) or set by IINDPM[4:0] register when the algorithm is disabled (EN_ICO = 0). In addition, the current limit is clamped by ILIM pin unless EN_ILIM bit is 0 to disable ILIM pin function.

When the algorithm is enabled, it runs continuously to adjust input current limit of dynamic power management (I_{INDPM}) using ICO_ILIM[4:0] register until ICO_STAT[1:0] and ICO_FLAG bits are set (the ICO_FLAG bit indicates any change in ICO_STAT[1:0] bits). The algorithm operates depending on battery voltage:

1. When battery voltage is below V_{SYS_MIN}, the algorithm starts ICO_ILIM[4:0] register with I_{INDPM} which is the maximum input current limit allowed by system
2. When battery voltage is above V_{SYS_MIN}, the algorithm starts ICO_ILIM[4:0] register with 500mA which is the minimum input current limit to minimize adapter overload

When optimal input current is identified, the ICO_FLAG bit are set and ICO_STAT[1:0] bits are updated to indicate the status. The input current limit in ICO_ILIM[4:0] register would not be changed until the algorithm is forced to run by the following event (these events also reset the ICO_STAT[1:0] bits to '01'):

1. A new input source is plugged-in, or EN_HIZ bit is toggled.
2. IINDPM[4:0] register is changed.
3. VINDPM[4:0] register is changed.
4. FORCE_ICO bit is set to 1.
5. VBUS_OVP event.

DETAILED DESCRIPTION (continued)

Buck Mode

The SGM41528 supports USB On-The-Go. When a load device is connected to the USB port, the converter can operate as a step-down synchronous converter (buck mode) with 1.5MHz switching frequency to supply power from the battery to that load. The 500mA (OTG_ILIM[3:0] = 0000) USB OTG output current limit requirement is achieved by programming, however the buck converter can deliver 2A to the output (default limit). Converter will be set to buck mode if at least 30ms is passed from enabling this mode (EN_OTG bit = 1) and the following conditions are satisfied:

1. $V_{BAT} > V_{OTG\_BAT}$.
2. $V_{VBUS} < V_{VBUS\_PRESENT}$.
3. Voltage at TS (thermistor) pin is within range configured by buck mode temperature monitor as configured by BHOT[1:0] and BCOLD register bits.

The output voltage is set to V_{VBUS} = 5.1V by default (selectable via OTG_VLIM[3:0] register bits) and is maintained as long as V_{BAT} is above V_{OTG_BAT}, and V_{VBUS} is above $V_{VBUS\_PRESENT}$. The output current can reach up to the programmed value by OTG_ILIM bit (2A). The VBUS_STAT[2:0] status register bits are set to 111 in buck mode (OTG).

In order to improve light-load efficiency, the device switches to PFM control at light load. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS. PFM operation may be disabled by the host using the PFM_DIS bit. PFM operation also includes an out-of-audio (OOA) feature to prevent the converter from switching within the audible range (< 20kHz) at no load conditions. This feature may be disabled by the host using the PFM_OOA_DIS bit.

Host Mode and Default Mode Operation with the Watchdog Timer

After a power-on reset, the device starts in default mode (standalone) with all registers reset as if the watchdog timer is expired. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41528 operates like an autonomous charger. The battery is charged for 16.5 hours (default value for the fast charging safety timer). Then the charge stops while boost converter continues to operate to power the system load.

Most of the flexibility features of the SGM41528 become available in the host mode when the device is controlled by a host with I²C. By setting the WD_RST bit to 1, the charger mode changes from default mode to host mode. In this mode the WD_STAT bit is low and all device parameters can be programmed by the host. To prevent the device watchdog reset from going back to the default mode, the host must disable the watchdog timer by setting WATCHDOG[1:0] = 00, or it must consistently reset the watchdog timer before expiry by writing 1 to WD_RST to prevent WD_STAT bit to be set. Every time a 1 is written to the WD_RST, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. If the watchdog timer expires (WD_STAT bit = 1), the device returns to default mode and all registers are reset to their default values except as detailed in the Register Maps section.

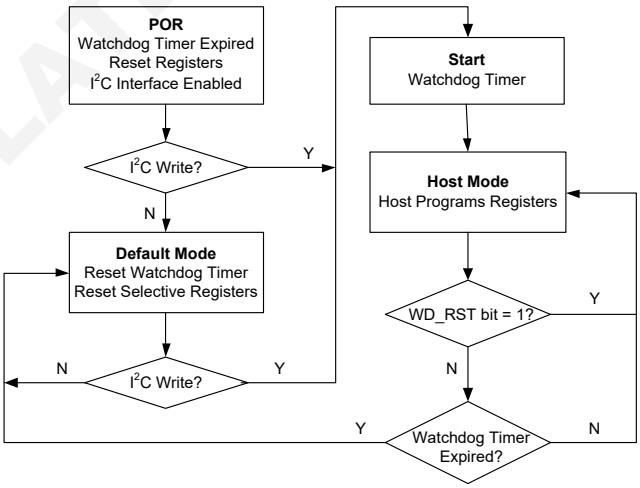


Figure 4. Watchdog Timer Flow Chart

DETAILED DESCRIPTION (continued)

Battery Charging Management

The SGM41528 is designed for charging 2-cell Li-Ion or Li-poly batteries with a charge current up to 2.2A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path features low on-resistance to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if EN_CHG = 1 and nCE pin is pulled low. In default mode, the SGM41528 runs a charge cycle with the default parameters itemized in Table 4. At any moment, the host can be controlled by changing to the host mode.

Table 4. Charging Parameter Default Setting

Default Mode	SGM41528
Charging Voltage (VREG)	8.40V
Charging Current (I_{CHG_REG})	1.00A
Pre-Charge Current (I_{PRECHG})	150mA
Termination Current (I_{TERM})	150mA
Temperature Profile	JEITA
Safety Timer	16.5 hours

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied a new charge cycle starts:

- NTC temperature fault is not asserted (TS pin).
- Safety timer fault is not asserted.
- Charging enabled (2 conditions: EN_CHG bit = 1, nCE pin is low).
- Battery voltage is below the programmed full charge level (VREG).

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (VREG - 100mV or VREG - 200mV configured by VRECHG[1:0] bits). Also, if the charge cycle is completed, a new charging cycle can be initiated by toggling of the nCE pin or EN_CHG bit.

Normally a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or Dynamic Power Management (DPM) mode.

Charge Status Report

The status register (CHRG_STAT[2:0]) indicates the different charging phases as:

- 000 = Not Charging
- 001 = Trickle Charge ($V_{BAT} < V_{BAT\_SHORT}$)
- 010 = Pre-charge ($V_{BAT\_SHORT} < V_{BAT} < V_{BAT\_LOW}$)
- 011 = Fast Charge (CC Mode)
- 100 = Taper Charge (CV Mode)
- 101 = Top-off Timer Active Charging
- 110 = Charge Termination Done

When the charger transitions to any of these states, including when charge cycle is completed, an INT is asserted to notify the host.

DETAILED DESCRIPTION (continued)

Battery Charging Profile

The SGM41528 features a full battery charging profile with five phases. In the beginning of the cycle, the battery voltage (V_{BAT}) is tested and appropriate current and voltage regulation levels are selected as shown in Table 5. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The phases are: battery short (battery voltage too low), pre-conditioning, constant current, constant voltage and an optional top-off trickle charging phase.

Table 5. Charging Current Setting Based on V_{BAT}

V_{BAT}	Selected Charging Current	Default Value in the Register	CHRG_STAT[2:0]
< V_{BAT_SHORT}	I_{SHORT}	70mA	001
V_{BAT_SHORT} to V_{BAT_LOW}	I_{PRECHG}	150mA	010
> V_{BAT_LOW}	I_{CHG}	1000mA	011

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified: the charge current will be less than the value in the register; termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

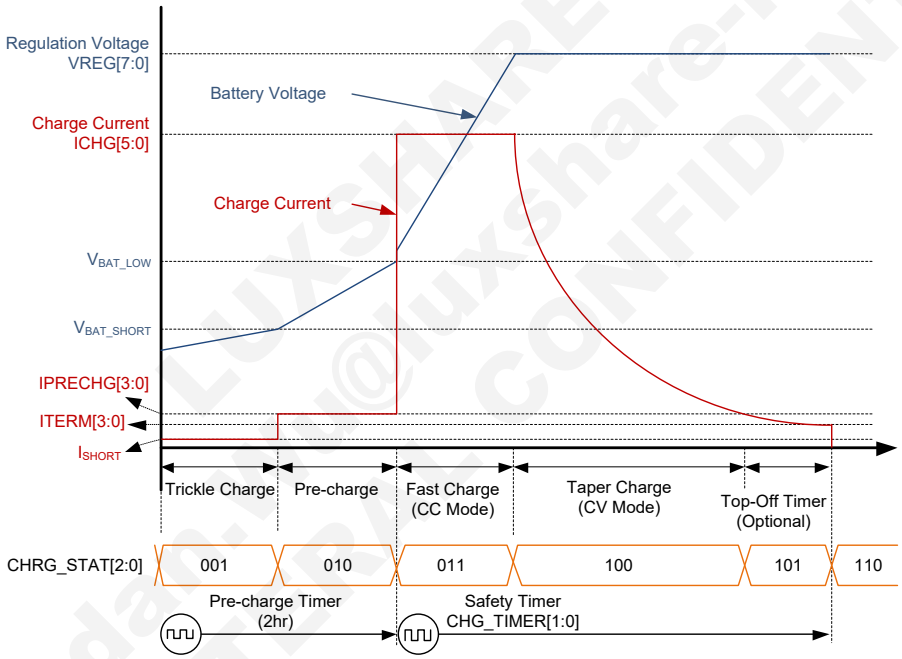


Figure 5. Battery Charging Profile

Termination

A charge cycle is terminated when the battery voltage is above the recharge threshold and the current falls below the programmed termination current. Unless there is a high power demand for system and need to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the boost converter continues to operate to supply power to the system.

CHRG_STAT[2:0] register is set to 110 and a negative pulse is sent to nINT pin after termination.

If the charger is regulating input current or input voltage or junction temperature instead of charge current, termination will be temporarily prevented. EN_TERM bit is termination control bit and can be set to 0 to permanently disable termination before it happens.

DETAILED DESCRIPTION (continued)

At low termination currents (50mA TYP), the offset in the internal comparator may rise up to 40% higher actual termination current. A delay in termination can be added (optional) as a compensation for comparator offset using a programmable top-off timer. During the delay, constant voltage charge phase continues and gives the falling charge current the chance to drop closer to the programmed value. The top-off delay timer has the same restrictions of the safety timer. As an example, if under some conditions the safety timer is suspended, the top-off timer will also be suspended or if the safety timer is slowed down, the termination timer will also be slowed down. The CHRG_STAT bit reports the active status of the top-off timer via the 101 code. Once the top-off timer expires, the CHRG_STAT[2:0] register is set to 110 and an INT pulse is asserted to the host.

Any of the following events resets the top-off timer:

1. Disable to enable transition of nCE (charge enable).
2. A low to high change in the status of termination.
3. Set REG_RST bit to 1.

The setting of the top-off timer is applied at the time of termination detection and unless a new charge cycle is started, modifying the top-off timer parameters after termination has no effect. A negative pulse is sent to nINT when top-off timer is started or ended. All charge cycle related INT pulses (including top-off timer INT pulses) can be masked by CHRG_MASK bit.

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines. There is no battery temperature protection when boost or buck converter stop switching.

Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should to be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside normal operating temperatures (typically 0℃ and 60℃). Four temperatures levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range charging should be stopped. The corresponding voltages sensed by NTC are named V_{T1} to V_{T4}. Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin. The battery cool range is between T1 - T2 and the warm range is between T3 - T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the TS voltage within V_{T1} to V_{T4} window limits. If during the charge, battery gets too cold or too hot and TS voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

JEITA recommends reducing charge current to 1/2 of fast charging current or lower at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to be kept below 4.1V.

The SGM41528 exceeds the JEITA requirement by its flexible charge parameter settings. At warm temperature range (T3 - T4), the charge voltage can be set to V_{REG}, 8.0V, 8.3V, or charge suspend using the JEITA_VSET[1:0] register. At cool temperatures (T1 - T2), the fast charge current setting can be 100%, 40%, or 20% of fast charge current selectable by the JEITA_ISETC[1:0] bits. Whenever the charger detects "warm" or "cool" temperature, the termination is automatically disabled regardless of JEITA_VSET[1:0], JEITA_ISETH and JEITA_ISETC[1:0] register bit settings.

DETAILED DESCRIPTION (continued)

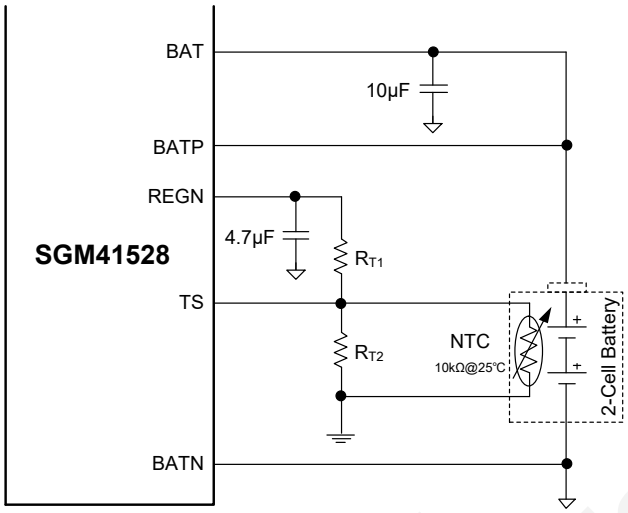


Figure 6. Battery Thermistor Connection and Bias Network

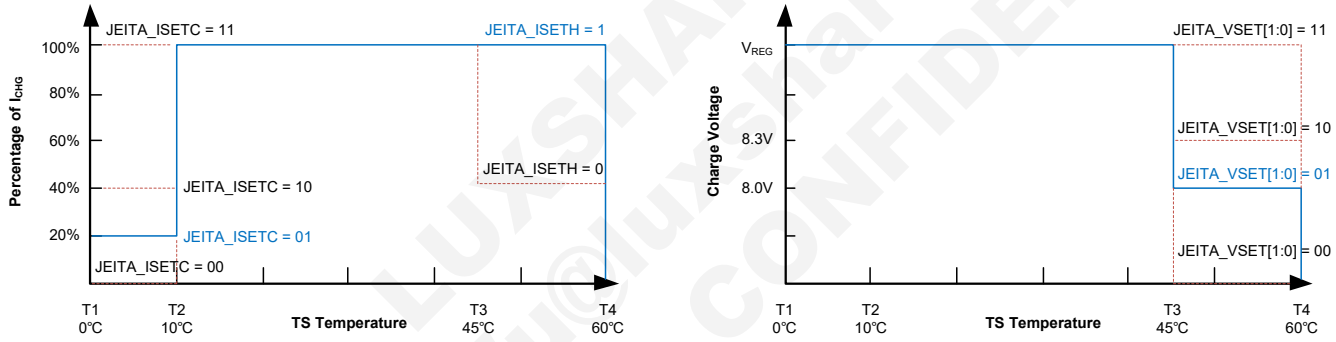


Figure 7. TS Charging Values

A 103AT-2 type thermistor is recommended for use with the SGM41528. Other thermistors may be used and bias network (Figure 6) can be calculated based on the following equations:

$$R_{T2} = \frac{V_{REGN} \times R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{V_{REGN}}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{V_{REGN}}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\left(\frac{V_{REGN}}{V_{T1}}\right) - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

Where, V_{T1}, V_{T4} and V_{REGN} are characteristics of the device and R_{THCOLD} and R_{THHOT} are thermistor resistances (R_{TH}) at desired T1 (Cold) and T4 (Hot) temperatures. Select T_{COLD} = 0℃ and T_{HOT} = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ that results in:

- R_{T1} = 5.24kΩ
- R_{T2} = 30.31kΩ

DETAILED DESCRIPTION (continued)

OTG Buck Mode Temperature Monitoring

The device is capable to monitor the battery temperature for safety during the OTG buck mode. The temperature must remain within the V_{BCOLDx} to V_{BHOTx} thresholds otherwise the OTG mode will be suspended and VBUS_STAT[2:0] bits are set to 000. Moreover, TS_STAT[2:0] register is updated to report OTG mode cold or hot condition. Once the temperature returns within the window, the OTG mode is resumed and TS_STAT[2:0] register is cleared to 000 (normal).

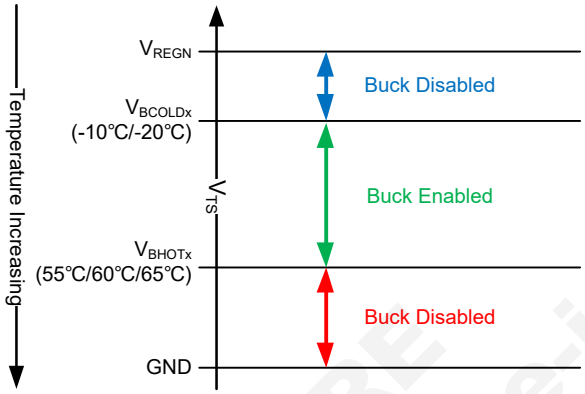


Figure 8. TS Pin Thermistor Temperature Window Settings in OTG Buck Mode

Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the safety time is expired, TMR_STAT bit is set to 1 and a negative pulse is sent to nINT pin. This feature is optional and can be disabled by clearing EN_TIMER bit.

The safety timer counts at half clock rate when charger is running under input voltage regulation, input current regulation or thermal regulation, because in these conditions, the actual charge current is likely to be less than the register setting. As an example, if the safety timer is set to 7.5 hours and the charger is regulating the input current (IINDPM_STAT bit = 1) in the whole charging cycle, the actual safety time will be 15 hours. Clearing the TMR2X_EN bit will disable the half clock rate feature. Changing the TMR2X_EN bit while the device is running has no effect on the safety timer count, other than forcing the timer to count at half the rate under the conditions dictated above.

The safety timer is paused if the fault which disable charging, or supplement mode occurs and charging is suspended. Since the timer is not counting in this state, the TMR2X_EN bit has no effect. It will resume once the fault condition is removed. If charging cycle is stopped by a restart or by toggling nCE pin or EN_CHG bit, the timer resets and restarts a new timing.

The safety timer is reset for the following events:

1. Charging cycle stop and restart (toggle nCE pin, EN_CHG bit, or charged battery falls below recharge threshold).
2. BAT voltage changes from pre-charge to fast charge or vice versa (in host-mode or default mode).

The pre-charge safety timer (fixed 2hr counter that runs when $V_{BAT} < V_{BAT\_SHORT}$), follows the same rules as the fast charge safety timer in terms of getting suspended, reset, and counting at half-rate when TMR2X_EN is set.

DETAILED DESCRIPTION (continued)

Narrow Voltage DC (NVDC) Design in SGM41528

The SGM41528 features an NVDC design using the BATFET that connects the system and battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using boost converter even if the battery voltage is very low. MOSFET linear mode allows for the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. SYS_MIN[3:0] register sets the minimum system voltage (default 7V). If the system is in minimum system voltage regulation, VSYS_STAT bit is set.

The BATFET operates in linear region when the battery voltage is below the minimum system voltage setting. The system voltage is regulated to 300mV (TYP) above the minimum system voltage setting. The battery gradually gets charged and its voltage rises above the minimum system voltage and lets BATFET to change from linear mode to fully turned-on switch such that the voltage difference between the system and battery is the small V_{DS} of fully on BATFET.

The system voltage is always regulated to 100mV (TYP) above the battery voltage if:

1) The charging is terminated or
2) Charging is disabled and the battery voltage is above the minimum system voltage setting.

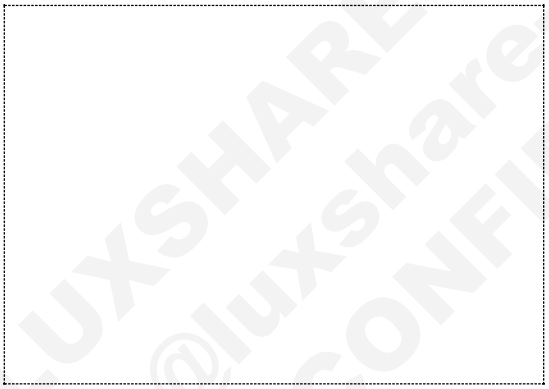


Figure 9. System Voltage vs. Battery Voltage

SGM41528 Dynamic Power Management (DPM)

The SGM41528 features a dynamic power management (DPM). To implement DPM the device always monitors, the input current and voltage to regulate power demand from the source and avoid input adapter overloading or to meet the maximum current limits specified in the USB specifications. Overloading an input source may results in either current trying to exceed the input current limit (I_{INDPM} or ICO_ILIM or ILIM pin setting) or the voltage tending to fall below the input voltage limit (V_{INDPM}). With DPM, the device keeps the VSYS regulated to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduces to satisfy $I_{IN} \le I_{INDPM}$ or $V_{IN} \ge V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINDPM) or V_{IN} type (VINDPM) depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased and reached to zero, but the input is still overloaded. In this case the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provide a portion of system power demand from the battery through the BATFET.

The IINDPM_STAT or VINDPM_STAT status bits are set during an IINDPM or VINDPM respectively. Figure 10 summarizes the DPM behavior (IINDPM type) for a design example with a 5V/3A adapter, 6.4V battery, 1.5A charge current setting and 6.8V minimum system voltage setting.

DETAILED DESCRIPTION (continued)

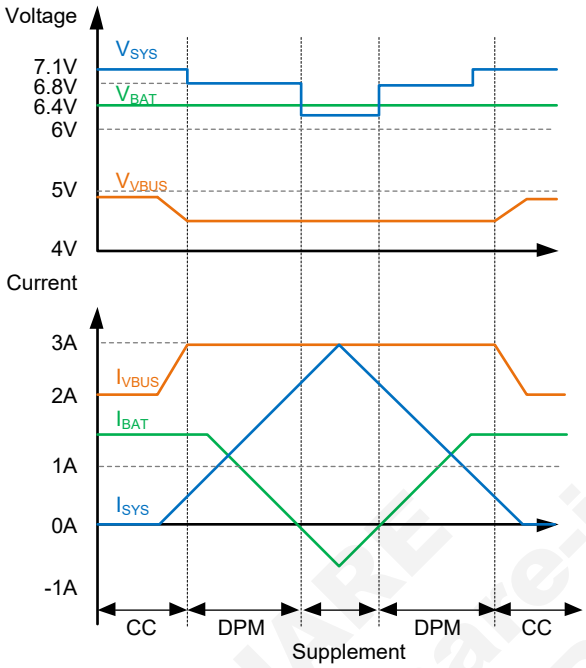


Figure 10. Input, Battery and System Voltage and Currents in DPM

Supplement Mode

If the system voltage drops below the battery voltage, the BATFET gradually starts to turn on. At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation). At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by $R_{DSON} \times I_D$). Use of the MOSFET linear mode at lower currents prevents swinging oscillation of entering and exiting the supplement mode.

BATFET gate regulation V-I characteristics is shown in Figure 11. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

Figure 11. BATFET Gate Regulation V-I Curve

DETAILED DESCRIPTION (continued)

Integrated 16-Bit ADC for Monitoring

The device includes a 16-bit ADC to monitor critical system information based on the device's modes of operation. The control of the ADC is done through the ADC control register (REG15). The ADC_EN bit provides the ability to enable and disable the ADC to conserve power. The ADC_RATE bit allows continuous conversion or one-shot behavior. After a one-shot conversion finishes, the ADC_EN bit is cleared, and must be re-asserted to start a new conversion.

To enable the ADC, the ADC_EN bit must be set to 1. The ADC is allowed to operate if either the V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ} is valid. If no adapter is present, and the V_{BAT} is less than V_{BAT_UVLOZ}, the device will not perform an ADC measurement, nor update the ADC read-back values in REG17 through REG24. Additionally, the device will immediately reset ADC_EN bit without sending any interrupt. The same will happen if the ADC is enabled when all ADC channels are disabled. It is recommended to read back ADC_EN bit after setting it to 1 to ensure ADC is running a conversion. If the charger changes modes (for example, if the adapter is connected, EN_HIZ goes to 1, or EN_OTG goes to 1) while an ADC conversion is running, the conversion is interrupted. Once the mode change is complete, the ADC resumes conversion, starting with the channel where it was interrupted.

The ADC_SAMPLE[1:0] bits control the sample speed of the ADC, with conversion time of t_{ADC_CONV}. The integrated ADC has two rate conversion options: a one-shot mode and a continuous conversion mode set by the ADC_RATE bit. By default, all ADC parameters will be converted in one-shot or continuous conversion mode unless disabled in the ADC function disable register (REG16). If an ADC parameter is disabled by setting the corresponding bit in REG16, then the read-back value in the corresponding register will be from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place). If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC function disable register is set to 0. If all channels are disabled in one-shot conversion mode, the ADC_EN bit is cleared.

The ADC_DONE_STAT and ADC_DONE_FLAG bits signal when a conversion is complete in one-shot mode only. This event produces an INT pulse, which can be masked with ADC_DONE_MASK bit. During continuous conversion mode, the ADC_DONE_STAT bit has no meaning and will be 0. The ADC_DONE_FLAG bit will remain unchanged in continuous conversion mode.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = 0 to disable the ADC. ADC conversion is interrupted upon adapter plug-in, and will only resume until after input source type detection is complete. ADC readings are only valid for DC states and not for transients. When host writes ADC_EN = 0, the ADC stops immediately, and ADC measurement values correspond to last valid ADC reading.

If the host wants to exit ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE bit to one-shot, and the ADC will stop at the end of a complete cycle of conversions, or
2. Disable all ADC conversion channels, and the ADC will stop at the end of the current measurement.

DETAILED DESCRIPTION (continued)

Status Outputs Pins (nPG and nINT)

Power Good Indication (nPG)

When a good input source is connected to VBUS and input type is detected, the PG_STAT status bit goes high and the nPG pin goes low. A good input source is detected if all following conditions on V_{VBUS} are satisfied and input type detection is completed:

- V_{VBUS} is in the operating range: $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$.
- Input source is not poor: $V_{VBUS} > V_{BAD\_SRC}$ (3.6V TYP) when I_{BAD_SRC} (15mA TYP) loading is applied. (Poor source detection.)
- Completed input source type detection.

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt it can react and check the charger situation on time. By default, the following events will generate an INT pulse.

1. Good input source detected
   a) $V_{VBUS} < V_{VBUS\_OV}$ threshold
   b) $V_{VBUS} > V_{BAD\_SRC}$ when I_{BAD_SRC} current is applied (not a poor source)
2. Good input source removed
3. Entering IC junction temperature regulation during charging (T_{REG})
4. Entering VINDPM regulation
5. Entering IINDPM regulation
6. I²C Watchdog timer expired
   At initial power-up, this INT gets asserted to signal I²C is ready for communication
7. VBUS_STAT[2:0] register changes state (VBUS_STAT[2:0] any bit change)
8. TS_STAT[2:0] register changes state (TS_STAT[2:0] any bit change)
9. Charger status changes state (CHRG_STAT[2:0] register values change), including charge complete
10. A rising edge on any of the *_STAT bits
11. Battery over-voltage detected (V_{BAT_OVP})
12. Junction temperature shutdown (T_{SHUT})
13. VBUS over-voltage detected (V_{VBUS_OVP})
14. Charge safety timer expired

Each one of these INT sources can be masked off to prevent INT pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the current status of each INT source.
- The FLAG bit holds information on which source produced an INT, regardless of the current status.
- The MASK bit is used to prevent the device from sending out INT for each particular event.

When one of the above conditions occurs (a rising edge on any of the *_STAT bits), the device sends out an INT pulse and keeps track of which source generated the INT via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG.

DETAILED DESCRIPTION (continued)

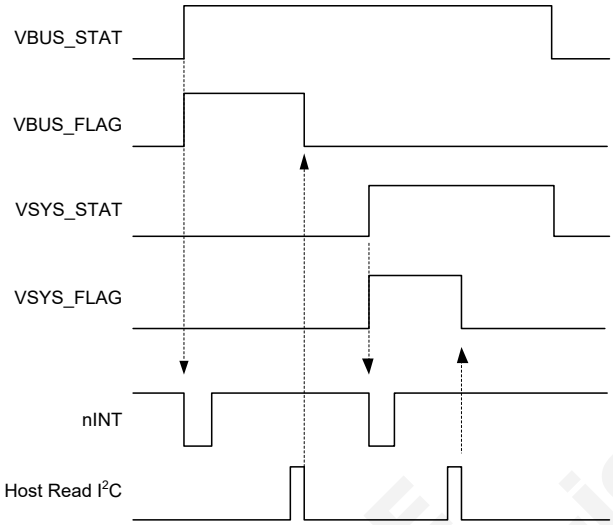


Figure 12. INT Generation Behavior Example

Input Current Limit on ILIM Pin

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM pin setting and register setting (IINDPM[4:0]). For example, if the register setting is 3.3A (0x1C), and ILIM has an 820Ω resistor to ground, the input current limit is 1.32A (K_{ILIM} = 1080 TYP). ILIM pin can be used to set the input current limit rather than the register settings when EN_ILIM bit is set. The device regulates ILIM pin at 0.8V. If ILIM voltage exceeds 0.8V, the device enters input current regulation (refer to Dynamic Power Management section). Entering IINDPM through ILIM pin sets the IINDPM_STAT and FLAG bits, and produces an interrupt to host. The interrupt can be masked via the IINDPM_MASK bit.

The ILIM pin can also be used to monitor input current when EN_ILIM bit is set and the device is not in ILIM regulation. The voltage on ILIM pin is proportional to the input current. ILIM can be used to monitor input current with the following relationship:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \quad (4)$$

For example, if ILIM pin is set with 820Ω resistor, and the ILIM voltage 0.5V, the actual input current is 0.823A (TYP). If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8V. If ILIM pin is shorted, the input current limit is set by the register.

The ILIM pin function can be disabled by setting the EN_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring function are not available.

DETAILED DESCRIPTION (continued)

SGM41528 Protection Features

Monitoring of Voltage and Current

During the converter operation, the input and system voltages (V_{VBUS} and V_{SYS}) and switch currents are constantly monitored to assure safe operation of the device in both buck and boost modes, as will be explained below.

Boost Mode Voltage and Current Monitoring

1. Input Over-Voltage

The valid input voltage range for boost mode operation is V_{VBUS_OP}. Converter switching will stop as soon as VBUS voltage exceeds V_{VBUS_OV} over-voltage limit. During input over-voltage, an INT pulse is asserted to signal the host, and the VBUS_OVP_STAT and VBUS_OVP_FLAG fault registers get set. The device automatically starts switching again when the over-voltage condition goes away.

2. Input Under-Voltage

The valid input voltage range for boost mode operation is V_{VBUS_OP}. If V_{VBUS} voltage falls below V_{BAD_SRC} during operation, the device stops switching. During input under-voltage, an INT pulse is asserted to signal the host, and the PG_STAT bit gets cleared. The PG_FLAG bit will get set to signal this event. The device automatically attempts to restart switching when the under-voltage condition goes away.

3. System Over-Voltage (SYSOVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP threshold is related to the battery voltage. When $V_{BAT} < V_{SYS\_MIN}$, the SYSOVP threshold is V_{SYS_MIN} + 360mV; when $V_{BAT} > V_{SYS\_MIN}$, the SYSOVP is V_{BAT} + 440mV. Once a SYSOVP occurs, switching stops to clamp any overshoot and a 16mA sink current is applied to SYS to pull the voltage down.

4. System Over-Current

The charger device continually monitors and compares V_{VBUS} to V_{SYS} to protect against a system short-circuit event. In the event that V_{SYS} drops to within 250mV of V_{VBUS} during operation, and the input current exceeds IINDPM threshold, a short circuit event is flagged and the converter stops switching. The SYS_SHORT_FLAG bit is set and an INT pulse is asserted to the host. The device attempts to recover from this condition automatically.

OTG Buck Mode Voltage and Current Monitoring

In buck mode, the QBLK (blocking FET) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Output Over-Voltage Protection for VBUS

In buck mode, converter stops switching and exits buck mode (by clearing EN_OTG bit) if VBUS voltage rises above regulation and exceeds the V_{OTG_OVP} over-voltage limit (6V TYP). An INT pulse is sent and the OTG_FLAG bit is set high.

2. Output Over-Current Protection for VBUS

The device monitors output current to provide output short protection. The OTG buck mode has built-in constant current regulation to allow OTG to adapt to various types of loads. If short circuit is detected on VBUS, the OTG turns off and OTG is disabled with EN_OTG bit cleared. In addition, the OTG_FLAG bit is set high to indicate the fault, and an INT is asserted to the host.

DETAILED DESCRIPTION (continued)

SGM41528 Thermal Regulation and Shutdown

Boost Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of 120℃ is considered for maximum IC surface temperature in boost mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to 120℃ (thermal regulation mode) and sets the TREG_STAT bit to 1. As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation. A wide thermal regulation range from +60℃ to +120℃ allows optimization for the system thermal performance.

If the temperature exceeds T_{SHUT} (150℃), thermal shutdown protection arise in which the converter is turned off, the fault register bits TSHUT_STAT and TSHUT_FLAG are set and an INT pulse is sent.

When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (20℃ under T_{SHUT}), the converter resumes automatically.

If the charge is disabled, the thermal regulation mode doesn't work, but the thermal shutdown protection keeps work.

OTG Buck Mode Thermal Protections

Similar to boost mode, T_J is monitored in OTG buck mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (150℃), the buck mode will be disabled (converter is turned off) by setting EN_OTG bit low. If T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}). Buck can recover again by re-enabling EN_OTG bit by host.

Battery Protections

Battery Over-Voltage Protection (BATOVP)

The over-voltage limit for the battery is 4% above the battery regulation voltage setting while charging. In case of a BATOVP, charging stops right away, the BATOVP_STAT bit is set to 1 and an INT pulse is sent.

Battery Over-Discharge Protection

If battery discharges too much and V_{BAT} falls below the depletion level (V_{BAT_UVLOZ}), the device turns off BATFET to protect battery. This protection is latched and is not recovered until an input source is connected to the VBUS pin. In such condition, the battery will start charging with the small I_{SHORT} current (70mA TYP) first as long as $V_{BAT} < V_{BAT\_SHORT}$. When battery voltage is increased and $V_{BAT\_SHORT} < V_{BAT} < V_{BAT\_LOW}$, the charge current will increase to the pre-charge current level programmed in the IPRECHG[3:0] register.

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41528 parameters and get status reports. I²C is well known 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41528 operates as a slave device with address 0x6B (6BH). It has 26 8-bit registers, numbered from REG00 to REG25. A register read beyond REG25 (0x25) returns 0xFF.

Physical Layer

The SGM41528 supports I²C standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s) communication speeds. Bus lines are pulled high by weak current source or pull-up resistors are in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

DETAILED DESCRIPTION (continued)

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 13. All transactions begin by the master who applies a START condition on the bus lines to take over the bus and exchange data. In the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is when SCL is high and a high-to-low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low-to-high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

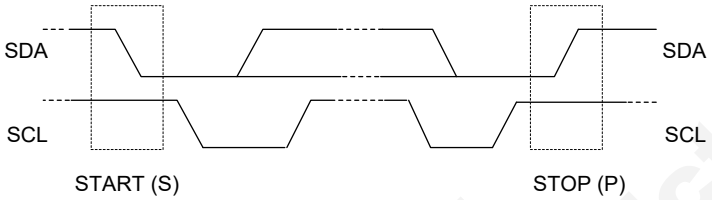


Figure 13. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the HIGH period of the clock. The state of the SDA can only change when the clock (SCL) is LOW. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 14.

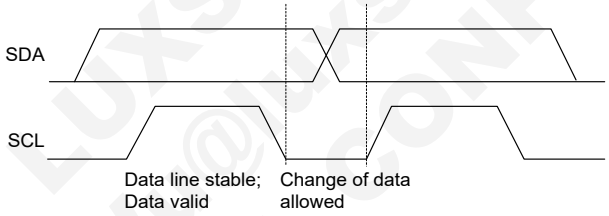


Figure 14. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 15 shows the byte transfer process with I²C interface.

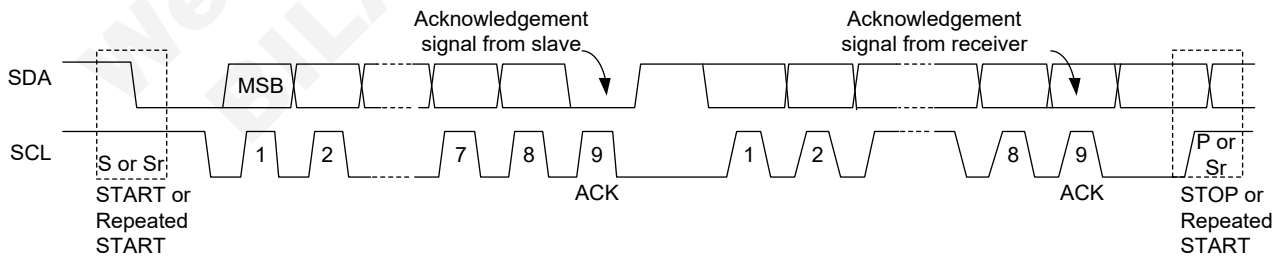


Figure 15. Data Transfer on the I²C Bus

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter an acknowledge bit is replied by the receiver as ninth bit. With the acknowledge bit the receiver informs the transmitter that the byte was received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including for the acknowledge ninth bit, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse and the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address and then without a stop condition another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is also a WRITE sending the register address that is supposed to be accesses in the next byte(s). The device 7-bit address is defined as '1101011' (0x6B) by default. The address bit arrangement is shown below.

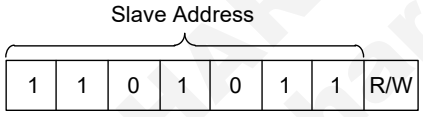


Figure 16. 7-Bit Addressing (0x6B)

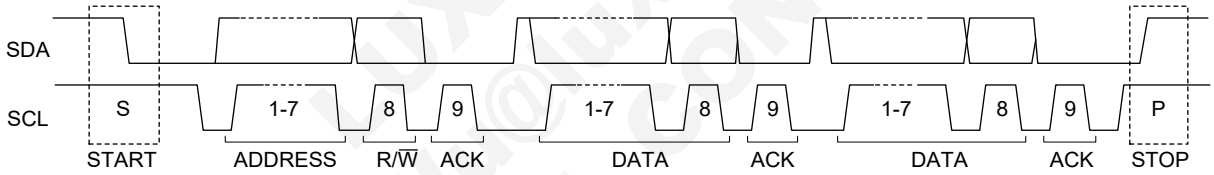


Figure 17. A Complete Data Transfer Transaction

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 18 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

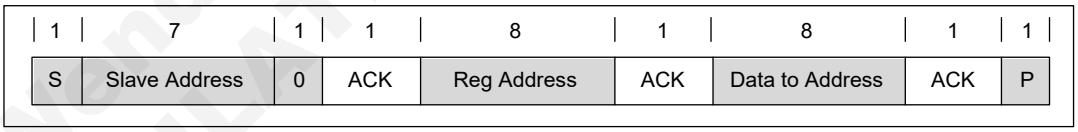


Figure 18. A Single Write Transaction

DETAILED DESCRIPTION (continued)

READ: If the master wants to read a single register (Figure 19), it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NAK is sent by master. A STOP must be sent by master in any case to end the transaction.

In the figures, the data blocks with gray background shows the bits sent by master and the white background represent data bits sent by slave. If the register address is not defined, the device replies with NCK and goes back to the I²C slave idle state.

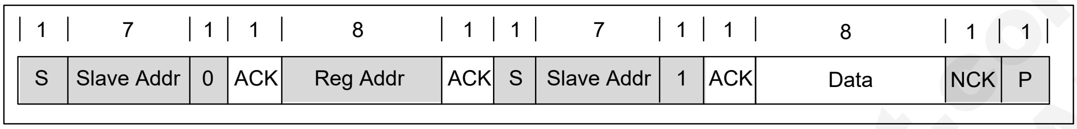


Figure 19. A Single Read Transaction

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41528 for REG00 through REG25 registers, as explained in Figure 20 and Figure 21.

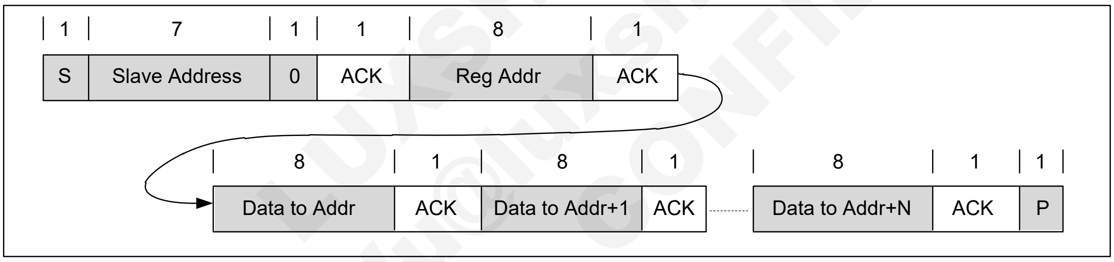


Figure 20. A Multi-Write Transaction

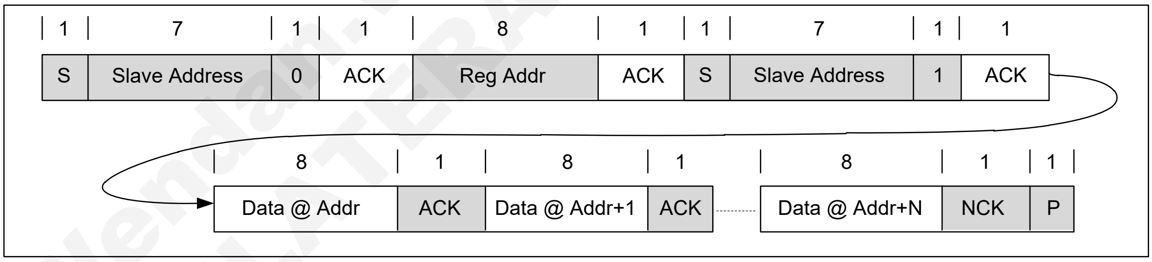


Figure 21. A Multi-Read Transaction

REGISTER MAPS

I²C Slave Address of SGM41528 is: 0x6B (7 Bits)

R/W: Read/Write bit(s)
R: Read only bit(s)
PORV: Power-On Reset Value

Table 6. I²C Registers

Address	Access Type	Acronym	Register Name	Section
00h	R/W	REG00	Battery Voltage Regulation Limit	Go
01h	R/W	REG01	Charge Current Limit	Go
02h	R/W	REG02	Input Voltage Limit	Go
03h	R/W	REG03	Input Current Limit	Go
04h	R/W	REG04	Pre-Charge and Termination Current Limit	Go
05h	R/W	REG05	Charger Control 1	Go
06h	R/W	REG06	Charger Control 2	Go
07h	R/W	REG07	Charger Control 3	Go
08h	R/W	REG08	Charger Control 4	Go
09h	R/W	REG09	OTG Control	Go
0Ah	R	REG0A	ICO Current Limit	Go
0Bh	R	REG0B	Charger Status 1	Go
0Ch	R	REG0C	Charger Status 2	Go
0Dh	R	REG0D	NTC Status	Go
0Eh	R	REG0E	FAULT Status	Go
0Fh	R	REG0F	Charger Flag 1	Go
10h	R	REG10	Charger Flag 2	Go
11h	R	REG11	Fault Flag	Go
12h	R/W	REG12	Charger Mask 1	Go
13h	R/W	REG13	Charger Mask 2	Go
14h	R/W	REG14	Fault Mask	Go
15h	R/W	REG15	ADC Control	Go
16h	R/W	REG16	ADC Function Disable	Go
17h	R	REG17	IBUS ADC 1	Go
18h	R	REG18	IBUS ADC 0	Go
19h	R	REG19	ICHG ADC 1	Go
1Ah	R	REG1A	ICHG ADC 0	Go
1Bh	R	REG1B	VBUS ADC 1	Go
1Ch	R	REG1C	VBUS ADC 0	Go
1Dh	R	REG1D	VBAT ADC 1	Go
1Eh	R	REG1E	VBAT ADC 0	Go
1Fh	R	REG1F	VSYS ADC 1	Go
20h	R	REG20	VSYS ADC 0	Go
21h	R	REG21	TS ADC 1	Go
22h	R	REG22	TS ADC 0	Go
23h	R	REG23	TDIE ADC 1	Go
24h	R	REG24	TDIE ADC 0	Go
25h	R/W	REG25	Part Information	Go

REGISTER MAPS (continued)

REG00: Battery Voltage Regulation Limit Register

Register address: 0x00; R/W

PORV = 0xA0

Table 7. REG00 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	VREG[7:0]	VREG[7] 1 = 1280mV	Charge Voltage Limit Offset: 6.80V Range: 6.80V - 9.20V Default: 8.40V (10100000)	1	R/W	REG_RST or Watchdog
		VREG[6] 1 = 640mV		0	R/W	
		VREG[5] 1 = 320mV		1	R/W	
		VREG[4] 1 = 160mV		0	R/W	
		VREG[3] 1 = 80mV		0	R/W	
		VREG[2] 1 = 40mV		0	R/W	
		VREG[1] 1 = 20mV		0	R/W	
		VREG[0] 1 = 10mV		0	R/W	

REG01: Charge Current Limit Register

Register address: 0x01; R/W

PORV = 0x54

Table 8. REG01 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	EN_HIZ	Enable HIZ Mode 0 = Disable (default) 1 = Enable		0	R/W	REG_RST or Watchdog
D[6]	EN_ILIM	Enable ILIM Pin Function 0 = Disable 1 = Enable (default)		1	R/W	REG_RST or Watchdog
D[5:0]	ICHG[5:0]	ICHG[5] 1 = 1600mA	Fast Charge Current Limit Offset: 0mA Range: 100mA - 2200mA Default: 1000mA (010100) Notes: I_{CHG} > 2.2A (2Ch) clamped to 2.2A. I_{CHG} < 100mA (01h) clamped at 100mA.	0	R/W	REG_RST or Watchdog
		ICHG[4] 1 = 800mA		1		
		ICHG[3] 1 = 400mA		0		
		ICHG[2] 1 = 200mA		1		
		ICHG[1] 1 = 100mA		0		
		ICHG[0] 1 = 50mA		0		

REGISTER MAPS (continued)

REG02: Input Voltage Limit Register

Register address: 0x02; R/W

PORV = 0x85

Table 9. REG02 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	EN_VINDPM_RST	Enable VINDPM Automatic Reset upon Adapter Plug-in 0 = Disable VINDPM reset when adapter is plugged in 1 = Enable VINDPM reset when adapter is plugged in (VINDPM resets to default value after input source type detection)		1	R/W	REG_RST or Watchdog
D[6]	EN_BAT_DISCHG	Enable BAT Pin Discharge Load (I_{BAT_DISCHG}) 0 = Disable load (default) 1 = Enable BAT discharge load		0	R/W	REG_RST or Watchdog
D[5]	PFM_OOA_DIS	PFM Out-of-Audio (OOA) Mode Disable 0 = Out-of-audio mode enabled while in converter is in PFM (default) 1 = Out-of-audio mode disabled while in converter is in PFM		0	R/W	REG_RST
D[4:0]	VINDPM[4:0]	VINDPM[4] 1 = 1600mV	Absolute Input Voltage Limit Offset: 3.9V Range: 3.9V - 5.5V Default: 4.4V (00101) Note: V_{INDPM} > 5.5V (10h) clamped to 5.5V. VINDPM[4:0] register is reset upon adapter plug-in if EN_VINDPM_RST = 1.	0	R/W	REG_RST
		VINDPM[3] 1 = 800mV		0		
		VINDPM[2] 1 = 400mV		1		
		VINDPM[1] 1 = 200mV		0		
		VINDPM[0] 1 = 100mV		1		

REG03: Input Current Limit Register

Register address: 0x03; R/W

PORV = 0x39

Table 10. REG03 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	FORCE_ICO	Force Start Input Current Optimizer (ICO) 0 = Do not force ICO (default) 1 = Force ICO start	Note: This bit can only be set and always returns 0 after ICO starts. This bit only valid when EN_ICO = 1.	0	R/W	REG_RST or Watchdog
D[6]	FORCE_INDET	Force D+/D- Detection 0 = Not in D+/D- detection (default) 1 = Force D+/D- detection		0	R/W	REG_RST or Watchdog
D[5]	EN_ICO	Input Current Optimization (ICO) Algorithm Control 0 = Disable ICO 1 = Enable ICO (default)		1	R/W	REG_RST
D[4:0]	IINDPM[4:0]	IINDPM[4] 1 = 1600mA	Input Current Limit Offset: 500mA Range: 500mA - 3300mA Default: 3000mA (11001) Note: I_{INDPM} > 3300mA (1Ch) clamped to 3300mA. Actual input current limit is lower of I²C or ILIM pin.	1	R/W	REG_RST
		IINDPM[3] 1 = 800mA		1		
		IINDPM[2] 1 = 400mA		0		
		IINDPM[1] 1 = 200mA		0		
		IINDPM[0] 1 = 100mA		1		

REGISTER MAPS (continued)

REG04: Pre-Charge and Termination Current Limit Register

Register address: 0x04; R/W

PORV = 0x22

Table 11. REG04 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:4]	IPRECHG[3:0]	IPRECHG[3] 1 = 400mA	Pre-Charge Current Limit Offset: 50mA Range: 50mA - 800mA Default: 150mA (0010)	0	R/W	REG_RST or Watchdog
		IPRECHG[2] 1 = 200mA		0		
		IPRECHG[1] 1 = 100mA		1		
		IPRECHG[0] 1 = 50mA		0		
D[3:0]	ITERM[3:0]	ITERM[3] 1 = 400mA	Termination Current Limit Offset: 50mA Range: 50mA - 800mA Default: 150mA (0010)	0	R/W	REG_RST or Watchdog
		ITERM[2] 1 = 200mA		0		
		ITERM[1] 1 = 100mA		1		
		ITERM[0] 1 = 5mA		0		

REG05: Charger Control 1 Register

Register address: 0x05; R/W

PORV = 0x9D

Table 12. REG05 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	EN_TERM	Charging Termination Enable 0 = Disable termination 1 = Enable termination (default)		1	R/W	REG_RST or Watchdog
D[6]	Reserved	Reserved	Reserved bit always reads 0.	0	R/W	REG_RST or Watchdog
D[5:4]	WATCHDOG[1:0]	I²C Watchdog Timer Setting 00 = Disable watchdog timer 01 = 40s (default) 10 = 80s 11 = 160s		01	R/W	REG_RST or Watchdog
D[3]	EN_TIMER	Charge Safety Timer Enable 0 = Disable 1 = Enable (default)		1	R/W	REG_RST or Watchdog
D[2:1]	CHG_TIMER[1:0]	Fast Charge Timer Setting 00 = 7.5hrs 01 = 12hrs 10 = 16.5hrs (default) 11 = 21hrs		10	R/W	REG_RST or Watchdog
D[0]	TMR2X_EN	Enable Half Clock Rate Safety Timer 0 = Disable 1 = Safety timer slow down during DPM or thermal regulation (default)	Slow down by a factor of 2.	1	R/W	REG_RST or Watchdog

NOTE: When the WATCHDOG[1:0] bits are changed (writing the same value does not change WATCHDOG[1:0] bit), the internal counter is reset. The same applies for the CHG_TIMER[1:0] bits. Only changing the value in the register will reset the CHG_TIMER[1:0] register.

REGISTER MAPS (continued)

REG06: Charger Control 2 Register

Register address: 0x06; R/W

PORV = 0x7D

Table 13. REG06 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	EN_OTG	Buck (OTG) Mode Control 0 = Disable OTG (default) 1 = Enable OTG	Note: If EN_OTG register and EN_CHG register are set simultaneously, EN_CHG takes priority.	0	R/W	REG_RST or Watchdog
D[6]	AUTO_INDET_EN	Automatic Input Source Detection Enable 0 = Disable D+/D- detection when VBUS plugs in 1 = Enable D+/D- detection when VBUS plugs in (default)		1	R/W	REG_RST or Watchdog
D[5:4]	TREG[1:0]	Thermal Regulation Threshold 00 = 60℃ 01 = 80℃ 10 = 100℃ 11 = 120℃ (default)		11	R/W	REG_RST or Watchdog
D[3]	EN_CHG	Charger Enable Configuration 0 = Charge Disable 1 = Charge Enable (default)	Note: If EN_OTG register and EN_CHG register are set simultaneously, EN_CHG takes priority.	1	R/W	REG_RST or Watchdog
D[2]	BATLOW	Battery Pre-Charge to Fast Charge Threshold 0 = 5.6V 1 = 6.0V (default)		1	R/W	REG_RST or Watchdog
D[1:0]	VRECHG[1:0]	VRECHG[1] 1 = 200mV	Battery Recharge Threshold Offset (below VREG[7:0]) Offset: 100mV Range: 100mV - 400mV Default: 200mV	01	R/W	REG_RST
		VRECHG[0] 1 = 100mV				

REG07: Charger Control 3 Register

Register address: 0x07; R/W

PORV = 0x0A

Table 14. REG07 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	PFM_DIS	Enable PFM Mode 0 = Enable PFM operation (default) 1 = Disable PFM operation		0	R/W	REG_RST
D[6]	WD_RST	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset (bit goes back to 0 after timer reset)		0	R/W	REG_RST or Watchdog
D[5:4]	TOPOFF_TIMER[1:0]	Top-Off Timer 00 = Disabled (default) 01 = 15min 10 = 30min 11 = 45min		00	R/W	REG_RST or Watchdog
D[3:0]	SYS_MIN[3:0]	SYS_MIN[3] 1 = 800mV	Minimum System Voltage Limit Offset: 6.0V Range: 6.0V - 7.5V Default: 7.0V (1010)	1	R/W	REG_RST
		SYS_MIN[2] 1 = 400mV		0		
		SYS_MIN[2] 1 = 200mV		1		
		SYS_MIN[0] 1 = 100mV		0		

REGISTER MAPS (continued)

REG08: Charger Control 4 Register

Register address: 0x08; R/W

PORV = 0x0D

Table 15. REG08 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:6]	BHOT[1:0]	TS Hot Temperature Threshold in OTG Mode 00 = V_{BHOT1} threshold (34.45%) (default) 01 = V_{BHOT0} threshold (37.75%) 10 = V_{BHOT2} threshold (31.35%) 11 = Disable OTG mode thermal protection		00	R/W	REG_RST or Watchdog
D[5]	BCOLD	TS Cold Temperature Threshold in OTG Mode 0 = V_{BCOLD0} threshold (77%) (default) 1 = V_{BCOLD1} threshold (80%)		0	R/W	REG_RST or Watchdog
D[4:3]	JEITA_VSET[1:0] (45℃ - 60℃)	JEITA High Temperature Voltage Setting 00 = Charge suspend 01 = Set V_{REG} to 8.0V (default) 10 = Set V_{REG} to 8.3V 11 = V_{REG} unchanged		01	R/W	REG_RST or Watchdog
D[2]	JEITA_ISETH (45℃ - 60℃)	JEITA High Temperature Current Setting 0 = 40% of I_{CHG} 1 = 100% of I_{CHG} (default)	Percentage with respect to ICHG[5:0] register.	1	R/W	REG_RST or Watchdog
D[1:0]	JEITA_ISETC[1:0] (0℃ - 10℃)	JEITA Low Temperature Current Setting 00 = Charge suspend 01 = 20% of I_{CHG} (default) 10 = 40% of I_{CHG} 11 = 100% of I_{CHG}	Percentage with respect to ICHG[5:0] register.	01	R/W	REG_RST or Watchdog

REG09: OTG Control Register

Register address: 0x09; R/W

PORV = 0xF6

Table 16. REG09 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:4]	OTG_ILIM[3:0]	OTG_ILIM[3] 1 = 800mA	Buck (OTG) Mode Current Limit Offset: 0.5A Range: 0.5A - 2.0A Default: 2A (1111)	1	R/W	REG_RST or Watchdog
		OTG_ILIM[2] 1 = 400mA		1		
		OTG_ILIM[1] 1 = 200mA		1		
		OTG_ILIM[0] 1 = 100mA		1		
D[3:0]	OTG_VLIM[3:0]	OTG_VLIM[3] 1 = 800mV	Buck (OTG) Mode Regulation Voltage Offset: 4.5V Range: 4.5V - 5.5V Default: 5.1V (0110) Note: Values above 5.5V (Ah) will be clamped to 5.5V.	0	R/W	REG_RST or Watchdog
		OTG_VLIM[2] 1 = 400mV		1		
		OTG_VLIM[1] 1 = 200mV		1		
		OTG_VLIM[0] 1 = 100mV		0		

REGISTER MAPS (continued)

REG0A: ICO Current Limit Register

Register address: 0x0A; R

PORV = 0xXX

Table 17. REG0A Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:5]	Reserved	Reserved	Reserved bit always reads 0.	000	R	NA
D[4:0]	ICO_ILIM[4:0]	ICO_ILIM[4] 1 = 1600mA ICO_ILIM[3] 1 = 800mA ICO_ILIM[2] 1 = 400mA ICO_ILIM[1] 1 = 200mA ICO_ILIM[0] 1 = 100mA	Input Current Limit when ICO is Enabled Offset: 500mA Range: 500mA - 3300mA	xxxxx	R	NA

REG0B: Charger Status 1 Register

Register address: 0x0B; R

PORV = 0xXX

Table 18. REG0B Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	ADC_DONE_STAT	ADC Conversion Status (in One-Shot Mode Only) 0 = Conversion not complete 1 = Conversion complete	Note: Always reads 0 in continuous mode.	x	R	NA
D[6]	IINDPM_STAT	Input Current Regulation (Dynamic Power Management) 0 = Not in IINDPM regulation 1 = In IINDPM regulation (ILIM pin or IINDPM[4:0] register)		x	R	NA
D[5]	VINDPM_STAT	Input Voltage Regulation (Dynamic Power Management) 0 = Not in VINDPM regulation 1 = In VINDPM regulation		x	R	NA
D[4]	TREG_STAT	IC Thermal Regulation Status 0 = Normal 1 = In thermal regulation		x	R	NA
D[3]	WD_STAT	I²C Watchdog Timer Status Bit 0 = Normal 1 = Watchdog timer expired		x	R	NA
D[2:0]	CHRG_STAT[2:0]	Charge Status Bits 000 = Not charging 001 = Trickle charge (V_{BAT} < V_{BAT_SHORT}) 010 = Pre-charge (V_{BAT_SHORT} < V_{BAT} < V_{BAT_LOW}) 011 = Fast charge (CC mode) 100 = Taper charge (CV mode) 101 = Top-off timer active charging 110 = Charge termination done 111 = Reserved		xxx	R	NA

REGISTER MAPS (continued)

REG0C: Charger Status 2 Register

Register address: 0x0C; R

PORV = 0xXX

Table 19. REG0C Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	PG_STAT	Input Power Status (VBUS in Good Voltage Range and Not Poor) 0 = Input power source is not good 1 = Input power source is good		x	R	NA
D[6:4]	VBUS_STAT[2:0]	VBUS Status Register 000 = No input 001 = USB host SDP (500mA) 010 = USB CDP (1.5A) 011 = USB DCP (3.0A) 100 = POORSRC detected 7 consecutive times 101 = Unknown adapter (500mA/1000mA) 110 = Non-standard adapter (1A/2A/2.1A/2.4A) 111 = OTG		xxx	R	NA
D[3]	Reserved	Reserved	Reserved bit always reads 0.	0	R	NA
D[2:1]	ICO_STAT[1:0]	Input Current Optimizer (ICO) Status 00 = ICO disabled 01 = ICO optimization is in progress 10 = Maximum input current detected 11 = Reserved		xx	R	NA
D[0]	VSYS_STAT	System Voltage Regulation Status 0 = Not in SYS_MIN regulation (V_{BAT} > V_{SYS_MIN}) 1 = In SYS_MIN regulation (V_{BAT} < V_{SYS_MIN})		x	R	NA

REG0D: NTC Status Register

Register address: 0x0D; R

PORV = 0x0X

Table 20. REG0D Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:3]	Reserved	Reserved	Reserved bit always reads 0.	00000	R	NA
D[2:0]	TS_STAT[2:0]	NTC (TS) Status 000 = Normal 010 = TS warm 011 = TS cool 101 = TS cold 110 = TS hot		xxx	R	NA

REGISTER MAPS (continued)

REG0E: FAULT Status Register

Register address: 0x0E; R

PORV = 0xXX

Table 21. REG0E Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	VBUS_OVP_STAT	Input Over-Voltage Status 0 = Normal 1 = Device in over-voltage protection		x	R	NA
D[6]	TSHUT_STAT	IC Temperature Shutdown Status 0 = Normal 1 = Device in thermal shutdown protection		x	R	NA
D[5]	BATOVP_STAT	Battery Over-Voltage Status 0 = Normal 1 = BATOVP (V_{BAT} > V_{BATOVP})		x	R	NA
D[4]	TMR_STAT	Charge Safety Timer Status 0 = Normal 1 = Charge safety timer expired		x	R	NA
D[3:0]	Reserved	Reserved	Reserved bit always reads 0.	0000	R	NA

REG0F: Charger Flag 1 Register

Register address: 0x0F; R

PORV = 0x00

Table 22. REG0F Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	ADC_DONE_FLAG	ADC Conversion Flag (Only One-Shot Mode) 0 = Conversion not complete (default) 1 = Conversion complete	Note: Always reads 0 in continuous mode.	0	R	REG_RST
D[6]	IINDPM_FLAG	IINDPM Regulation INT Flag 0 = Normal (default) 1 = IINDPM signal rising edge detected		0	R	REG_RST
D[5]	VINDPM_FLAG	VINDPM Regulation INT Flag 0 = Normal (default) 1 = VINDPM signal rising edge detected		0	R	REG_RST
D[4]	TREG_FLAG	IC Temperature Regulation INT Flag 0 = Normal (default) 1 = TREG signal rising edge detected		0	R	REG_RST
D[3]	WD_FLAG	I²C Watchdog INT Flag 0 = Normal (default) 1 = WD_STAT signal rising edge detected		0	R	REG_RST
D[2:1]	Reserved	Reserved	Reserved bit always reads 0.	00	R	REG_RST
D[0]	CHRG_FLAG	Charge Status INT Flag 0 = Normal (default) 1 = CHRG_STAT[2:0] bits changed (transition to any state)		0	R	REG_RST

REGISTER MAPS (continued)

REG10: Charger Flag 2 Register

Register address: 0x10; R

PORV = 0x00

Table 23. REG10 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	PG_FLAG	Power Good INT Flag 0 = Normal (default) 1 = PG signal toggle detected		0	R	REG_RST
D[6:5]	Reserved	Reserved	Reserved bit always reads 0.	00	R	REG_RST
D[4]	VBUS_FLAG	VBUS Status INT Flag 0 = Normal (default) 1 = VBUS_STAT[2:0] bits changed (transition to any state)		0	R	REG_RST
D[3]	Reserved	Reserved	Reserved bit always reads 0.	0	R	REG_RST
D[2]	TS_FLAG	TS Status INT Flag 0 = Normal (default) 1 = TS_STAT[2:0] bits changed (transition to any state)		0	R	REG_RST
D[1]	ICO_FLAG	Input Current Optimizer (ICO) INT Flag 0 = Normal (default) 1 = ICO_STAT[1:0] changed (transition to any state)		0	R	REG_RST
D[0]	VSYS_FLAG	System Voltage Regulation INT Flag 0 = Normal (default) 1 = Entered or exited SYS_MIN regulation		0	R	REG_RST

REG11: FAULT Flag Register

Register address: 0x11; R

PORV = 0x00

Table 24. REG11 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	VBUS_OVP_FLAG	Input Over-Voltage INT Flag 0 = Normal (default) 1 = Entered VBUS_OVP fault		0	R	REG_RST
D[6]	TSHUT_FLAG	IC Temperature Shutdown INT Flag 0 = Normal (default) 1 = Entered TSHUT fault		0	R	REG_RST
D[5]	BATOVP_FLAG	Battery Over-Voltage INT Flag 0 = Normal (default) 1 = Entered BATOVP fault		0	R	REG_RST
D[4]	TMR_FLAG	Charge Safety Timer Fault INT Flag 0 = Normal (default) 1 = Charge safety timer expired rising edge detected		0	R	REG_RST
D[3]	SYS_SHORT_FLAG	System Short INT Flag 0 = Normal (default) 1 = Stopped switching due to boost converter overload		0	R	REG_RST
D[2:1]	Reserved	Reserved	Reserved bit always reads 0.	00	R	REG_RST
D[0]	OTG_FLAG	OTG Buck Mode Fault INT Flag 0 = Normal (default) 1 = VBUS overloaded in OTG, or VBUS OVP, or battery below V_{OTG_BAT}		0	R	REG_RST

REGISTER MAPS (continued)

REG12: Charger Mask 1 Register

Register address: 0x12; R/W

PORV = 0x00

Table 25. REG12 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	ADC_DONE_MASK	ADC Conversion INT Mask Flag (Only One-Shot Mode) 0 = ADC_DONE does produce INT pulse (default) 1 = ADC_DONE does produce not INT pulse		0	R/W	REG_RST
D[6]	IINDPM_MASK	IINDPM Regulation INT Mask 0 = IINDPM entry produces INT pulse (default) 1 = IINDPM entry does not produce INT pulse		0	R/W	REG_RST
D[5]	VINDPM_MASK	VINDPM Regulation INT Mask 0 = VINDPM entry produces INT pulse (default) 1 = VINDPM entry not produce INT pulse		0	R/W	REG_RST
D[4]	TREG_MASK	IC Temperature Regulation INT Mask 0 = TREG entry produces INT pulse (default) 1 = TREG entry produce INT pulse		0	R/W	REG_RST
D[3]	WD_MASK	I²C Watchdog Timer INT Mask 0 = WD_STAT bit rising edge produces INT pulse (default) 1 = WD_STAT bit rising edge does not produce INT		0	R/W	REG_RST
D[2:1]	Reserved	Reserved	Reserved bit always reads 0.	00	R/W	REG_RST
D[0]	CHRG_MASK	Charge Status INT Mask 0 = CHRG_STAT[2:0] bit change produces INT (default) 1 = CHRG_STAT[2:0] bit change does not produce INT pulse		0	R/W	REG_RST

REG13: Charger Mask 2 Register

Register address: 0x13; R/W

PORV = 0x00

Table 26. REG13 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	PG_MASK	Power Good INT Mask 0 = PG toggle produces INT pulse 1 = PG toggle does not produce INT pulse		0	R/W	REG_RST
D[6:5]	Reserved	Reserved	Reserved bit always reads 0.	00	R/W	REG_RST
D[4]	VBUS_MASK	VBUS Status INT Mask 0 = VBUS_STAT[2:0] bit change produces INT 1 = VBUS_STAT[2:0] bit change does not produces INT		0	R/W	REG_RST
D[3]	Reserved	Reserved	Reserved bit always reads 0.	0	R/W	REG_RST
D[2]	TS_MASK	TS Status INT Mask 0 = TS_STAT[2:0] bit change produces INT 1 = TS_STAT[2:0] bit change does not produces INT pulse		0	R/W	REG_RST
D[1]	ICO_MASK	Input Current Optimizer (ICO) INT Mask 0 = ICO_STAT rising edge produces INT 1 = ICO_STAT rising edge does not produce INT		0	R/W	REG_RST
D[0]	VSYS_MASK	System Voltage Regulation INT Mask 0 = Entering or exiting SYS_MIN produces INT 1 = Entering or exiting SYS_MIN does not produce INT		0	R/W	REG_RST

REGISTER MAPS (continued)

REG14: Fault Mask Register

Register address: 0x14; R/W

PORV = 0x00

Table 27. REG14 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	VBUS_OVP_MASK	Input Over-Voltage INT Mask 0 = VBUS_OVP rising edge produces INT pulse 1 = VBUS_OVP rising edge does not produce INT pulse		0	R/W	REG_RST
D[6]	TSHUT_MASK	Thermal Shutdown INT Mask 0 = TSHUT rising edge produces INT pulse 1 = TSHUT rising edge does not produce INT pulse		0	R/W	REG_RST
D[5]	BATOVP_MASK	Battery Over-Voltage INT Mask 0 = BATOVP rising edge produces INT pulse 1 = BATOVP rising edge does not produce INT pulse		0	R/W	REG_RST
D[4]	TMR_MASK	Charge Safety Timer Fault INT Mask 0 = Timer expired rising edge produces INT pulse 1 = Timer expired rising edge does not produce INT pulse		0	R/W	REG_RST
D[3]	SYS_SHORT_MASK	System Short Fault INT Mask 0 = System short rising edge produces INT pulse 1 = System short rising edge does not produce INT pulse		0	R/W	REG_RST
D[2:1]	Reserved	Reserved	Reserved bit always reads 0	00	R/W	REG_RST
D[0]	OTG_MASK	OTG Buck Mode Fault INT Mask 0 = OTG buck mode fault event produces INT 1 = OTG buck mode fault event does not produce INT		0	R/W	REG_RST

REG15: ADC Control Register

Register address: 0x15; R/W

PORV = 0x30

Table 28. REG15 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	ADC_EN	ADC Control 0 = Disable ADC (default) 1 = Enable ADC		0	R/W	REG_RST or Watchdog
D[6]	ADC_RATE	0 = Continuous conversion (default) 1 = One-shot conversion		0	R/W	REG_RST
D[5:4]	ADC_SAMPLE[1:0]	Sample Speed of ADC 00 = 15-bit effective resolution 01 = 14-bit effective resolution 10 = 13-bit effective resolution 11 = 12-bit effective resolution (default)		11	R/W	REG_RST
D[3:0]	Reserved	Reserved	Reserved bit always reads 0.	0000	R/W	REG_RST

REGISTER MAPS (continued)

REG16: ADC Function Disable Register

Register address: 0x16; R/W

PORV = 0x00

Table 29. REG16 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	IBUS_ADC_DIS	0 = Enable conversion 1 = Disable conversion		0	R/W	REG_RST
D[6]	ICHG_ADC_DIS	0 = Enable conversion 1 = Disable conversion		0	R/W	REG_RST
D[5]	VBUS_ADC_DIS	0 = Enable conversion 1 = Disable conversion		0	R/W	REG_RST
D[4]	VBAT_ADC_DIS	0 = Enable conversion 1 = Disable conversion		0	R/W	REG_RST
D[3]	VSYS_ADC_DIS	0 = Enable conversion 1 = Disable conversion		0	R/W	REG_RST
D[2]	TS_ADC_DIS	0 = Enable conversion 1 = Disable conversion		0	R/W	REG_RST
D[1]	Reserved	Reserved	Reserved bit always reads 0	0	R/W	REG_RST
D[0]	TDIE_ADC_DIS	0 = Enable conversion 1 = Disable conversion		0	R/W	REG_RST

REG17: IBUS ADC 1 Register

Register address: 0x17; R

PORV = 0x00

Table 30. REG17 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	IBUS_ADC[15:8]	IBUS_ADC[15]	Sign bit: overall results reported in two's complement.	0	R	REG_RST
		IBUS_ADC[14] 1 = 16384mA		0	R	REG_RST
		IBUS_ADC[13] 1 = 8192mA		0	R	REG_RST
		IBUS_ADC[12] 1 = 4096mA		0	R	REG_RST
		IBUS_ADC[11] 1 = 2048mA	VBUS Current Reading (positive current flows into VBUS pin, negative current flows out of VBUS pin): Range: 0A - 4A	0	R	REG_RST
		IBUS_ADC[10] 1 = 1024mA		0	R	REG_RST
		IBUS_ADC[9] 1 = 512mA		0	R	REG_RST
		IBUS_ADC[8] 1 = 256mA		0	R	REG_RST

REGISTER MAPS (continued)

REG18: IBUS ADC 0 Register

Register address: 0x18; R

PORV = 0x00

Table 31. REG18 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	IBUS_ADC[7:0]	IBUS_ADC[7] 1 = 128mA	VBUS Current Reading (positive current flows into VBUS pin, negative current flows out of VBUS pin): Range: 0A - 4A	0	R	REG_RST
		IBUS_ADC[6] 1 = 64mA		0	R	REG_RST
		IBUS_ADC[5] 1 = 32mA		0	R	REG_RST
		IBUS_ADC[4] 1 = 16mA		0	R	REG_RST
		IBUS_ADC[3] 1 = 8mA		0	R	REG_RST
		IBUS_ADC[2] 1 = 4mA		0	R	REG_RST
		IBUS_ADC[1] 1 = 2mA		0	R	REG_RST
		IBUS_ADC[0] 1 = 1mA		0	R	REG_RST

REG19: ICHG ADC 1 Register

Register address: 0x19; R

PORV = 0x00

Table 32. REG19 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	Reserved	Reserved	Reserved register always reads 0.	0	R	REG_RST
D[6:0]	ICHG_ADC[14:8]	ICHG_ADC[14] 1 = 16384mA		0	R	REG_RST
		ICHG_ADC[13] 1 = 8192mA		0	R	REG_RST
		ICHG_ADC[12] 1 = 4096mA		0	R	REG_RST
		ICHG_ADC[11] 1 = 2048mA	Charge Current Reading Range: 0A - 4A	0	R	REG_RST
		ICHG_ADC[10] 1 = 1024mA		0	R	REG_RST
		ICHG_ADC[9] 1 = 512mA		0	R	REG_RST
		ICHG_ADC[8] 1 = 256mA		0	R	REG_RST

REGISTER MAPS (continued)

REG1A: ICHG ADC 0 Register

Register address: 0x1A; R

PORV = 0x00

Table 33. REG1A Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	ICHG_ADC[7:0]	ICHG_ADC[7] 1 = 128mA	Charge Current Reading Range: 0A - 4A	0	R	REG_RST
		ICHG_ADC[6] 1 = 64mA		0	R	REG_RST
		ICHG_ADC[5] 1 = 32mA		0	R	REG_RST
		ICHG_ADC[4] 1 = 16mA		0	R	REG_RST
		ICHG_ADC[3] 1 = 8mA		0	R	REG_RST
		ICHG_ADC[2] 1 = 4mA		0	R	REG_RST
		ICHG_ADC[1] 1 = 2mA		0	R	REG_RST
		ICHG_ADC[0] 1 = 1mA		0	R	REG_RST

REG1B: VBUS ADC 1 Register

Register address: 0x1B; R

PORV = 0x00

Table 34. REG1B Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	VBUS_ADC[15:8]	VBUS_ADC[15]	Sign bit: overall results reported in two's complement.	0	R	REG_RST
		VBUS_ADC[14] 1 = 16384mV		0	R	REG_RST
		VBUS_ADC[13] 1 = 8192mV	VBUS Voltage Reading Range: 0V - 10V	0	R	REG_RST
		VBUS_ADC[12] 1 = 4096mV		0	R	REG_RST
		VBUS_ADC[11] 1 = 2048mV		0	R	REG_RST
		VBUS_ADC[10] 1 = 1024mV		0	R	REG_RST
		VBUS_ADC[9] 1 = 512mV		0	R	REG_RST
		VBUS_ADC[8] 1 = 256mV		0	R	REG_RST

REGISTER MAPS (continued)

REG1C: VBUS ADC 0 Register

Register address: 0x1C; R

PORV = 0x00

Table 35. REG1C Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	VBUS_ADC[7:0]	VBUS_ADC[7] 1 = 128mV	VBUS Voltage Reading Range: 0V - 10V	0	R	REG_RST
		VBUS_ADC[6] 1 = 64mV		0	R	REG_RST
		VBUS_ADC[5] 1 = 32mV		0	R	REG_RST
		VBUS_ADC[4] 1 = 16mV		0	R	REG_RST
		VBUS_ADC[3] 1 = 8mV		0	R	REG_RST
		VBUS_ADC[2] 1 = 4mV		0	R	REG_RST
		VBUS_ADC[1] 1 = 2mV		0	R	REG_RST
		VBUS_ADC[0] 1 = 1mV		0	R	REG_RST

REG1D: VBAT ADC 1 Register

Register address: 0x1D; R

PORV = 0x00

Table 36. REG1D Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	VBAT_ADC[15:8]	VBAT_ADC[15]	Sign bit: overall results reported in two's complement.	0	R	REG_RST
		VBAT_ADC[14] 1 = 16384mV		0	R	REG_RST
		VBAT_ADC[13] 1 = 8192mV	VBAT Voltage Reading Range: 0V - 10V	0	R	REG_RST
		VBAT_ADC[12] 1 = 4096mV		0	R	REG_RST
		VBAT_ADC[11] 1 = 2048mV		0	R	REG_RST
		VBAT_ADC[10] 1 = 1024mV		0	R	REG_RST
		VBAT_ADC[9] 1 = 512mV		0	R	REG_RST
		VBAT_ADC[8] 1 = 256mV		0	R	REG_RST

REGISTER MAPS (continued)

REG1E: VBAT ADC 0 Register

Register address: 0x1E; R

PORV = 0x00

Table 37. REG1E Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	VBAT_ADC[7:0]	VBAT_ADC[7] 1 = 128mV	VBAT Voltage Reading Range: 0V - 10V	0	R	REG_RST
		VBAT_ADC[6] 1 = 64mV		0	R	REG_RST
		VBAT_ADC[5] 1 = 32mV		0	R	REG_RST
		VBAT_ADC[4] 1 = 16mV		0	R	REG_RST
		VBAT_ADC[3] 1 = 8mV		0	R	REG_RST
		VBAT_ADC[2] 1 = 4mV		0	R	REG_RST
		VBAT_ADC[1] 1 = 2mV		0	R	REG_RST
		VBAT_ADC[0] 1 = 1mV		0	R	REG_RST

REG1F: VSYS ADC 1 Register

Register address: 0x1F; R

PORV = 0x00

Table 38. REG1F Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	VSYS_ADC[15:8]	VSYS_ADC[15]	Sign bit: overall results reported in two's complement.	0	R	REG_RST
		VSYS_ADC[14] 1 = 16384mV		0	R	REG_RST
		VSYS_ADC[13] 1 = 8192mV	VSYS Voltage Reading Range: 0V - 10V	0	R	REG_RST
		VSYS_ADC[12] 1 = 4096mV		0	R	REG_RST
		VSYS_ADC[11] 1 = 2048mV		0	R	REG_RST
		VSYS_ADC[10] 1 = 1024mV		0	R	REG_RST
		VSYS_ADC[9] 1 = 512mV		0	R	REG_RST
		VSYS_ADC[8] 1 = 256mV		0	R	REG_RST

REGISTER MAPS (continued)

REG20: VSYS ADC 0 Register

Register address: 0x20; R

PORV = 0x00

Table 39. REG20 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	VSYS_ADC[7:0]	VSYS_ADC[7] 1 = 128mV	VSYS Voltage Reading Range: 0V - 10V	0	R	REG_RST
		VSYS_ADC[6] 1 = 64mV		0	R	REG_RST
		VSYS_ADC[5] 1 = 32mV		0	R	REG_RST
		VSYS_ADC[4] 1 = 16mV		0	R	REG_RST
		VSYS_ADC[3] 1 = 8mV		0	R	REG_RST
		VSYS_ADC[2] 1 = 4mV		0	R	REG_RST
		VSYS_ADC[1] 1 = 2mV		0	R	REG_RST
		VSYS_ADC[0] 1 = 1mV		0	R	REG_RST

REG21: TS ADC 1 Register

Register address: 0x21; R

PORV = 0x00

Table 40. REG21 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	TS_ADC[15:8]	TS_ADC[15]	Sign bit: overall results reported in two's complement.	0	R	REG_RST
		TS_ADC[14]	TS as Percentage of REGN Reading Range: 0% - 94.9%	0	R	REG_RST
		TS_ADC[13]		0	R	REG_RST
		TS_ADC[12]		0	R	REG_RST
		TS_ADC[11]		0	R	REG_RST
		TS_ADC[10]		0	R	REG_RST
		TS_ADC[9] 1 = 50.0%		0	R	REG_RST
		TS_ADC[8] 1 = 25.0%		0	R	REG_RST

REGISTER MAPS (continued)

REG22: TS ADC 0 Register

Register address: 0x22; R

PORV = 0x00

Table 41. REG22 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	TS_ADC[7:0]	TS_ADC[7] 1 = 12.50%	TS as Percentage of REGN Reading Range: 0% - 94.9%	0	R	REG_RST
		TS_ADC[6] 1 = 6.25%		0	R	REG_RST
		TS_ADC[5] 1 = 3.125%		0	R	REG_RST
		TS_ADC[4] 1 = 1.563%		0	R	REG_RST
		TS_ADC[3] 1 = 0.781%		0	R	REG_RST
		TS_ADC[2] 1 = 0.391%		0	R	REG_RST
		TS_ADC[1] 1 = 0.195%		0	R	REG_RST
		TS_ADC[0] 1 = 0.098%		0	R	REG_RST

REG23: TDIE ADC 1 Register

Register address: 0x23; R

PORV = 0x00

Table 42. REG23 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	Reserved	Reserved	Reserved bit always reads 0.	0	R	REG_RST
	TDIE_ADC[14:8]	TDIE_ADC[14]		0	R	REG_RST
		TDIE_ADC[13]		0	R	REG_RST
		TDIE_ADC[12]		0	R	REG_RST
		TDIE_ADC[11]		0	R	REG_RST
		TDIE_ADC[10]		0	R	REG_RST
		TDIE_ADC[9]		0	R	REG_RST
		TDIE_ADC[8] 1 = 128℃	TDIE (IC Temperature) Reading Range: 0℃ - 128℃	0	R	REG_RST

REGISTER MAPS (continued)

REG24: TDIE ADC 0 Register

Register address: 0x24; R

PORV = 0x00

Table 43. REG24 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	TDIE_ADC[7:0]	TDIE_ADC[7] 1 = 64℃	TDIE (IC Temperature) Reading Range: 0℃ - 128℃	0	R	REG_RST
		TDIE_ADC[6] 1 = 32℃		0	R	REG_RST
		TDIE_ADC[5] 1 = 16℃		0	R	REG_RST
		TDIE_ADC[4] 1 = 8℃		0	R	REG_RST
		TDIE_ADC[3] 1 = 4℃		0	R	REG_RST
		TDIE_ADC[2] 1 = 2℃		0	R	REG_RST
		TDIE_ADC[1] 1 = 1℃		0	R	REG_RST
		TDIE_ADC[0] 1 = 0.5℃		0	R	REG_RST

REG25: Part Information Register

Register address: 0x25; R/W

PORV = 0x00

Table 44. REG25 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	REG_RST	Register Reset 0 = No effect (keep current register settings) 1 = Reset R/W bits of all registers to the default and reset safety timer (It also resets itself to 0 after register reset is completed.)		0	R	REG_RST
D[6:3]	PN[3:0]	Part ID 0000 = SGM41528		0000	R	REG_RST
D[2:0]	DEV_REV[2:0]	Revision: 000		000	R	REG_RST

APPLICATION INFORMATION

A typical application consists of the device configured as an I²C controlled power path management device and a 2-cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. It integrates an input blocking FET (QBLK, Q1), high-side switching FET (QHS, Q2), low-side switching FET (QLS, Q3), and battery FET (QBAT, Q4) between system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

Detailed Design Procedure

Inductor Selection

The device has 1.5MHz switching frequency to allow the use of small inductor and capacitor values. The inductor saturation current should be higher than the input current (I_{IN}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} > I_{IN} + \frac{I_{RIPPLE}}{2} \quad (5)$$

The inductor ripple current (I_{RIPPLE}) depends on input voltage (V_{VBUS}), duty cycle (D = V_{BAT}/V_{VBUS}), switching frequency (f_{SW}) and inductance (L):

$$I_{RIPPLE} = \frac{V_{VBUS} \times (V_{SYS} - V_{VBUS})}{V_{SYS} \times f_{SW} \times L} \quad (6)$$

The maximum inductor ripple current happens in the vicinity of D = 0.5. Usually inductor ripple is designed in the range of (20% - 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Input (VBUS/PMID) Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current occurs when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current IPMID occurs where the duty cycle is closest to 50% and can be estimated by

$$I_{PMID} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (7)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for up to 5V input voltage. 10μF capacitor is suggested for up to 3.3A input current.

Output (VSYS) Capacitor

SYS capacitor is the boost converter output capacitor and should also have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{CSYS} = I_{IN} \times \sqrt{\frac{V_{SYS}}{V_{VBUS}} - \frac{V_{SYS}^2}{V_{VBUS}^2}} \quad (8)$$

The output capacitor voltage ripple is a function of the boost output current (I_{OUT}), and can be calculated as follows:

$$\Delta V_{SYS} = \frac{I_{OUT} \times D}{f_{SW} \times C_{SYS}} \quad (9)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for SYS decoupling capacitor and should be placed close to the SYS and GND pins of the IC. Voltage rating of the capacitor must be higher than normal output voltage level. 16V rating or higher capacitor is preferred. 40μF capacitor is suggested for up to 2.2A boost converter output current.

APPLICATION INFORMATION (continued)

Input Power Supply Considerations

To power the system from the SGM41528, either an input power source with a voltage between 3.9V to 6.2V and at least 500mA current rating should power VBUS, or a 2-cell Li-Ion battery with voltage higher than V_{BAT_UVLO} should be connected to BAT pin of the device. The input source must have at least 3.3A current rating to allow maximum power delivery through charger (boost converter) to the system.

Layout Guidelines

The switching node (SW) creates very high frequency noises several times higher than f_{SW} (1.5MHz) due to sharp rise and fall times of the voltage and current in the switches. To reduce the ringing issues and noise generation designing a proper layout is important to minimize the current path impedance and loop area. The following considerations can help making a better layout.

1. Place SYS and BAT output capacitor as close to SYS, BAT and GND bumps as possible. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.

2. Place the input capacitor between PMID and GND pins as close as possible to the chip with shortest copper connections (avoid vias). Choose the smallest capacitor size.

3. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area connected to the SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

4. Place output capacitor GND pin as close as possible to the GND pin of the device and the GND pin of input capacitor C_{IN}. It is better to avoid using vias for these connections and keep the high frequency current paths very short and on the same layer. A GND copper layer under the component layer helps reducing noise emissions. Pay attention to the DC current and AC current paths in the layout and keep them short and decoupled as much as possible.

5. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin). Alternatively a 0Ω resistor can be used to tie analog ground to power ground to keep them as separate nets.

6. Place decoupling capacitors close to the IC pins with shortest possible copper connections.

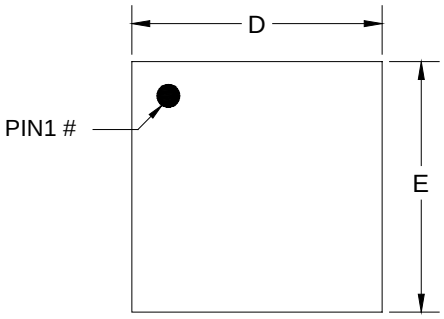
7. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

8. Select proper sizes for the vias and ensure enough copper is available to carry the current for a given current path. Vias usually have some considerable parasitic inductance and resistance.

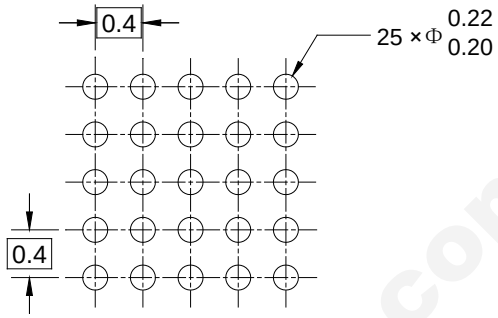
9. Route BATP and BATN away from switching nodes such as SW.

PACKAGE OUTLINE DIMENSIONS

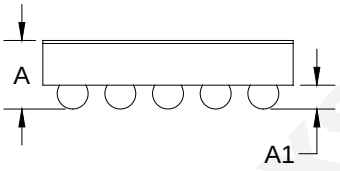
WLCSP-2.1×2.1-25B



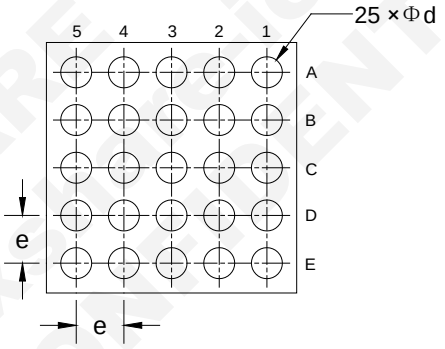
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



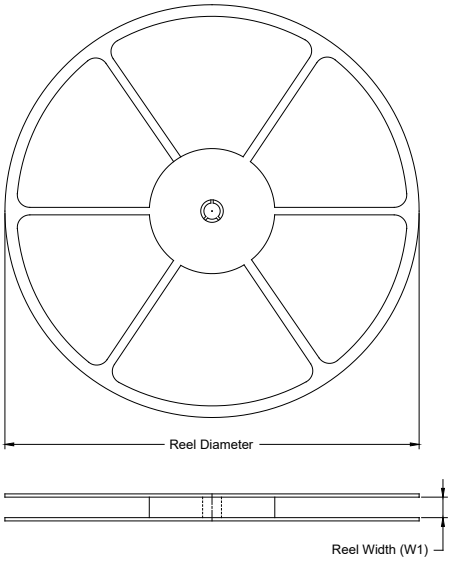
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.525	0.575	0.625
A1	0.180	0.200	0.220
D	2.070	2.100	2.130
E	2.070	2.100	2.130
d	0.230	0.260	0.290
e	0.400 BSC		

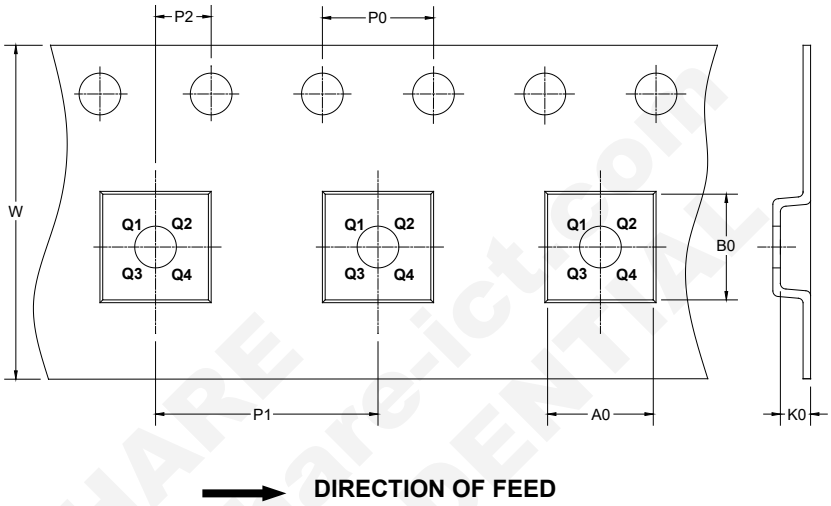
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



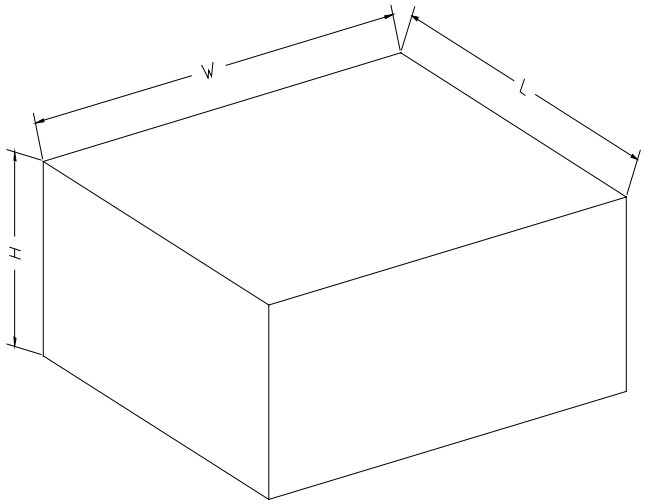
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.1×2.1-25B	7″	9.0	2.24	2.24	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002