



# SGM3851A Triple-Output AMOLED Display Power Supply

## GENERAL DESCRIPTION

The SGM3851A is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring  $V_{AVDD}$ ,  $V_{ELVDD}$  and  $V_{ELVSS}$ . The device integrates a boost converter for  $V_{ELVDD}$ , an inverting buck-boost converter for  $V_{ELVSS}$  and a boost converter for  $V_{AVDD}$ , which are suitable for battery operated products. The digital interface control pin (CTRL) allows programming  $V_{AVDD}$ ,  $V_{ELVDD}$  and  $V_{ELVSS}$  in digital steps.

The SGM3851A is available in Green TQFN-3×3-16L package. It operates over an ambient temperature range of -40°C to +85°C.

## FEATURES

- 2.9V to 4.5V Input Voltage Range
- Synchronous Boost Converter (AVDD)
  - ◆ 5.8V to 7.9V Output Voltage (Programmable)
  - ◆ 6.1V Default Output Voltage
  - ◆ 1% Accuracy
  - ◆ 80mA Output Current Capability
  - ◆  $V_{IN}$  to  $V_{OUT}$  and  $V_{OUT}$  to  $V_{IN}$  Isolation
- Synchronous Boost Converter (ELVDD)
  - ◆ 4.6V to 5.0V Output Voltage (Programmable)
  - ◆ 4.6V Default Output voltage
- ◆ 0.5% Accuracy
- ◆ 400mA Output Current Capability
- ◆ External Output Voltage Sensing Pin for Load Drop Compensation
- ◆  $V_{IN}$  to  $V_{OUT}$  and  $V_{OUT}$  to  $V_{IN}$  Isolation
- Synchronous Inverting Buck-Boost Converter (ELVSS)
  - ◆ -5.4V to -1.4V Output Voltage (Programmable)
  - ◆ -2.5V Default Output Voltage
  - ◆ 1.2% Accuracy at -2.5V ( $\pm 30$ mV)
  - ◆ 400mA Output Current Capability
  - ◆  $V_{IN}$  to  $V_{OUT}$  and  $V_{OUT}$  to  $V_{IN}$  Isolation
- Short Circuit Protection
- Thermal Shutdown
- $V_{ELVSS}$  Start-Up Delay: 10ms
- Short Circuit and OLP Detect Time: 1ms
- Available in Green TQFN-3×3-16L Package

## APPLICATIONS

Smartphones  
 Small Size Tablets  
 Active Matrix OLED Displays  $\leq 8''$

## TYPICAL APPLICATION

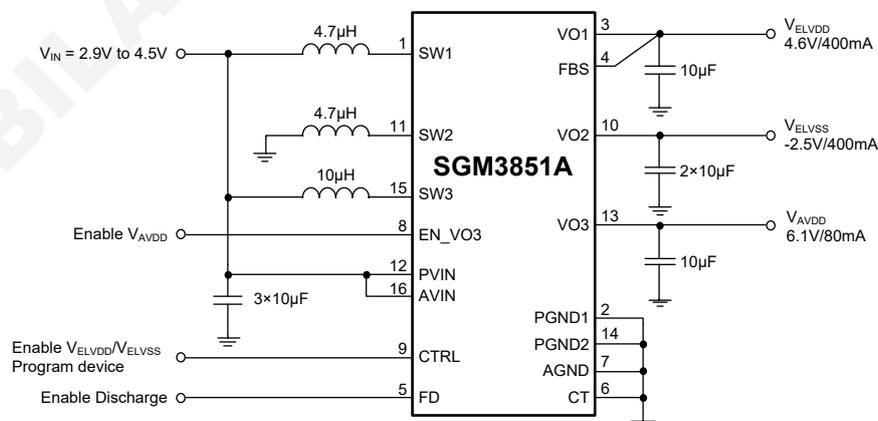


Figure 1. Typical Application Circuit

**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3851A	TQFN-3×3-16L	-40°C to +85°C	SGM3851AYTQ16G/TR	3851ATQ XXXXX	Tape and Reel, 4000

NOTE: XXXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

PVIN, AVIN, EN\_VO3, CTRL, CT, FD, SW1, VO1, FBS Voltages <sup>(1)</sup>..... -0.3V to 6V  
 SW3, VO3 Voltages <sup>(1)</sup>..... -0.3V to 10V  
 VO2 Voltage <sup>(1)</sup>..... -6.5V to 0.3V  
 SW2 Voltage <sup>(1)</sup>..... -6.5V to 5.5V  
 Package Thermal Resistance  
 TQFN-3×3-16L,  $\theta_{JA}$ ..... 45°C/W  
 Junction Temperature..... +150°C  
 Storage Temperature Range..... -65°C to +150°C  
 Lead Temperature (Soldering, 10s)..... +260°C

**RECOMMENDED OPERATING CONDITIONS**

Operating Ambient Temperature Range ..... -40°C to +85°C  
 Operating Junction Temperature Range ..... -40°C to +125°C

NOTE:

1. All voltages are with respect to network ground pin.

**OVERSTRESS CAUTION**

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

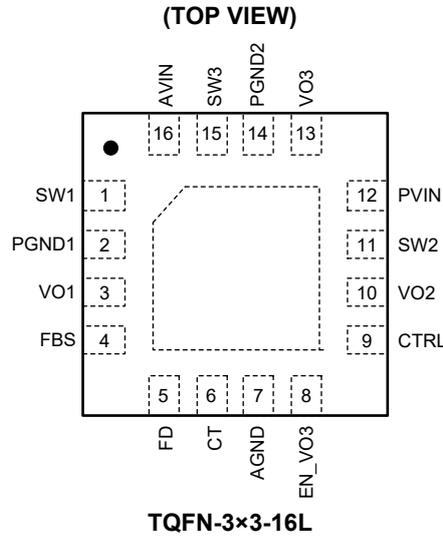
**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	SW1	O	Switch Pin of The ELVDD Boost Converter.
2	PGND1	—	Power Ground of The ELVDD Boost Converter.
3	VO1	O	Output of The ELVDD Boost Converter.
4	FBS	I	ELVDD Sense Input.
5	FD	I	Active Discharge Enable/Disable During Shutdown.
6	CT	I/O	Control of The ELVSS Transition Time.
7	AGND	—	Analog Ground.
8	EN_VO3	I	Enable AVDD Boost Converter.
9	CTRL	I	Enable ELVDD Boost Converter and Delayed ELVSS Inverting Buck-Boost Converter. Digital programming.
10	VO2	O	Output of The ELVSS Inverting Buck-Boost Converter.
11	SW2	O	Switch Pin of The ELVSS Inverting Buck-Boost Converter.
12	PVIN	—	Supply for ELVSS Inverting Buck-Boost Converter.
13	VO3	O	Output of The AVDD Boost Converter.
14	PGND2	—	Power Ground of The AVDD Boost Converter.
15	SW3	O	Switch Pin of The AVDD Boost Converter.
16	AVIN	—	Supply for The Internal Analog Circuits.
Exposed Pad		—	Connect this pad to AGND, PGND1 and PGND2.

NOTE: I: input; O: output; I/O: input or output.

## ELECTRICAL CHARACTERISTICS

(At  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ ,  $V_{CTRL} = V_{EN\_VO3} = V_{IN}$ ,  $V_{ELVDD} = 4.6\text{V}$ ,  $V_{ELVSS} = -2.5\text{V}$ ,  $V_{AVDD} = 6.1\text{V}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY CURRENT AND THERMAL PROTECTION</b>						
Input Voltage Range	$V_{IN}$		2.9		4.5	V
Shutdown Current into $V_{IN}$	$I_{SD}$	$V_{CTRL} = V_{EN\_VO3} = \text{GND}$ , $V_{FD} = \text{GND}$ or $V_{FD} = 3.7\text{V}$		0.3		$\mu\text{A}$
Under-Voltage Lockout Threshold (AVIN)	$V_{IT-}$	$V_{IN}$ falling		2.2		V
	$V_{IT+}$	$V_{IN}$ rising		2.3		
Thermal Shutdown Temperature		Junction temperature rising		135		$^\circ\text{C}$
Thermal Shutdown Hysteresis		Junction temperature falling		10		$^\circ\text{C}$
<b>LOGIC SIGNALS (EN_VO3, CTRL, FD)</b>						
High Level Input Voltage	$V_H$	$V_{IN} = 2.9\text{V}$ to $4.5\text{V}$	1.3			V
Low Level Input Voltage	$V_L$	$V_{IN} = 2.9\text{V}$ to $4.5\text{V}$			0.3	V
Pull-Down Resistor (EN_VO3, CTRL)	$R_{DOWN}$			540		k $\Omega$
<b>BOOST CONVERTER (<math>V_{VO1} = V_{ELVDD}</math>)</b>						
Positive Output 1 Voltage	$V_{VO1}$		4.6	4.6	5.0	V
Positive Output 1 Voltage Variation		No load $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , no load		$\pm 0.5$ $\pm 0.8$		
SW1 MOSFET On-Resistance	$R_{DS(ON)1}$	$I_{DS} = 100\text{mA}$		170		m $\Omega$
SW1 MOSFET Rectifier On-Resistance	$R_{DS(ON)2}$	$I_{DS} = 100\text{mA}$		300		m $\Omega$
SW1 Switch Current Limit	$I_{SW1}$	Inductor valley current		1		A
SW1 Switching Frequency	$f_{SW1}$	$I_{VO1} = 100\text{mA}$		1.5		MHz
Short Circuit Threshold in Operation	$V_{VO1(SCP)}$	Percentage of nominal $V_{VO1}$		90		%
Threshold of Output Sense with VO1	$V_{TVO1}$	$V_{VO1} - V_{FBS}$ increasing		300		mV
Threshold of Output Sense with FBS	$V_{TFBS}$	$V_{VO1} - V_{FBS}$ decreasing		200		mV
VO1 and FBS Leakage, No Discharge	$I_{LEAK\_VO1}$	$V_{FD} = V_{CTRL} = \text{GND}$		1.2		$\mu\text{A}$
Pull-Down Resistance of FBS	$R_{FBS}$			4		M $\Omega$
VO1 Discharge Resistance	$R_{VO1(DCG)}$	$V_{CTRL} = \text{GND}$ , $I_{VO1} = 1\text{mA}$		30		$\Omega$
Line Regulation		$I_{VO1} = 100\text{mA}$ , $V_{IN} = 2.9\text{V}$ to $4.5\text{V}$		0.007		%/V
Load Regulation		$1\text{mA} \leq I_{VO1} \leq 400\text{mA}$		0.27		%/A
<b>BUCK-BOOST CONVERTER (<math>V_{VO2} = V_{ELVSS}</math>)</b>						
Negative Output Voltage Range	$V_{VO2}$		-5.4	-2.5	-1.4	V
Negative Output Voltage Regulation		No load		$\pm 30$		mV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , no load		$\pm 50$		
SW2 MOSFET On-Resistance	$R_{DS(ON)3}$	$I_{DS} = 100\text{mA}$		230		m $\Omega$
SW2 MOSFET Rectifier On-Resistance	$R_{DS(ON)4}$	$I_{DS} = 100\text{mA}$		280		m $\Omega$
SW2 Switch Current Limit	$I_{SW2}$	Inductor peak current		1.8		A
SW2 Switching Frequency	$f_{SW2}$	$I_{VO2} = 100\text{mA}$		1.5		MHz
Short Circuit Threshold in Operation	$V_{VO2(SCP)}$	Voltage rise from nominal $V_{VO2}$		500		mV
VO2 Negative Comparator at Start-Up				-700		mV
VO2 Leakage, No Discharge	$I_{LEAK\_VO2}$	$V_{FD} = V_{CTRL} = \text{GND}$		0.2		$\mu\text{A}$
VO2 Discharge Resistance	$R_{VO2(DCG)}$	$V_{CTRL} = \text{GND}$ , $I_{VO2} = 1\text{mA}$		150		$\Omega$
CT Pin Output Impedance	$R_{CT}$			300		k $\Omega$
CT Pin Comparator	Comp <sub>CT</sub>	$V_{CT}$ rising		50		mV
Line Regulation		$I_{VO2} = 100\text{mA}$ , $V_{IN} = 2.9\text{V}$ to $4.5\text{V}$		0.003		%/V
Load Regulation		$1\text{mA} \leq I_{VO2} \leq 400\text{mA}$		0.37		%/A

**ELECTRICAL CHARACTERISTICS (continued)**

(At  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ ,  $V_{CTRL} = V_{EN\_VO3} = V_{IN}$ ,  $V_{ELVDD} = 4.6\text{V}$ ,  $V_{ELVSS} = -2.5\text{V}$ ,  $V_{AVDD} = 6.1\text{V}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BOOST CONVERTER (<math>V_{VO3} = V_{AVDD}</math>)</b>						
Positive Output 2 Voltage	$V_{VO3}$		5.8	6.1	7.9	V
Positive Output 2 Voltage Regulation		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , No load		$\pm 1$		%
SW3 MOSFET On-Resistance	$R_{DS(ON)5}$	$I_{DS} = 100\text{mA}$		500		m $\Omega$
SW3 MOSFET Rectifier On-Resistance	$R_{DS(ON)6}$	$I_{DS} = 100\text{mA}$		900		m $\Omega$
SW3 Switch Current Limit	$I_{SW3}$	Inductor peak current		0.4		A
SW3 Switching Frequency	$f_{SW3}$	$I_{VO3} = 30\text{mA}$		1.5		MHz
Output Current Sensing	$I_{OUT}$			100		mA
Short Circuit Threshold in Operation	$V_{VO3(SCP)}$	Percentage of nominal $V_{VO3}$		90		%
VO3 Leakage, No Discharge	$I_{LEAK\_VO3}$	$V_{FD} = V_{EN\_VO3} = \text{GND}$		1.6		$\mu\text{A}$
VO3 Discharge Resistance	$R_{VO3(DCG)}$	$V_{CTRL} = \text{GND}$ , $I_{VO3} = 1\text{mA}$		30		$\Omega$
Line Regulation		$I_{VO3} = 30\text{mA}$ , $V_{IN} = 2.9\text{V}$ to $4.5\text{V}$		0.013		%/V
Load Regulation		$1\text{mA} \leq I_{VO3} \leq 80\text{mA}$		0.4		%/A

**TIMING REQUIREMENTS**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
<b>SHORT-CIRCUIT TIMER</b>					
VO1 Short Circuit Detection Time in Start-Up	$t_{VO1(SCP)}$		10		ms
VO1 Short Circuit Detection Time in Operation			1		
VO2 Short Circuit Detection Time in Start-Up	$t_{VO2(SCP)}$		10		
VO2 Short Circuit Detection Time in Operation			1		
VO3 Short Circuit Detection Time in Operation	$t_{VO3(SCP)}$		1		
VO3 Overload Detection Delay	$t_{D(OVERLOAD)}$		1		
VO2 Discharge Time after CTRL Goes High	$t_{D(DISCHARGE)}$		10		
<b>CTRL INTERFACE</b>					
Initialization Time	$t_{INIT}$		300		$\mu\text{s}$
Shutdown Time Period	$t_{OFF}$		55		
Pulse High Level Time Period	$t_{HIGH}$		10		
Pulse Low Level Time Period	$t_{LOW}$		10		
Data Storage/Accept Time Period	$t_{STORE}$		55		

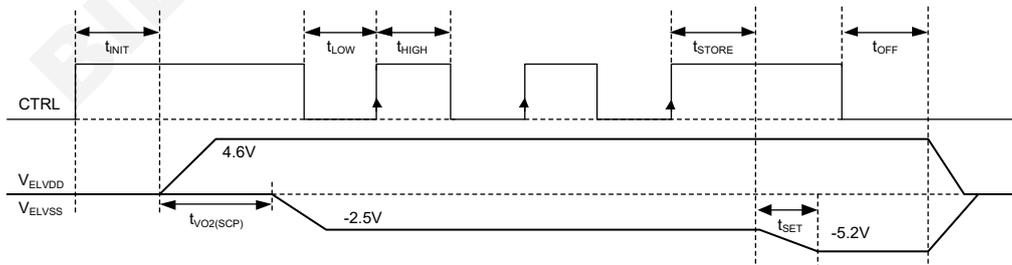
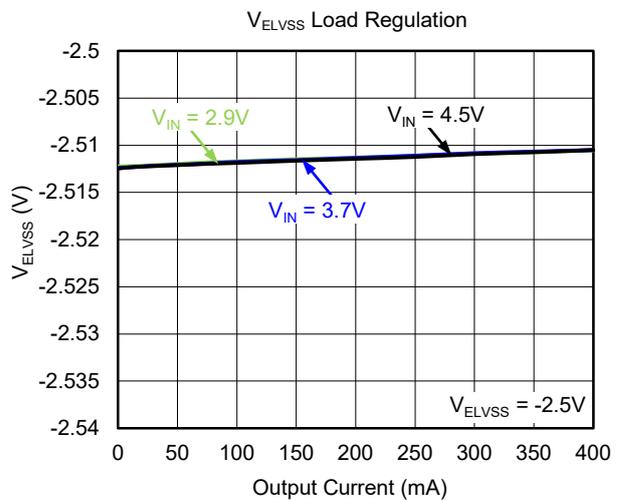
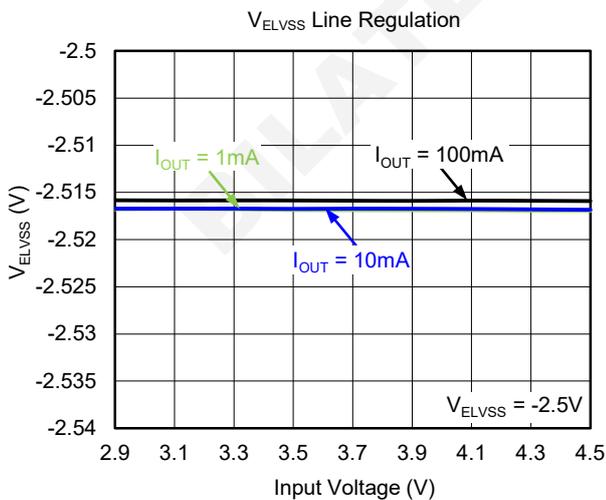
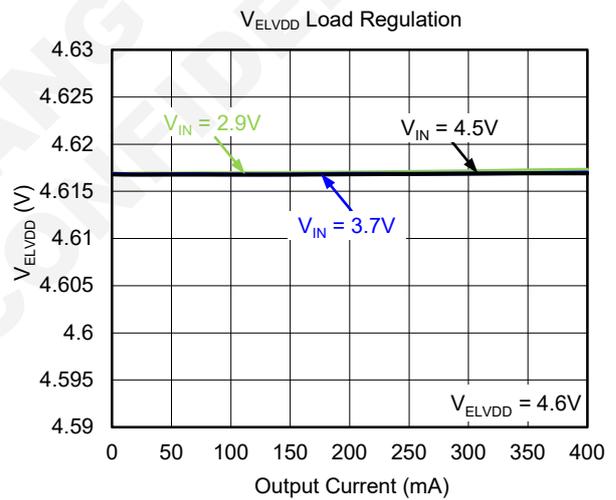
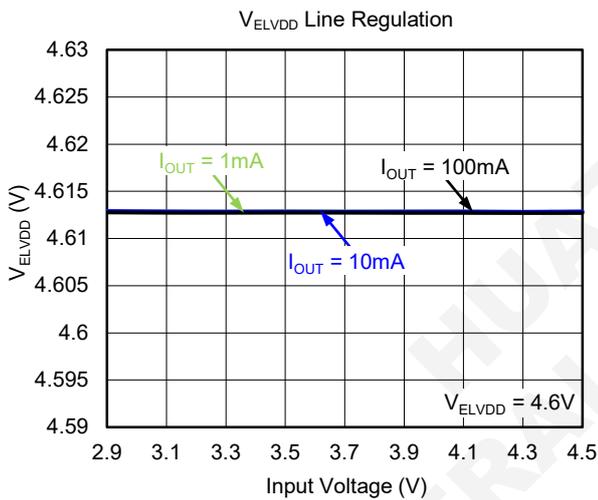
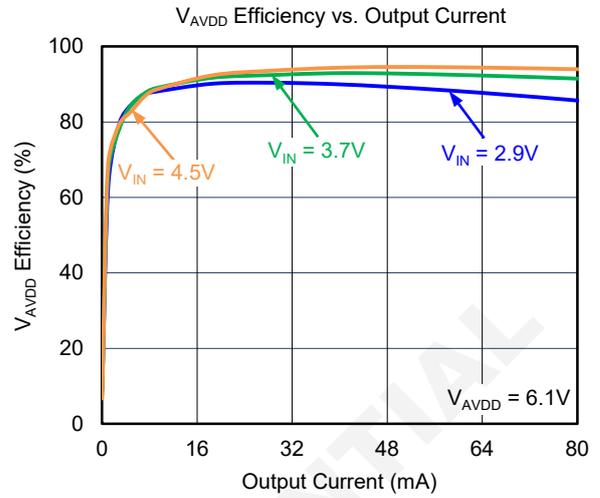
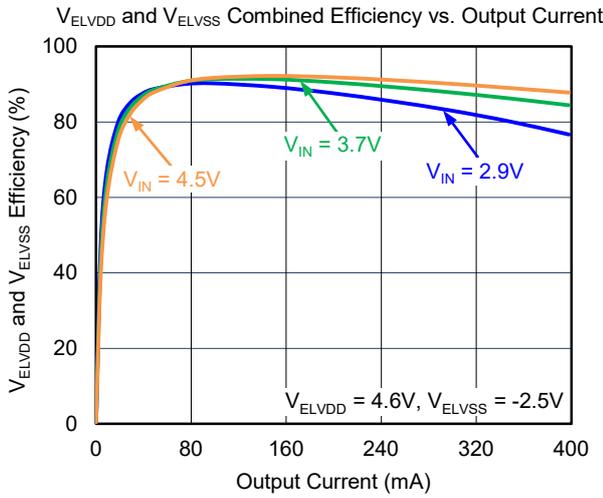


Figure 2. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

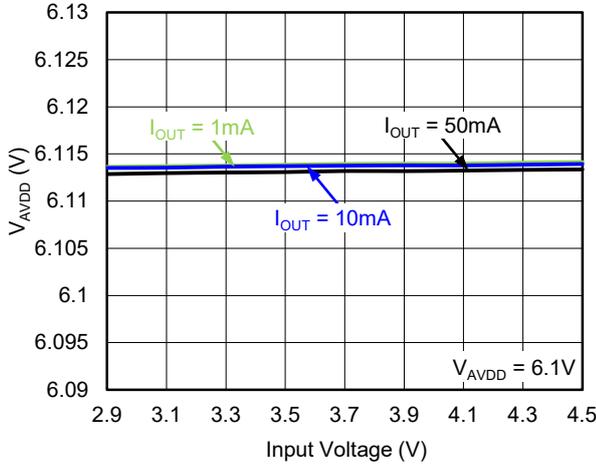
At  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ , unless otherwise noted.



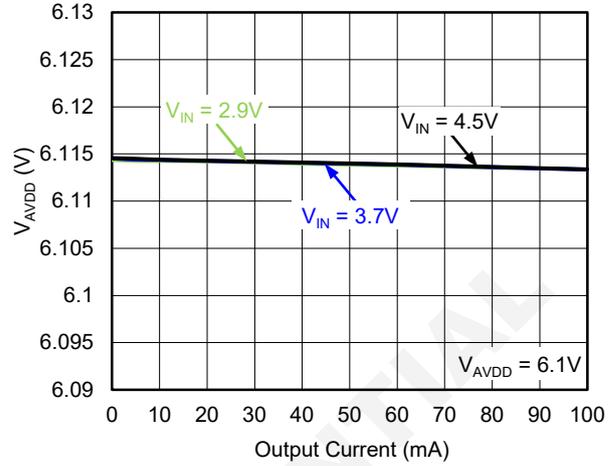
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ , unless otherwise noted.

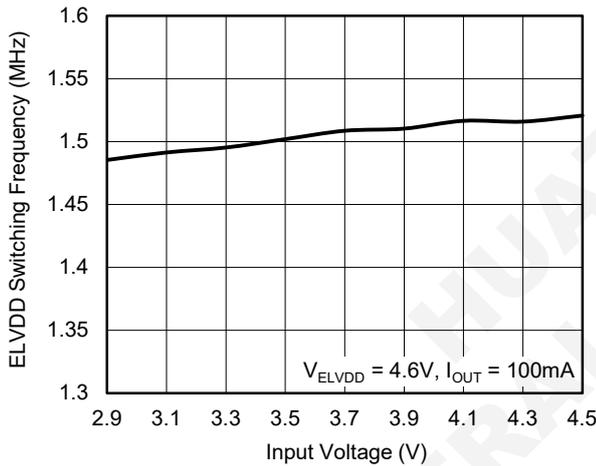
$V_{AVDD}$  Line Regulation



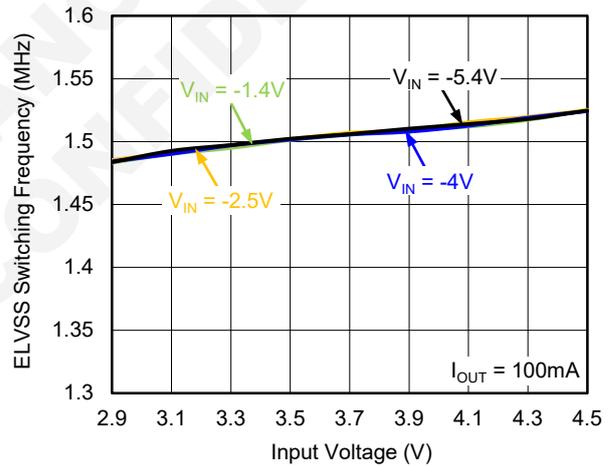
$V_{AVDD}$  Load Regulation



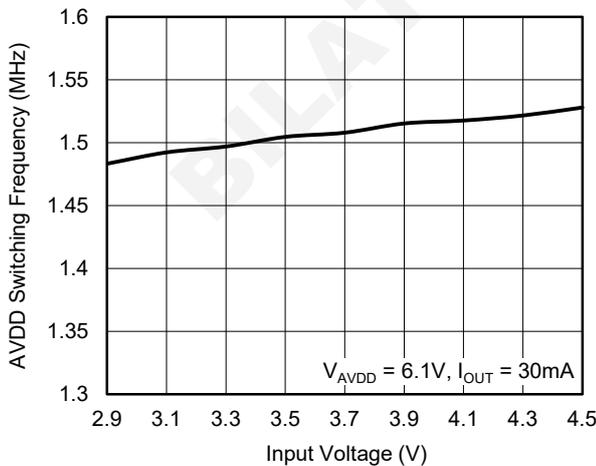
ELVDD Converter Switching Frequency



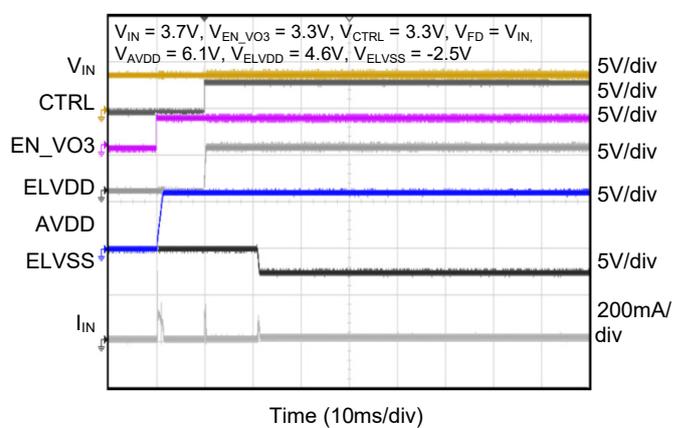
ELVSS Converter Switching Frequency



AVDD Converter Switching Frequency

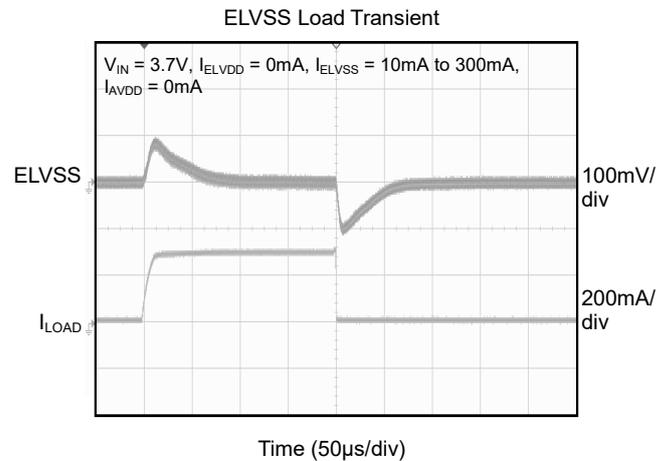
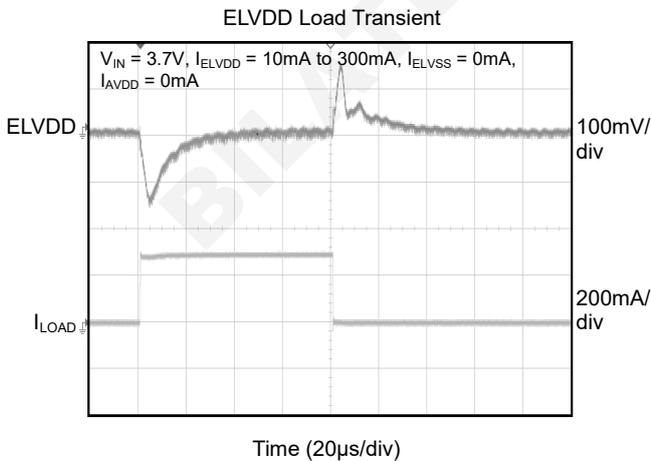
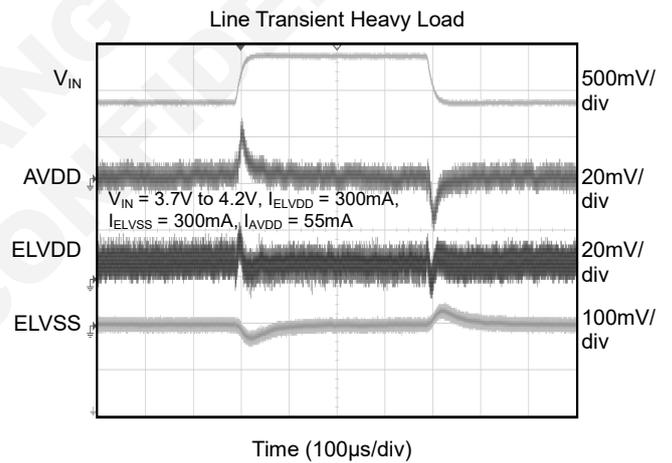
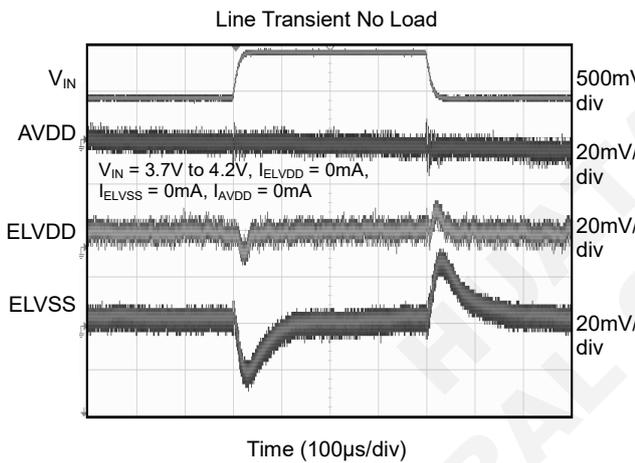
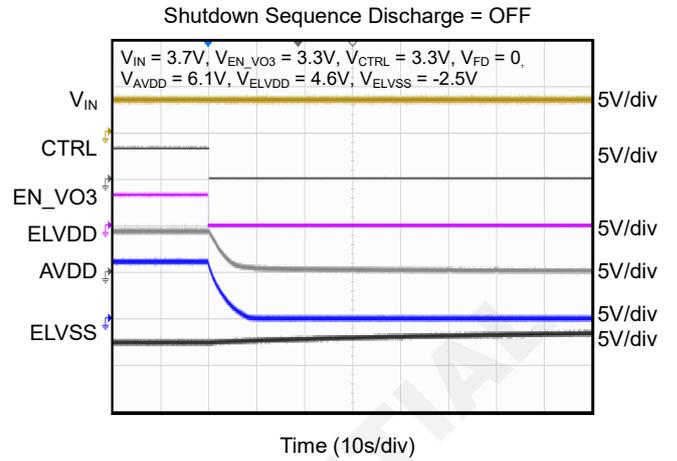
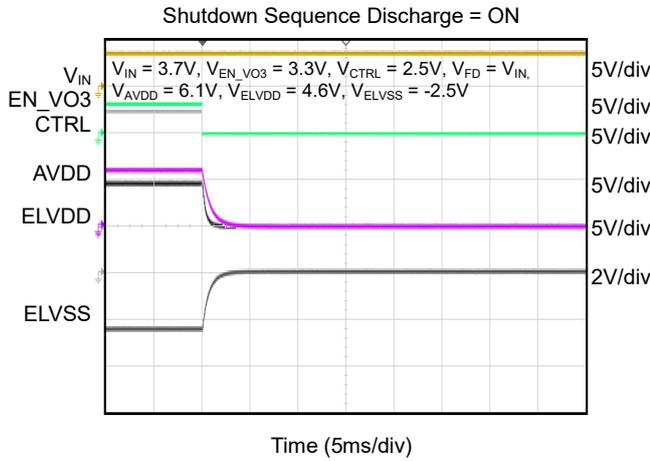


Startup Sequence



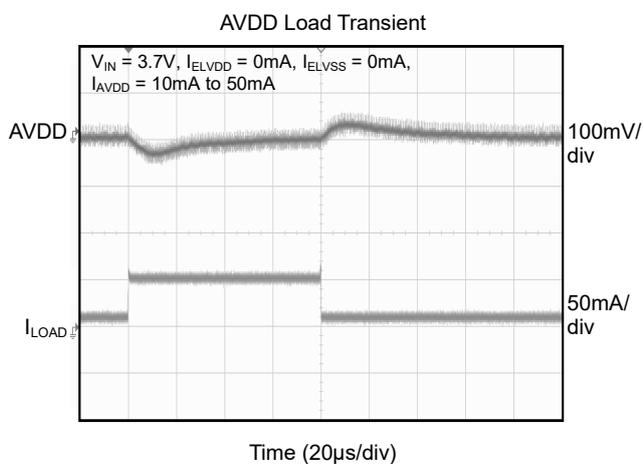
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ , unless otherwise noted.



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.7\text{V}$ , unless otherwise noted.



HUATANG  
BILATERAL CONFIDENTIAL

FUNCTIONAL BLOCK DIAGRAM

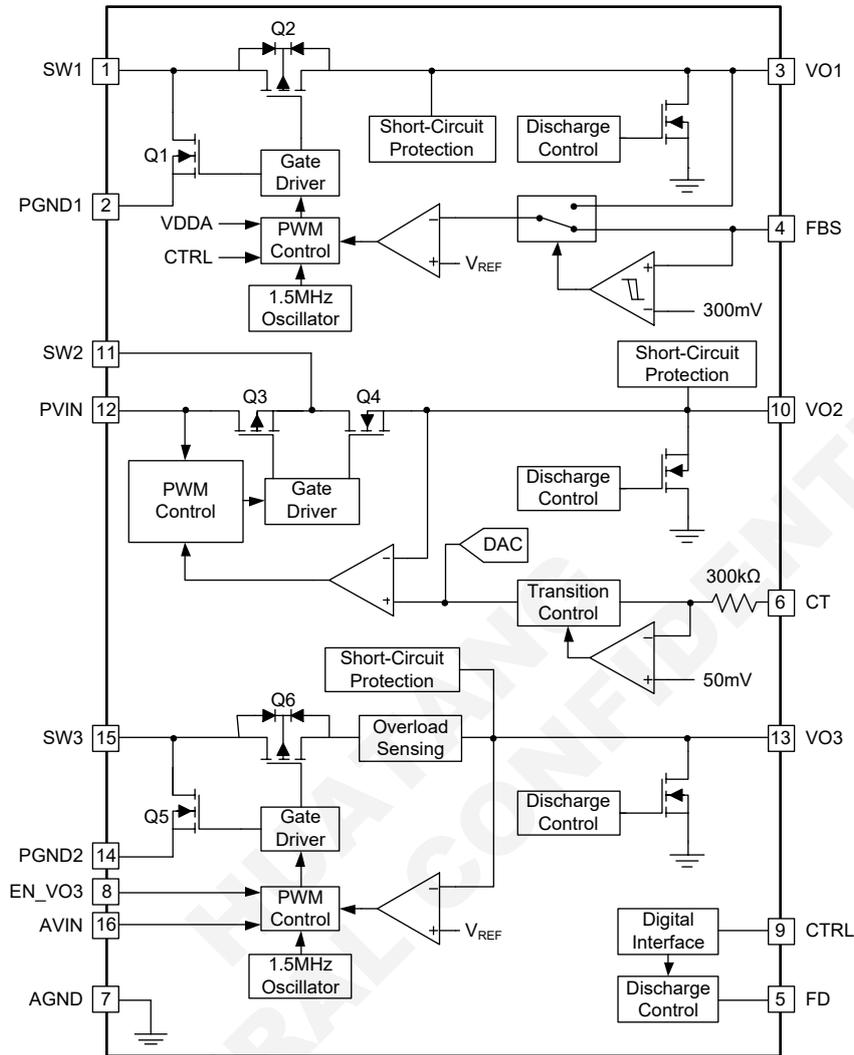


Figure 3. SGM3851A Functional Block Diagram

## DETAILED DESCRIPTION

The SGM3851A consists of two boost converters and an inverting buck-boost converter.  $V_{ELVDD}$  is programmable in the range of 4.6V to 5V (default = 4.6V).  $V_{ELVSS}$  is programmable in the range of -1.4V to -5.4V (default = -2.5V) and  $V_{AVDD}$  is programmable between 5.8V and 7.9V (default = 6.1V). The transition time when  $V_{ELVSS}$  is programmed to a different voltage is adjustable by the CT pin capacitor.

### Under-Voltage Lockout

The device has a built-in under-voltage lockout function that disables the device when the input supply voltage is too low for normal operation.

### Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once a temperature of typically +135°C is exceeded the device shuts down (the programming is not lost). When the temperature decreases to typically +125°C the device automatically restarts performing the start-up sequencing with the same voltages and programming as programmed before the thermal shutdown.

### ELVDD Boost Converter (VO1)

The ELVDD boost converter uses a fixed-frequency valley-current-mode topology. The output voltage  $V_{ELVDD}$  is adjustable between 4.6V and 5.0V with a default voltage of 4.6V (see Table 1). In shutdown its output is fully isolated (input to output and output to input).

For the highest output voltage accuracy, connect the output sense pin (FBS) directly to the positive pin of the output capacitor. If not used, the FBS pin can be left floating or connected to ground, then the output voltage is sensed at the VO1 pin.

### ELVSS Inverting Buck-Boost Converter (VO2)

The ELVSS inverting buck-boost converter uses a fixed-frequency peak-current-mode topology. The output voltage  $V_{ELVSS}$  is adjustable between -5.4V and -1.4V with a default voltage of -2.5V (see Table 1). In shutdown its output is fully isolated (input to output and output to input).

### AVDD Boost Converter (VO3)

The AVDD boost converter uses a fixed-frequency peak-current-mode topology. The output voltage  $V_{AVDD}$  is adjustable between 5.8V and 7.9V with a default voltage of 6.1V (see Table 1). In shutdown its output is fully isolated (input to output and output to input).

### Start-Up Sequence, Soft-Start and Shut-Down

The device has an implemented soft-start which limits the inrush current. When  $V_{IN}$  is applied, the output discharge is undefined until the rising edge of CTRL sets the output discharge to follow the FD pin setting. When the converters are disabled all outputs are discharged if FD = high or high impedance if FD = low. The typical start-up sequence is shown in Figure 4.

- Pulling EN\_VO3 high starts the AVDD boost converter.  $V_{AVDD}$  follows a linear 1.5ms long voltage ramp until it reaches its default value of 6.1V, then the switch current is limited to typical 0.2A.
- Pulling CTRL high starts the ELVDD boost converter.  $V_{ELVDD}$  starts with a reduced switch current limit of 0.2A until it reaches its default voltage of 4.6V, then the full current limit is released.
- 10ms after CTRL is pulled high the ELVSS inverting buck-boost converter starts.  $V_{ELVSS}$  starts with a reduced switch current limit of 0.4A until it reaches its default voltage of -2.5V, then the full current limit is released.

DETAILED DESCRIPTION (continued)

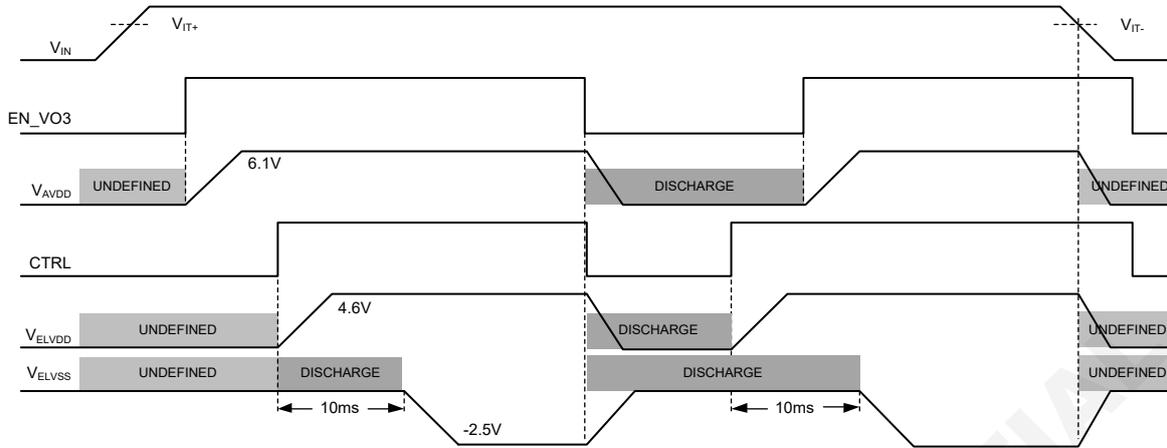


Figure 4. SGM3851A Start-Up Sequencing Active Discharge Enabled

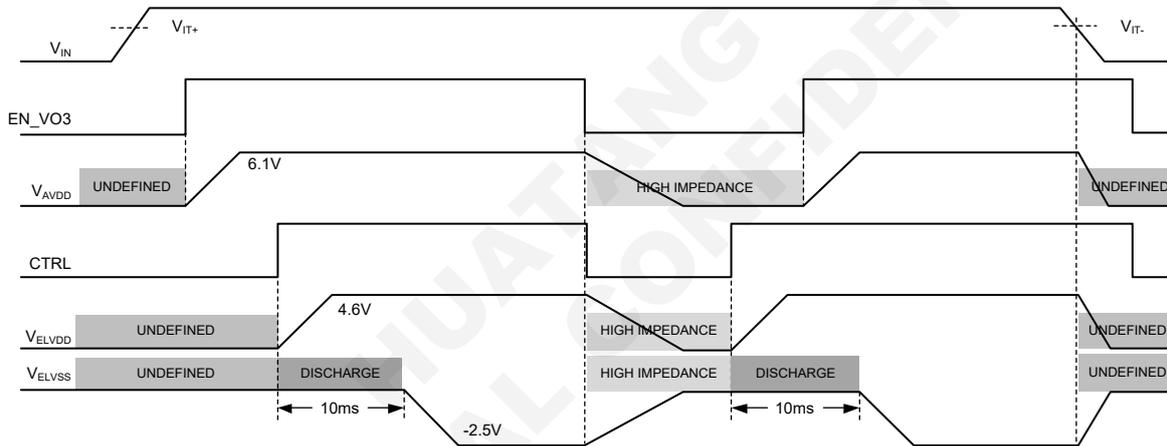


Figure 5. SGM3851A Start-Up Sequencing Active Discharge Disabled

**VELVSS Transition Time Control (CT Pin)**

The transition time is the time required to move VELVSS from the actual voltage level to the new programmed voltage level. The transition time can be controlled by an external capacitor connected to the CT pin. The typical 50mV CT pin comparator detects when the CT pin is connected to GND or floating, then the fastest possible transition time is used. When a capacitor is

connected the R-C time constant  $\tau$  sets the transition time. The output voltage is almost settled after  $3\tau$ , which means 95% of the target voltage is reached.

$$\begin{aligned} \tau &= \text{Internal CT resistance} \times \text{external capacitor} \\ &= R_{CT} \times C_{CT} \\ &= 300k\Omega \times 100nF \\ &= 30ms \end{aligned} \tag{1}$$



Figure 6. VELVSS Transition Time Control

DETAILED DESCRIPTION (continued)

Digital Interface (CTRL Pin)

The digital interface allows programming of the positive output voltages  $V_{AVDD}$ ,  $V_{ELVDD}$  and the negative output voltage  $V_{ELVSS}$  in discrete steps. By default the output discharge during shutdown is controlled by the FD pin, the setting can be overwritten by programming when FD is Low. If programming is not required the CTRL pin

can also be used as a standard enable pin. Once the device is enabled the device starts with its default values (blue marked values in Table 1). The interface counts the rising edges applied to the CTRL pin and sets the new values as shown in Table 1. The settings are stored in a volatile memory. The reset behavior is described in the device reset section.

Table 1. Programming Table

Rising Edges	$V_{ELVSS}$	Rising Edges	$V_{ELVSS}$	Rising Edges	$V_{AVDD}$	Rising Edges	Outputs Discharge	Rising Edges	$V_{ELVSS}$ Transition Time	Rising Edges	$V_{ELVDD}$
0/no pulse	-2.5V	21	-3.4V	0/no pulse	6.1V	0/no pulse	controlled by FD pin	0/no pulse	controlled by CT pin	0/no pulse	4.6V
1	-5.4V	22	-3.3V	42	7.9V	50	ON	52	reserved	54	4.7V
2	-5.3V	23	-3.2V	43	7.6V	51	OFF	53	reserved	55	4.8V
3	-5.2V	24	-3.1V	44	7.3V					56	4.9V
4	-5.1V	25	-3.0V	45	7.0V					57	5.0V
5	-5.0V	26	-2.9V	46	6.7V						
6	-4.9V	27	-2.8V	47	6.4V						
7	-4.8V	28	-2.7V	48	6.1V						
8	-4.7V	29	-2.6V	49	5.8V						
9	-4.6V	30	-2.5V								
10	-4.5V	31	-2.4V								
11	-4.4V	32	-2.3V								
12	-4.3V	33	-2.2V								
13	-4.2V	34	-2.1V								
14	-4.1V	35	-2.0V								
15	-4.0V	36	-1.9V								
16	-3.9V	37	-1.8V								
17	-3.8V	38	-1.7V								
18	-3.7V	39	-1.6V								
19	-3.6V	40	-1.5V								
20	-3.5V	41	-1.4V								

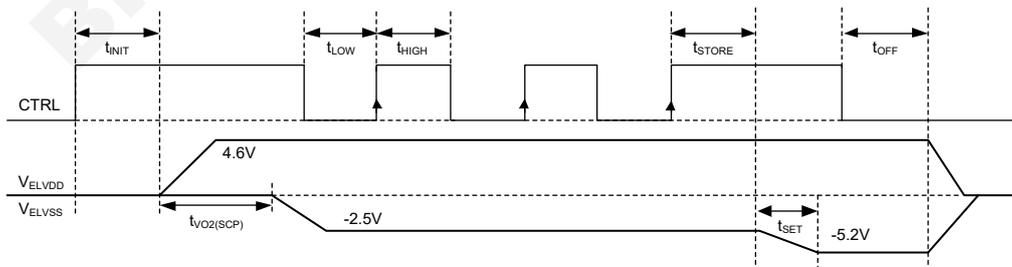


Figure 7. Programming  $V_{ELVSS}$

## DETAILED DESCRIPTION (continued)

### Short Circuit and Overload Protection

The device is protected against short of  $V_{AVDD}$ ,  $V_{ELVDD}$  and  $V_{ELVSS}$  to ground.  $V_{ELVDD}$  and  $V_{ELVSS}$  are also protected when they are shorted together. A short at any converter and the  $V_{AVDD}$  overload protection shuts down the whole device, the shut-down state is latched, and input and outputs are fully disconnected. To reset the whole device  $V_{IN}$  has to cycle below under-voltage lockout or EN\_VO3 and CTRL have to be low at the same time for minimum  $t_{OFF}$ . The device detects a short or an overload when one of the below conditions is fulfilled:

- $V_{ELVDD}$  is not in regulation 10ms after  $V_{ELVDD}$  is enabled (10ms CTRL = high) → shut-down all
- $V_{ELVSS}$  is not in regulation 10ms after  $V_{ELVSS}$  is enabled (20ms after CTRL = high) → shut-down all
- $V_{(AVDD)}$  protection is enabled when the soft-start is completed.

During Operation:

- $V_{AVDD}$  falls below 90% of its programmed voltage longer than 1ms → shut-down all
- $V_{ELVDD}$  falls below 90% of its programmed voltage longer than 1ms → shut-down all
- $V_{ELVSS}$  rises above 500mV of its programmed voltage longer than 1ms → shut-down all

### Enable/Disable Active Discharge During Shutdown

The active discharge during shutdown can be enabled and disabled by the FD pin or by programming. The

programming overwrites the FD pin setting until the function is reset.

- FD pin connected to GND or 51 CTRL pulses → Active discharge is disabled and all outputs are high impedance.
- FD pin connected to HIGH ( $V_{IH} > 1.3V$ ) or 50 CTRL pulses → Active discharge is enabled and all outputs are discharged.

### Device Reset

- A power cycle resets all settings to default values as well as the short-circuit protection.
- Enabling the  $V_{ELVDD}$  converter (first rising edge of CTRL) resets the output discharge → Output discharge is controlled by FD pin.
- When CTRL is low for  $t_{OFF}$  then  $V_{ELVSS}$  is reset to default value → -2.5V.
- EN\_VO3 and CTRL are low at the same time for  $t_{OFF}$  → Short circuit protection is reset.

### Operation with $V_{IN} < 2.9V$

The recommended minimum input supply voltage for full performance is 2.9V. The device continues to operate with input supply voltages below 2.9V, however, full performance is not ensured. The device does not operate with input supply voltages below the under-voltage Lockout threshold.

## APPLICATION INFORMATION

Figure 1 shows a typical application circuit suitable for supplying AMOLED displays in smartphone applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates positive output voltages  $V_{AVDD}$  of 6.1V and  $V_{ELVDD}$  of 4.6V as well as a negative output voltage  $V_{ELVSS}$  of -2.5V. ELVDD and ELVSS are capable of supplying up to 400mA of output current.

For this design example, use the following input parameters in Table 2.

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	2.9V to 4.5V
Output Voltage	$V_{AVDD} = 6.1V$ , $V_{ELVDD} = 4.6V$ , $V_{ELVSS} = -2.5V$
Switching Frequency	ELVDD, ELVSS and AVDD = 1.5MHz

In order to maximize performance, the device has been optimized for use with a relatively narrow range of component values. The  $V_{AVDD}$  boost converter typically requires a 10 $\mu$ H inductor,  $V_{ELVDD}$  and  $V_{ELVSS}$  require a 4.7 $\mu$ H inductor. Ceramic capacitors are usually used for input and output capacitors. It is recommended to use the suggested values in all applications. Customers using other values are strongly recommended to characterize circuit performance on a case-by-case basis.

### ELVDD Boost Converter (VO1)

#### Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an

influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.5MHz) the lower the core losses. Table 3 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3 $\mu$ H, maximum 6.1 $\mu$ H inductance.
- Minimum 0.5A saturation current, for full output current capability 1.3A.
- Minimum  $V_{IN}$  and maximum  $I_{OUT}$  must be taken to calculate the required saturation current.
- Duty Cycle:

$$D = \frac{V_{OUT} - V_{IN} \times \eta}{V_{OUT}}$$

where

$V_{IN}$  is the boost converter input supply voltage.

$V_{OUT}$  is the boost converter output voltage.

$\eta$  is the boost converter efficiency

- Peak Inductor Current:

$$I_{(SW)M} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times f \times L}$$

where

$I_{OUT}$  is the boost converter output current.

$f = 1.5\text{MHz}$  (the boost converter switching frequency).

$L$  is the boost converter inductance (4.7 $\mu$ H).

#### Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Table 4 and Table 5 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5 $\mu$ F resulting capacitance.
- Minimum 6.3V voltage rating.

Output Capacitor:

- Minimum 2.5 $\mu$ F, maximum 24 $\mu$ F resulting capacitance.
- Minimum 6.3V voltage rating.

## APPLICATION INFORMATION (continued)

Table 3. ELVDD Boost Converter (VO1) Inductor Selection

INDUCTANCE	I <sub>SAT</sub>	DCR	MANUFACTURER	PART NUMBER	DIMENSIONS
4.7μH	1.9A	200mΩ	TOKO	DFE252012C-4R7M	2.5mm × 2.0mm × 1.2mm
	2.2A	165mΩ	TOKO	DFE252012P-4R7M	2.5mm × 2.0mm × 1.2mm
	1.5A	175mΩ	ALPS	GLCLM4R701A	2.5mm × 2.0mm × 1.2mm
	1.5A	230mΩ	ALPS	GLCLK4R701A	2.5mm × 2.0mm × 1mm

Table 4. Input Capacitor Selection ELVDD Boost Converter (VO1)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10μF	6.3V	Murata	GRM188R60J106ME84	0603
10μF	10V	Murata	GRM219R61A106ME47	0805
22μF	10V	Samsung	CL21A226MPCLRNC	0805

Table 5. Output Capacitor Selection ELVDD Boost Converter (VO1)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10μF	10V	Murata	GRM219R61A106ME47	0805
22μF	10V	Samsung	CL21A226MPCLRNC	0805

## ELVSS Inverting Buck-Boost Converter (VO2)

## Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.5MHz) the lower the core losses. Table 6 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3μH, maximum 6.1μH inductance.
- Minimum 0.5A saturation current, for full output current capability 1.5A.

- Minimum V<sub>IN</sub> and maximum I<sub>O</sub> must be taken to calculate the required saturation current.

- Duty Cycle:

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN} \times \eta}$$

where

V<sub>IN</sub> is the inverting buck-boost converter input supply voltage.

V<sub>OUT</sub> is the inverting buck-boost converter output voltage.

η is the inverting buck-boost converter efficiency.

- Peak Inductor Current:

$$I_{(SW)M} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times f \times L}$$

where

I<sub>OUT</sub> is the inverting buck-boost converter output current.

f = 1.5MHz (the inverting buck-boost converter switching frequency).

L is the inverting buck-boost converter inductance (4.7μH).

## APPLICATION INFORMATION (continued)

**Capacitor Selection**

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Table 7 and Table 8 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5 $\mu$ F resulting capacitance.
- Minimum 6.3V voltage rating.

Output Capacitor:

- Minimum 2.5 $\mu$ F, maximum 24 $\mu$ F resulting capacitance.
- Minimum 10V voltage rating, when maximum -6V are used also 6.3V rated capacitors can be used.

Table 6. ELVSS Inverting Buck-Boost Converter (VO2) Inductor Selection

INDUCTANCE	I <sub>SAT</sub>	DCR	MANUFACTURER	PART NUMBER	DIMENSIONS
4.7 $\mu$ H	1.9A	200m $\Omega$	TOKO	DFE252012C-4R7M	2.5mm $\times$ 2.0mm $\times$ 1.2mm
	2.2A	165m $\Omega$	TOKO	DFE252012P-4R7M	2.5mm $\times$ 2.0mm $\times$ 1.2mm
	1.5A	175m $\Omega$	ALPS	GLCLM4R701A	2.5mm $\times$ 2.0mm $\times$ 1.2mm
	1.5A	230m $\Omega$	ALPS	GLCLK4R701A	2.5mm $\times$ 2.0mm $\times$ 1mm

Table 7. Input Capacitor Selection ELVSS Inverting Buck-Boost Converter (VO2)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10 $\mu$ F	6.3V	Murata	GRM188R60J106ME84	0603
10 $\mu$ F	10V	Murata	GRM219R61A106ME47	0805
22 $\mu$ F	10V	Samsung	CL21A226MPCLRNC	0805

Table 8. Output Capacitor Selection ELVSS Inverting Buck-Boost Converter (VO2)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10 $\mu$ F	10V	Murata	GRM219R61A106ME47	0805
22 $\mu$ F	10V	Samsung	CL21A226MPCLRNC	0805

**AVDD Boost Converter (VO3)****Inductor Selection**

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.2A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality

factor Q of the inductor at the switching frequency (1.5MHz) the lower the core losses. Table 9 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 7 $\mu$ H, maximum 13 $\mu$ H inductance.
- Minimum 0.2A saturation current, for full output current capability 0.25A.
- Minimum V<sub>IN</sub> and maximum I<sub>O</sub> must be taken to calculate the required saturation current.
- Duty Cycle:

$$D = \frac{V_{OUT} - V_{IN} \times \eta}{V_{OUT}}$$

Where

V<sub>IN</sub> is the boost converter input supply voltage.

V<sub>OUT</sub> is the boost converter output voltage.

$\eta$  is the boost converter efficiency

## APPLICATION INFORMATION (continued)

- Peak Inductor Current:

$$I_{(SW)M} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times f \times L}$$

Where

$I_{OUT}$  is the boost converter output current.

$f = 1.5\text{MHz}$  (the boost converter switching frequency).

$L$  is the boost converter inductance ( $10\mu\text{H}$ )

#### Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and

AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Table 10 and Table 11 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum  $2.5\mu\text{F}$  resulting capacitance.
- Minimum 6.3V voltage rating.

Output Capacitor:

- Minimum  $2.5\mu\text{F}$ , maximum  $24\mu\text{F}$  resulting capacitance.
- Minimum 10V voltage rating .

Table 9. AVDD Boost Converter (VO3) Inductor Selection

INDUCTANCE	$I_{SAT}$	DCR	MANUFACTURER	PART NUMBER	DIMENSIONS
10 $\mu\text{H}$	1.3A	400m $\Omega$	TOKO	DFE252012C-100M	2.5mm × 2.0mm × 1.2mm
	1.2A	530m $\Omega$	TOKO	DFE252010C-100M	2.5mm × 2.0mm × 1mm
	0.75A	600m $\Omega$	Taiyo Yuden	MDKK2020T-100MM	2mm × 2mm × 1mm
	0.8A	359m $\Omega$	CYNTEC	SDET25201B-100MS	2.5mm × 2mm × 1.2mm
	0.48A	817m $\Omega$	CYNTEC	SDER20121T-100MS	2.0mm × 1.2mm × 1mm

Table 10. Input Capacitor Selection AVDD Boost Converter (VO3)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10 $\mu\text{F}$	6.3V	Murata	GRM188R60J106ME84	0603
10 $\mu\text{F}$	10V	Murata	GRM219R61A106ME47	0805
22 $\mu\text{F}$	10V	Samsung	CL21A226MPCLRNC	0805

Table 11. Output Capacitor Selection AVDD Boost Converter (VO3)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
10 $\mu\text{F}$	10V	Murata	GRM219R61A106ME47	0805
22 $\mu\text{F}$	10V	Samsung	CL21A226MPCLRNC	0805

## APPLICATION INFORMATION (continued)

### Power Supply Recommendations

The SGM3851A device is designed to operate with input supplies from 2.9V to 4.5V. The input supply should be stable and free of noise if the device's full performance is to be achieved. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance may be required. The input capacitance shown in the Application Information is sufficient for typical applications.

### Layout Guideline

The PCB layout is an important step in the power supply design. An incorrect layout could cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching DC/DC converter at high load currents, too thin PCB traces can cause significant voltage spikes. Good grounding becomes important as well. If possible a common

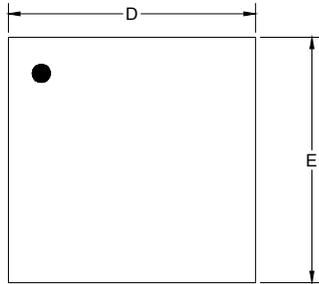
ground plane to minimize ground shifts between analog ground (GND) and power ground (PGND) is recommended.

- Place the input capacitor on PVIN and the output capacitor on VO2 as close as possible to the device. Use short and wide traces to connect the input capacitor on PVIN and the output capacitor on VO2.
- Place the output capacitor on VO1 and VO3 as close as possible to the device. Use short and wide traces to connect the output capacitor on VO1 and VO3.
- Connect the ground of the CT capacitor with AGND (pin 7) directly.
- Connect input ground and output ground on the same board layer, not through via hole.
- Connect AGND, PGND1 and PGND2 with the exposed thermal pad.

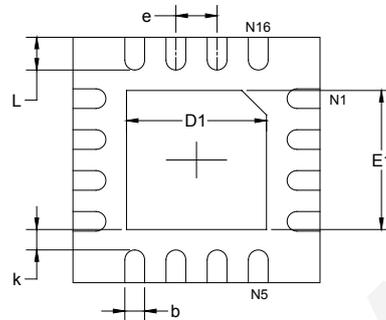
# PACKAGE INFORMATION

## PACKAGE OUTLINE DIMENSIONS

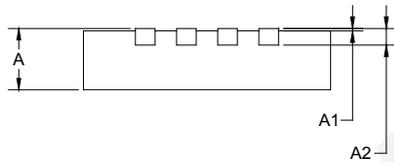
### TQFN-3×3-16L



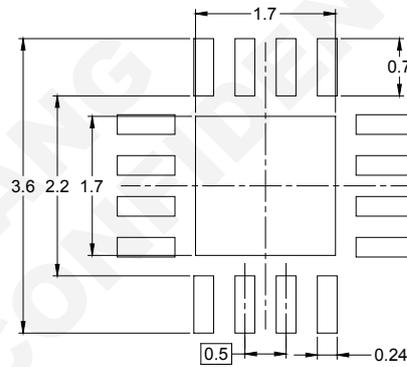
TOP VIEW



BOTTOM VIEW



SIDE VIEW



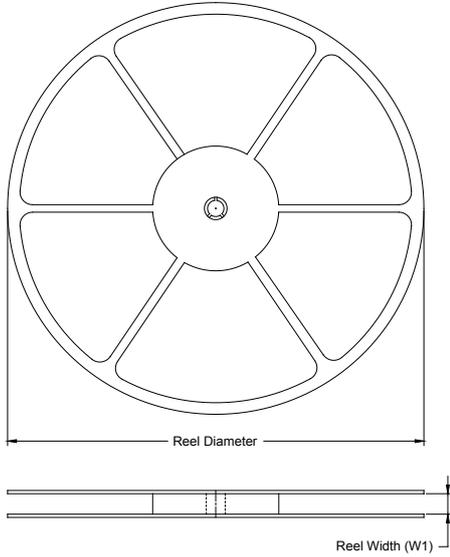
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

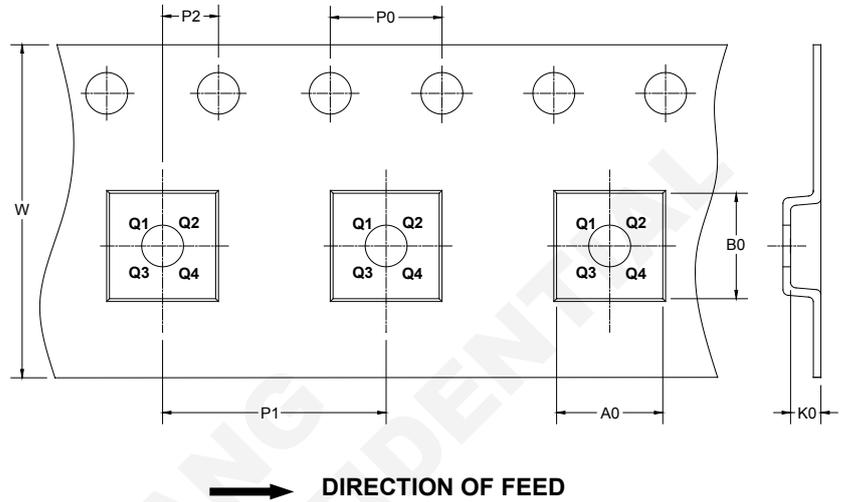
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

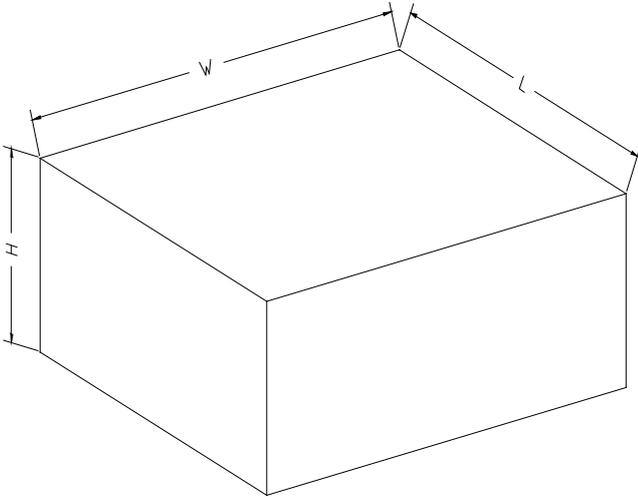
### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002