SGM3804
Single Inductor, Positive/Negative Dual Output, Buck/Boost Converter

GENERAL DESCRIPTION

The SGM3804 generates both positive and negative precision regulated voltage power sources, with a patent pending control scheme for single inductor dual output converter. Outputs are programmable in 100mV steps in 2.4V to 6.4V range, which are commonly used in drivers for LCD displays and AMOLED displays, as well as in any other circuits requiring both rails, with different loading on each rail. The device is equipped with I^2C interface. With input in the range of 2.7V to 5.5V, the device is optimized for loading 100mA in boost-inverter mode and also works in buck-inverter mode.

The SGM3804 is available in green WLCSP-1.7×1.51-12B package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Single Inductor for Positive & Negative Outputs**
- **High Efficiency in Wide Output Loading Range**
- **Outputs Programmable with I^2C Interface**
- **2.4V to 6.4V Programmable for Both Outputs**
- **Factory Programmable Default Outputs:**
  - **SGM3804-0: V_{PO} = +5.4V/V_{NO} = -5.4V**
  - **SGM3804-1: V_{PO} = +4.6V/V_{NO} = -3.5V**
  - **SGM3804-2: V_{PO} = +5.0V/V_{NO} = -5.0V**
  - **SGM3804-3: V_{PO} = +4.6V/V_{NO} = -2.4V**
  - **SGM3804-4: V_{PO} = +6.4V/V_{NO} = -6.4V**
- **1.6MHz Switching plus Pulse-Skip Operation**
- **Configurable Stop Active Discharge**
- **Slim Package Fits into *65132 Footprint**

APPLICATIONS

AMOLED/LCD Smart-Phones/Pads/Media-Players
Wearable Device Display/Audio
AFE with Positive & Negative Rails

TYPICAL APPLICATION

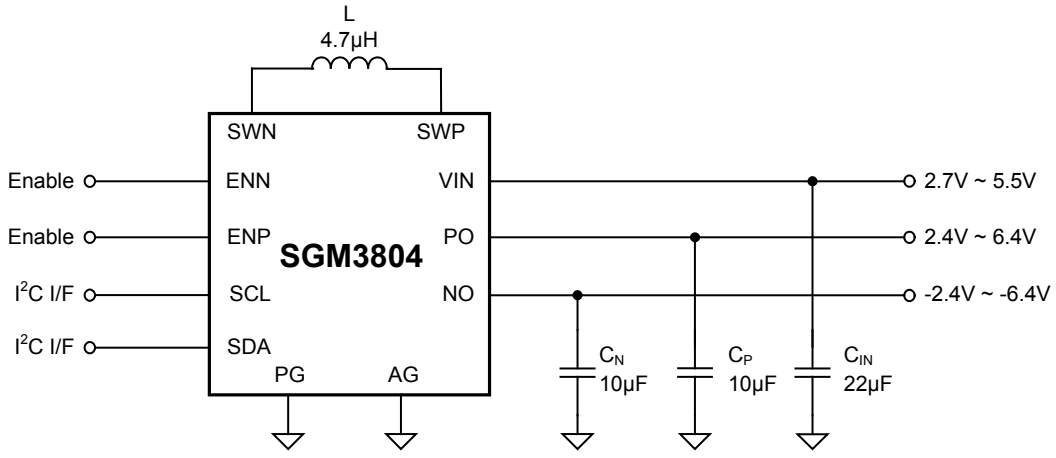


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3804-0	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-0YG/TR	XXXXX G0AYG	Tape and Reel, 3000
SGM3804-1	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-1YG/TR	XXXXX G16YG	Tape and Reel, 3000
SGM3804-2	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-2YG/TR	XXXXX G54YG	Tape and Reel, 3000
SGM3804-3	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-3YG/TR	XXXXX G55YG	Tape and Reel, 3000
SGM3804-4	WLCSP-1.7×1.51-12B	-40℃ to +85℃	SGM3804-4YG/TR	XXXXX G56YG	Tape and Reel, 3000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... -0.3V to 6V
Junction Temperature ..... 150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... 260℃
ESD Susceptibility
HBM 4000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.7V to 5.5V
Environmental Temperature Range ..... -40℃ to +85℃
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

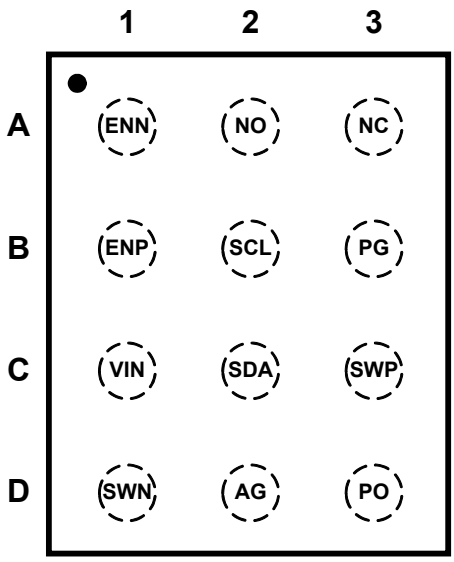
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.7×1.51-12B

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A1	ENN	I	Enable for Negative-Rail Output.
A2	NO	O	Negative-Rail Output.
A3	NC	I	No Connection.
B1	ENP	I	Enable for Positive-Rail Output.
B2	SCL	I	I²C Interface Clock Signal Pin.
B3	PG	–	Power Ground.
C1	VIN	–	Supply Input.
C2	SDA	I/O	I²C Interface Data Signal Pin.
C3	SWP	O	Switch Node for Powering the Positive-Rail. Connect this pin to one end of power inductor.
D1	SWN	O	Switch Node for Powering the Negative-Rail. Connect this pin to the other end of power inductor.
D2	AG	–	Analog Ground.
D3	PO	O	Positive-Rail Output.

FUNCTIONAL BLOCK DIAGRAM

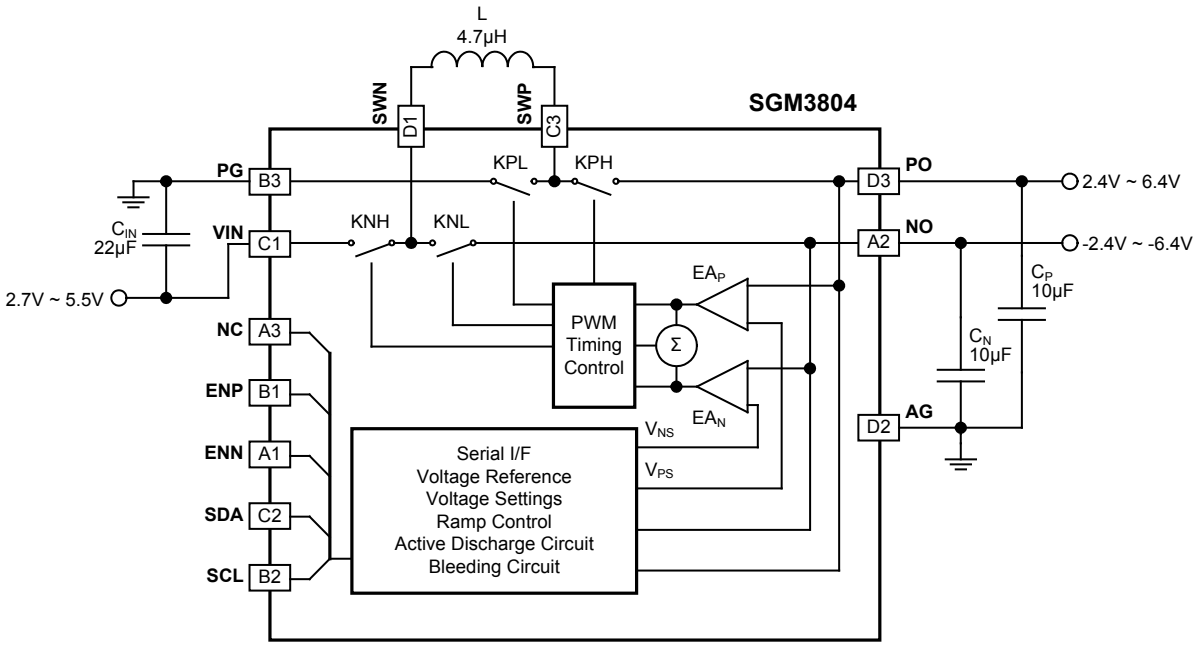


Figure 2. SGM3804 Functional Block Diagram

RECOMMENDED APPLICATION CIRCUIT

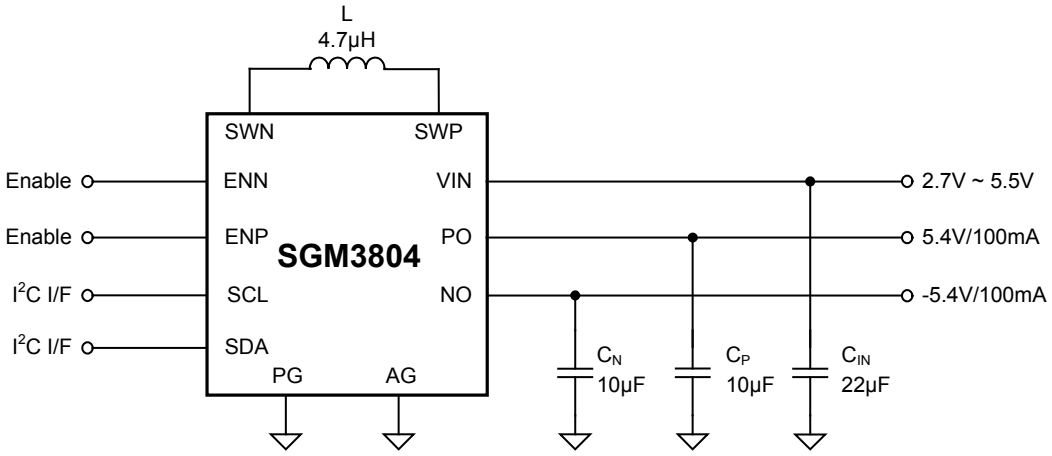


Figure 3. Recommended Application Circuit

ELECTRICAL CHARACTERISTICS

(Test at Full = -40℃ to +85℃, T_A = 25℃, V_{IN} = 3.7V, ENP = ENN = V_{IN}, unless otherwise specified noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
GENERAL FEATURES							
Input Voltage Range	V_{IN}		25℃	2.7		5.5	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	25℃		2.2	2.65	V
Supply Current with No Load	I_S	V_{IN} = 3.7V, no switching	25℃		0.4	0.55	mA
Shutdown Current	I_{OFF}	V_{IN} = 3.7V, ENP = ENN = GND	25℃		0.4	1	μA
Power-On Blanking Time	t_{BLANK}	V_{IN} = 3.7V	25℃		40		ms
Switching Frequency	f_{SW}	V_{IN} = 3.7V	25℃	1.48	1.6	1.72	MHz
Inductor Peak Current	I_{PEAK}	V_{IN} = 3.7V	25℃	1.3	1.55	1.85	A
Positive Output Voltage Range	V_{PO}		25℃	2.4		6.4	V
Positive Output Voltage Accuracy	$V_{PO\_acc\_54}$	V_{IN} = 3.7V, V_{PO} = +5.4V	25℃	-60		60	mV
	$V_{PO\_acc\_35}$	V_{IN} = 3.7V, V_{PO} = +3.5V	25℃	-60		60	mV
Discharge Resistor of Positive Output	R_{DP}		25℃		50		Ω
Discharge Time of Positive Output	t_{DISP}		25℃		10		ms
Negative Output Voltage Range	V_{NO}		25℃	-6.4		-2.4	V
Negative Output Voltage Accuracy	$V_{NO\_acc\_54}$	V_{IN} = 3.7V, V_{NO} = -5.4V	25℃	-65		65	mV
	$V_{NO\_acc\_35}$	V_{IN} = 3.7V, V_{NO} = -3.5V	25℃	-60		60	mV
Discharge Resistor of Negative Output	R_{DN}		25℃		50		Ω
Discharge Time of Negative Output	t_{DISN}		25℃		10		ms
LOGIC ENN, ENP, SCL, SDA							
Low Level Input Voltage	V_{IL}	V_{IN} = 2.7V to 5.5V	Full			0.4	V
High Level Input Voltage	V_{IH}	V_{IN} = 2.7V to 5.5V	Full	1.05			V
ENN and ENP Pull-Down Resistors	R_{EN}		25℃		200		kΩ

I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	25℃			100	kHz
		Fast mode	25℃			400	kHz
LOW Period of the SCL Clock	t_{LOW}	Standard mode	25℃	4.7			μs
		Fast mode	25℃	1.3			μs
HIGH Period of the SCL Clock	t_{HIGH}	Standard mode	25℃	4.0			μs
		Fast mode	25℃	600			ns
Bus Free Time between a STOP and a START Conditions	t_{BUF}	Standard mode	25℃	4.7			μs
		Fast mode	25℃	1.3			μs
Hold Time for a Repeated START Condition	$t_{hd;STA}$	Standard mode	25℃	4.0			μs
		Fast mode	25℃	600			ns
Setup Time for a Repeated START Condition	$t_{su;STA}$	Standard mode	25℃	4.7			μs
		Fast mode	25℃	600			ns
Data Setup Time	$t_{su;DAT}$	Standard mode	25℃	250			ns
		Fast mode	25℃	100			ns
Data Hold Time	$t_{hd;DAT}$	Standard mode	25℃	0.05		3.45	μs
		Fast mode	25℃	0.05		0.9	μs
Rise Time of SCL Signal after a Repeated START Condition and after an Acknowledge Bit	t_{RCL1}	Standard mode	25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	25℃	$20 + 0.1C_B$		1000	ns
Rise Time of SCL Signal	t_{RCL}	Standard mode	25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	25℃	$20 + 0.1C_B$		300	ns
Fall Time of SCL Signal	t_{FCL}	Standard mode	25℃	$20 + 0.1C_B$		300	ns
		Fast mode	25℃	$20 + 0.1C_B$		300	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode	25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	25℃	$20 + 0.1C_B$		300	ns
Fall Time of SDA Signal	t_{FDA}	Standard mode	25℃	$20 + 0.1C_B$		300	ns
		Fast mode	25℃	$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{su;STO}$	Standard mode	25℃	4.0			μs
		Fast mode	25℃	600			ns
Capacitive Load for SDA and SCL	C_B		25℃			0.4	nF

NOTE:
1. Industry standard I²C timing characteristics according to I²C-Bus Specification. Not tested in production.

I²C INTERFACE TIMING DIAGRAM

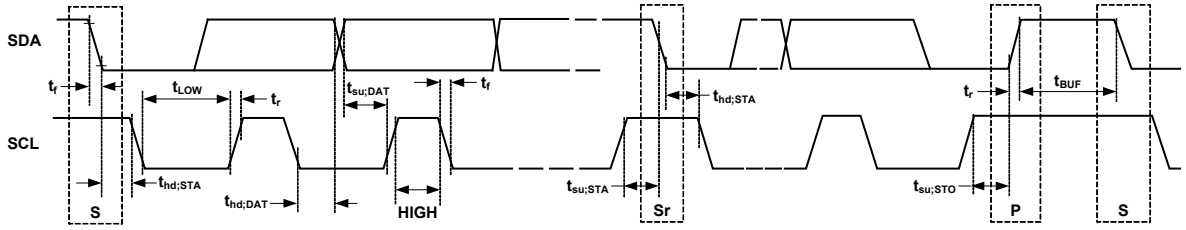


Figure 4. Serial Interface Timing for F/S-Mode

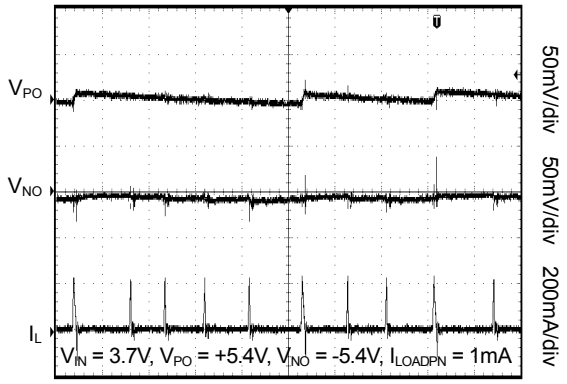
RECOMMENDED COMPONENTS OF TEST CIRCUITS

	COMPONENT		COMPONENT
INDUCTOR	4.7μH/YCL-C0805KKX7R9BB475	CAPACITOR	10μF/08055C106KAT2A
			22μF/C2012X7R1H226KT

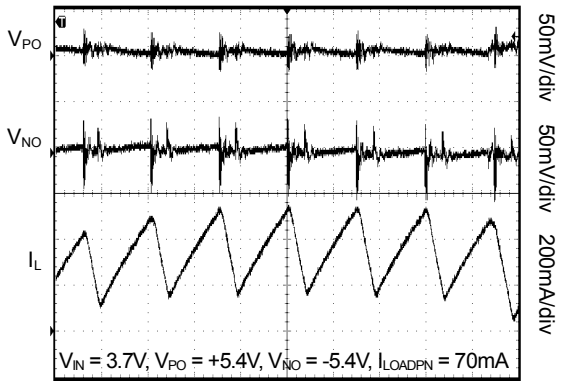
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 3.7V, V_{PO} = +5.4V, V_{NO} = -5.4V, unless otherwise noted.

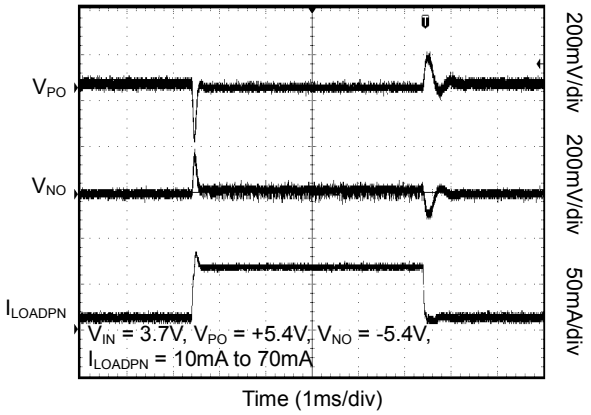
Light Load



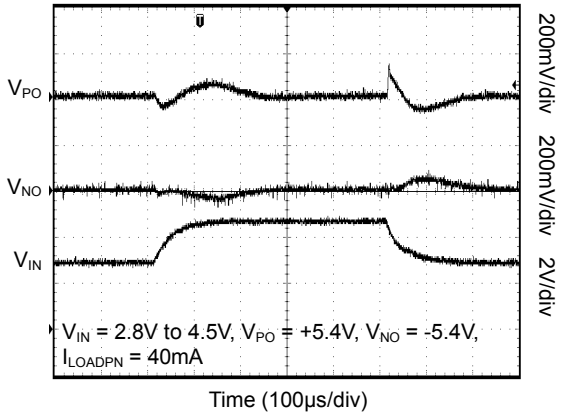
Heavy Load



Load Transient



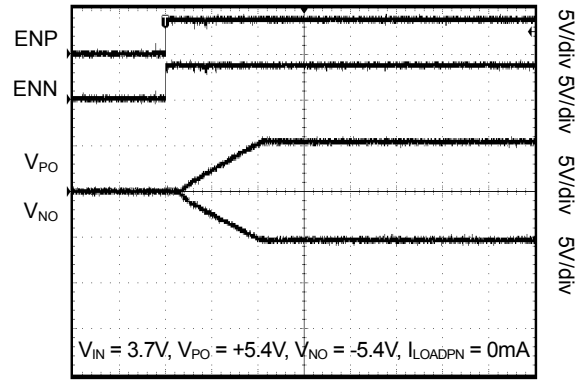
Line Transient



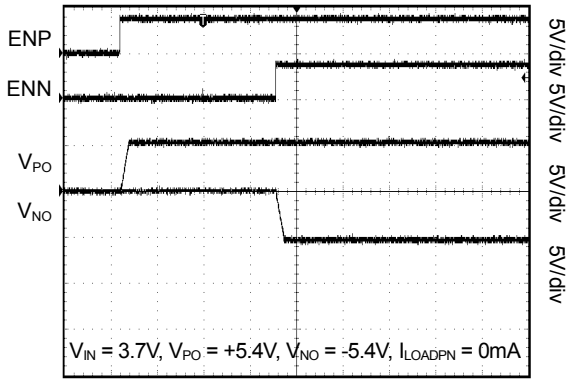
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 3.7V, V_{PO} = +5.4V, V_{NO} = -5.4V, unless otherwise noted.

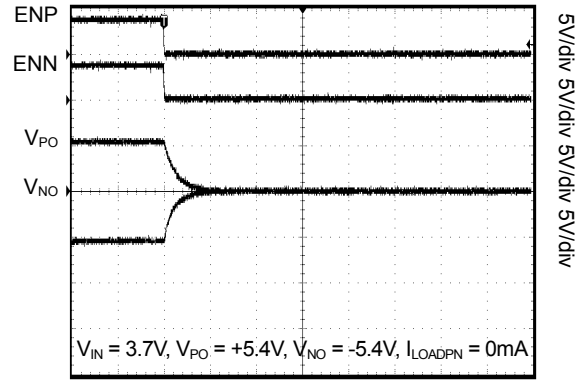
Power-Up Sequencing



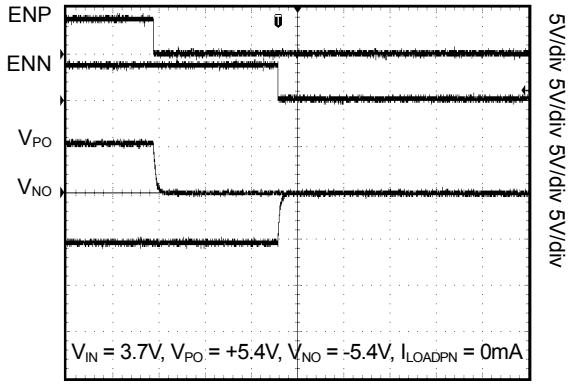
Power-Up Sequencing



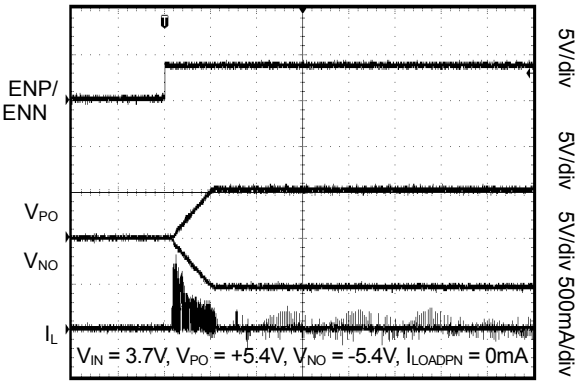
Power-Down Sequencing



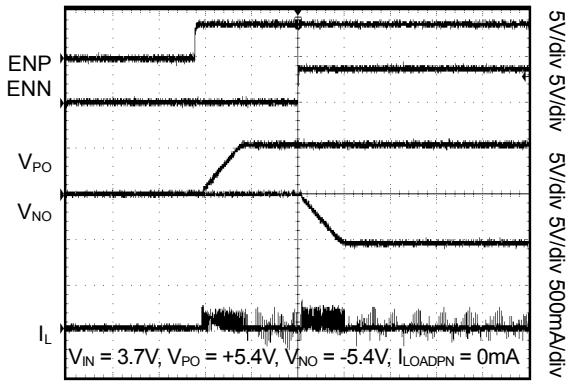
Power-Down Sequencing



Inrush Current



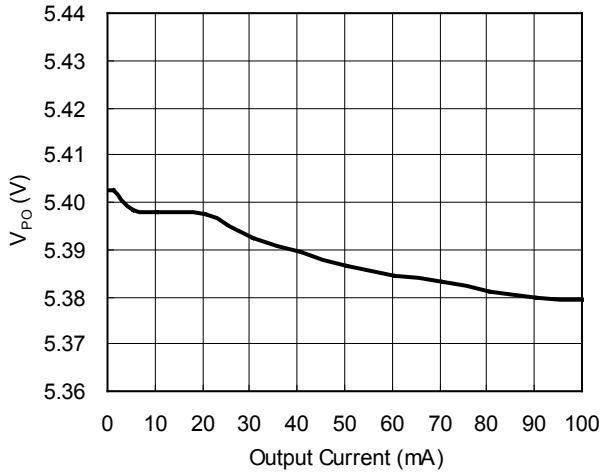
Inrush Current



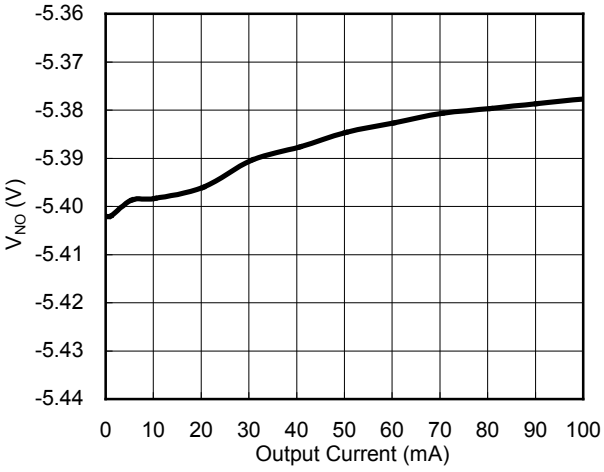
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 3.7V, V_{PO} = +5.4V, V_{NO} = -5.4V, unless otherwise noted.

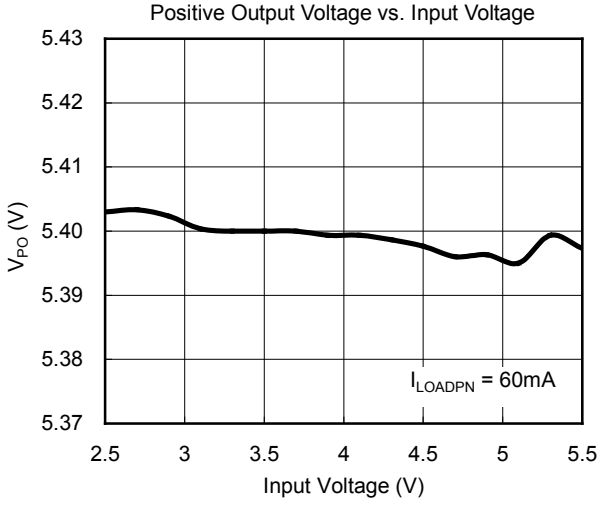
Positive Output Voltage vs. Output Current



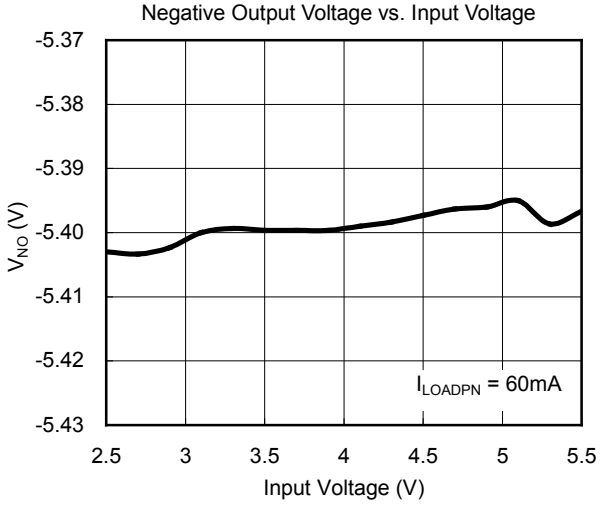
Negative Output Voltage vs. Output Current



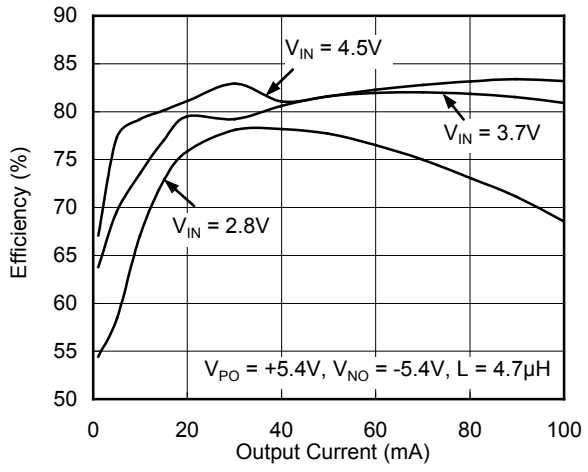
Positive Output Voltage vs. Input Voltage



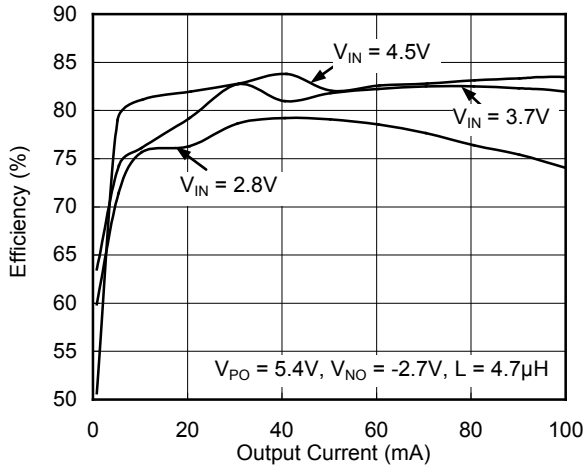
Negative Output Voltage vs. Input Voltage



Efficiency vs. Output Current



Efficiency vs. Output Current



FUNCTION, OPERATION AND APPLICATION

This device is a dedicated approach for providing two independent power rails, one positive and one negative for LCD and AMOLED driver circuit, in a small overall board area with just a few external components, which are one inductor and three capacitors. A unique control scheme is developed for suppressing the loading cross interference between two rails, which is considered as a common drawback when using single inductor to generate two rails. The circuit maintains regulation on both rails without compromising performance in either boost-inverter operation with any loading condition or buck-inverter operation with almost any loading condition.

The device could be placed into *65132's footprint, which is good with supply chain management in practice.

Under-Voltage Lockout

The SGM3804 integrates an under-voltage lockout block (or UVLO) that enables the device once the voltage on VIN pin exceeds the UVLO rising threshold. No output voltage will however be generated as long as the enable signals are not pulled HIGH. The device will be disabled as soon as the VIN voltage falls below the UVLO falling threshold.

A 40ms delay is starting as soon as the UVLO rising threshold is reached. This delay is implemented to prevent the device from being disabled or enabled by an unwanted VIN voltage spike. Once this delay has passed, the output rails can be enabled or disabled as desired with the enable signals without any delay.

Sequencing

Each output rail (V_{PO} and V_{NO}) is enabled or disabled using an external enable signal (ENP and ENN). ENP and ENN can be simultaneous or sequential.

Active Discharge

An active discharge of the positive rail and/or the negative rail can be programmed (DISP and DISN bits respectively - refer to Register Address Mapping). If programmed to be active, the discharge will occur at power down, when the enable signals go LOW.

Output Voltage

The output voltages of the converter are automatically adjusted depending on the programmed V_{PO} and V_{NO} voltages.

EMI and Acoustic Interference

Switching noise propagating along wire connections commonly dominates the EMI from the device operation, which may degrade receiver sensitivities by injecting interference into its carrier band or interim band through inter-modulation in its down converters. Inserting a ferrite bead into input power path and making short and straightforward path always work well in practice.

The device limits its lowest pulse skip frequency to be higher than audible frequency range for acoustic interference free operation.

Component and Parameter Selection

C_{IN}, C_P and C_N can be any capacitance in the range of 10μF ~ 47μF, and low loss Z5U, X7R and X5R dielectric capacitors are recommended for better performance. A 4.7μH inductor is recommended for the best efficiency.

FUNCTION, OPERATION AND APPLICATION

I²C Serial Interface Description

The SGM3804 communicates through an industry standard I²C compatible interface, to receive data in slave mode. I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification).

The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus.

The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The SGM3804 works as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: standard mode (100kbps) and fast mode (400kbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The SGM3804 supports 7-bit addressing. The device 7-bit address is 3Eh (see Figure 5), and the LSB enables the write or read function.

The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on SCL, controls the bus access, and generates START and STOP conditions (see Figure 6). A START initiates a new data transfer to a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/(W) on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledgment, ACK, (see Figure 8) by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this Acknowledgment, the master knows that communication link with a slave has been established.

MSB		SGM3804		ADDRESS			LSB
0	1	1	1	1	1	0	R/$\overline{W}$

NOTE: R/$\overline{W}$ = R/(W).

Figure 5. SGM3804 Slave Address Byte

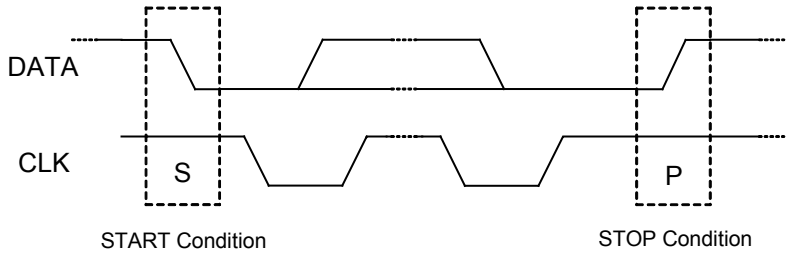


Figure 6. Start and Stop Conditions

FUNCTION, OPERATION AND APPLICATION

The master generates further SCL cycles to either transmit data to the slave (R/(W) bit = 0) or receive data from the slave (R/(W) bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To terminate the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 9). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

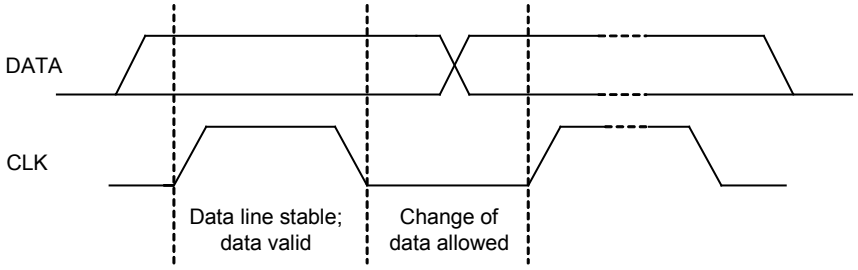


Figure 7. Bit Transfer on the Serial Interface

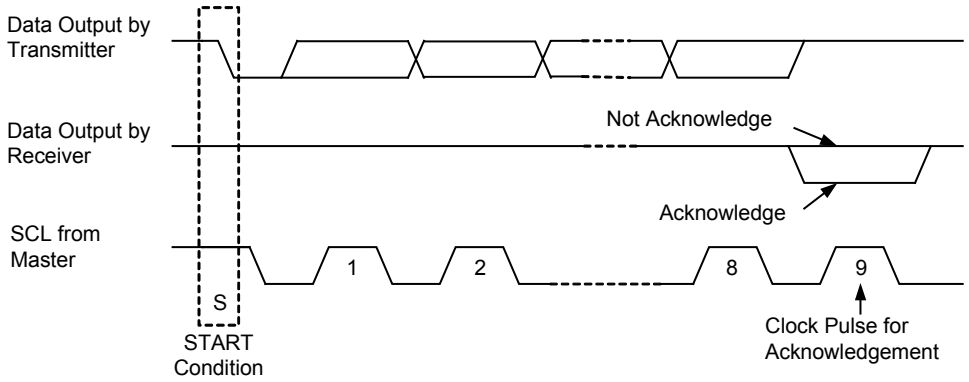


Figure 8. Acknowledge on the I^2C Bus

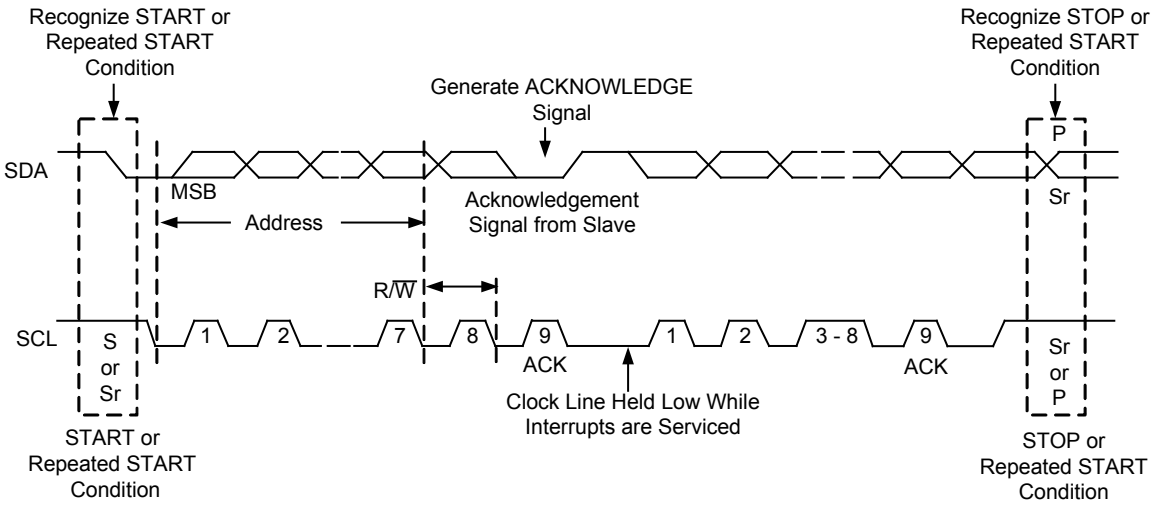


Figure 9. Bus Protocol

CONTROLS AND LOGIC DIAGRAMS

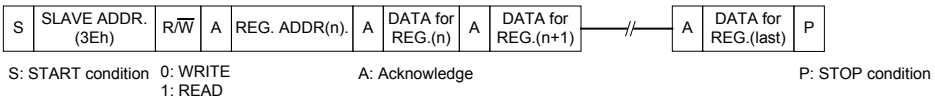


Figure 10. I²C Transfer Format Register Address Auto-Increment

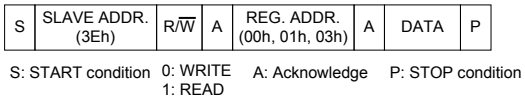


Figure 11. I²C Transfer Format Writing into a Single Register

Register Address Mapping

P: Programmable default value.

REG. ADDR.	BIT SYMBOLS AND DEFAULTS [7:0]							
	D7	D6	D5	D4	D3	D2	D1	D0
0x00			Bit5P	Bit4P	Bit3P	Bit2P	Bit1P	Bit0P
			P	P	P	P	P	P
0x01			Bit5N	Bit4N	Bit3N	Bit2N	Bit1N	Bit0N
			P	P	P	P	P	P
0x03						ADD50	DISP	DISN
						0	1	1

NOTE: Spaces left blank are not used, which could be filled with any value when programming.

Registers and Bits Descriptions

P: factory preset, W: write only bits, R/$\overline{W}$: free read or write bits. Blank for no predictable status or not care.

REG.	SYMBOL	BIT	DEFAULT	TYPE	DESCRIPTION
0x00	Bit5P	D5	P	W	Voltage code bit5 for positive rail.
0x00	Bit4P	D4	P	W	Voltage code bit4 for positive rail.
0x00	Bit3P	D3	P	W	Voltage code bit3 for positive rail.
0x00	Bit2P	D2	P	W	Voltage code bit2 for positive rail.
0x00	Bit1P	D1	P	W	Voltage code bit1 for positive rail.
0x00	Bit0P	D0	P	W	Voltage code bit0 for positive rail.
0x01	Bit5N	D5	P	W	Voltage code bit5 for negative rail.
0x01	Bit4N	D4	P	W	Voltage code bit4 for negative rail.
0x01	Bit3N	D3	P	W	Voltage code bit3 for negative rail.
0x01	Bit2N	D2	P	W	Voltage code bit2 for negative rail.
0x01	Bit1N	D1	P	W	Voltage code bit1 for negative rail.
0x01	Bit0N	D0	P	W	Voltage code bit0 for negative rail.
0x03	ADD50	D2	0	W	0: Keep the coded voltage specified with <Bit5N:Bit0N>; 1: Shift the negative rail voltage 50mV lower than the coded value.
0x03	DISP	D1	1	W	0: Disable positive rail discharge; 1: Enable positive rail discharge.
0x03	DISN	D0	1	W	0: Disable negative rail discharge; 1: Enable negative rail discharge.

CONTROLS AND LOGIC DIAGRAMS

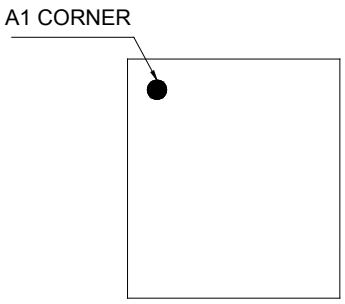
Voltage Codes to Voltage Value Mapping

CODES (1)	NEGATIVE VOLTAGE (V)	POSITIVE VOLTAGE (V)	CODES (1)	NEGATIVE VOLTAGE (V)	POSITIVE VOLTAGE (V)	CODES (1)	NEGATIVE VOLTAGE (V)	POSITIVE VOLTAGE (V)
18h	-6.4	6.4	**0Ah**	-5	5	**2Ch**	-3.6	3.6
17h	-6.3	6.3	**09h**	-4.9	4.9	**2Bh**	-3.5	3.5
16h	-6.2	6.2	**08h**	-4.8	4.8	**2Ah**	-3.4	3.4
15h	-6.1	6.1	**07h**	-4.7	4.7	**29h**	-3.3	3.3
14h	-6.0	6.0	**06h**	-4.6	4.6	**28h**	-3.2	3.2
13h	-5.9	5.9	**05h**	-4.5	4.5	**27h**	-3.1	3.1
12h	-5.8	5.8	**04h**	-4.4	4.4	**26h**	-3.0	3.0
11h	-5.7	5.7	**03h**	-4.3	4.3	**25h**	-2.9	2.9
10h	-5.6	5.6	**02h**	-4.2	4.2	**24h**	-2.8	2.8
0Fh	-5.5	5.5	**01h**	-4.1	4.1	**23h**	-2.7	2.7
0Eh	-5.4	5.4	**00h**	-4.0	4.0	**22h**	-2.6	2.6
0Dh	-5.3	5.3	**2Fh**	-3.9	3.9	**21h**	-2.5	2.5
0Ch	-5.2	5.2	**2Eh**	-3.8	3.8	**20h**	-2.4	2.4
0Bh	-5.1	5.1	**2Dh**	-3.7	3.7			

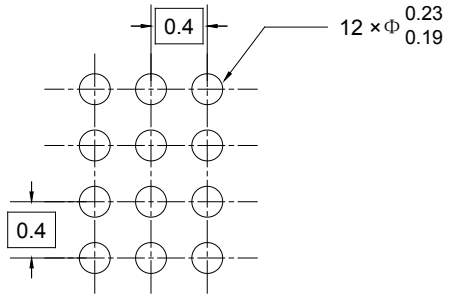
NOTE:
1. CODES = <Bit5P:Bit0P> = <Bit5N:Bit0N> with I^2C interface.

PACKAGE OUTLINE DIMENSIONS

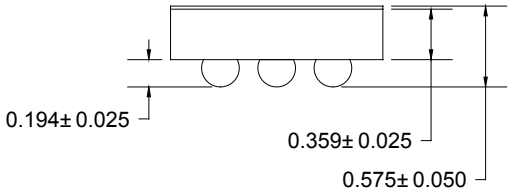
WLCSP-1.7×1.51-12B



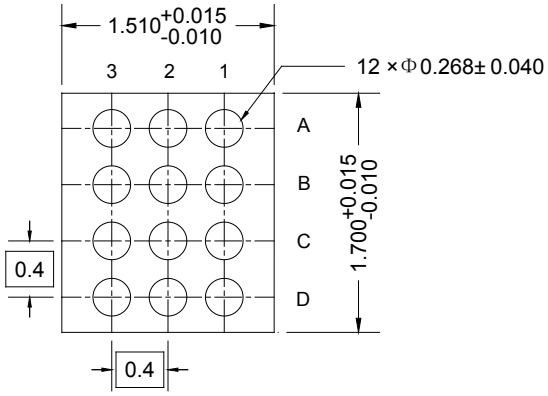
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

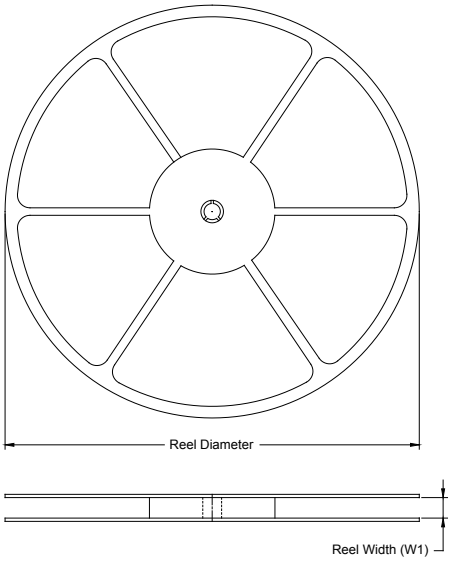


BOTTOM VIEW

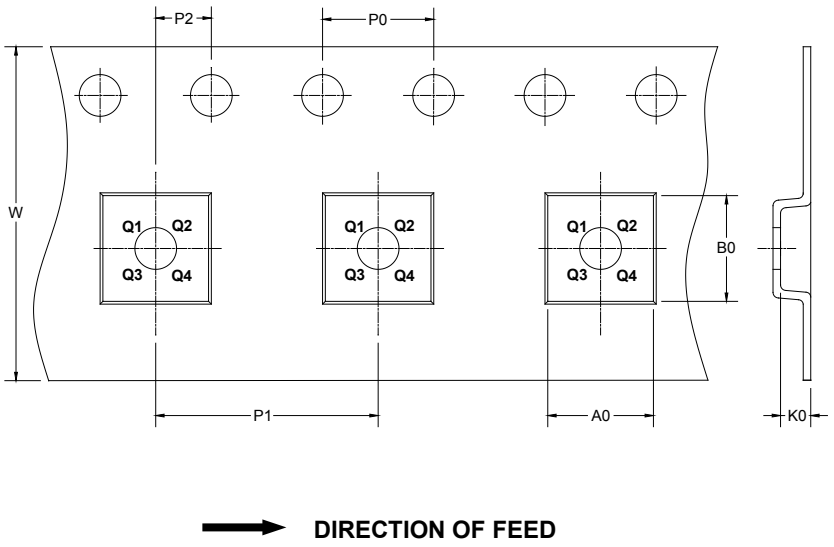
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

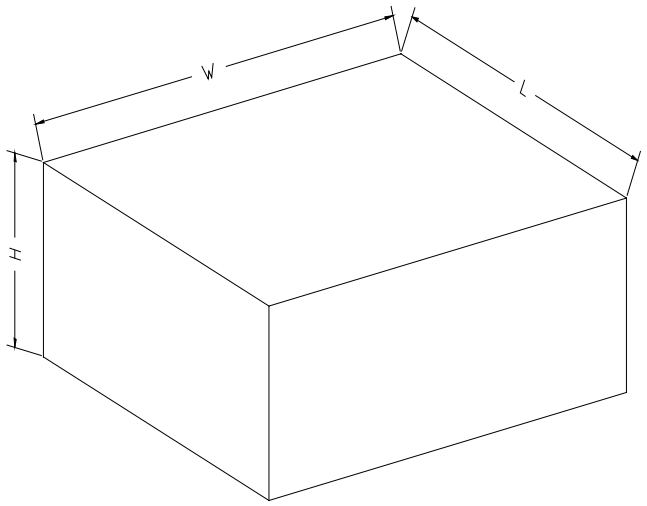
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.7×1.51-12B	7″	9.5	1.7	2.0	0.8	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002