SGM61160
4.5V to 18V Input, 6A, Synchronous Step-Down Converter with PSM

GENERAL DESCRIPTION

The SGM61160 is a peak current control, adaptive off-time Turbo™ mode synchronous step-down DC/DC converter with power-save mode (PSM) and integrated power switches. The input voltage range is from 4.5V to 18V and the output is programmable between 0.765V and 5.5V with 6A maximum output current capability.

This device offers a cost-effective and low-component count solution for bus regulators and includes a rich set of features such as low standby current, PSM at light loads to maintain high light load efficiency. The adaptive off-time Turbo™ mode control provides a fast transient response without external compensation component and seamless transitions between pulse width modulation (PWM) mode and PSM.

The SGM61160 also has a proprietary feature that enables the device to adopt low or ultra-low equivalent series resistance (ESR) output capacitors, such as POS-CAP and SP-CAP or ultra-low ESR ceramic capacitors.

The SGM61160 is available in a Green SIOC-8 (Exposed Pad) package. It operates over the -40℃ to +125℃ junction temperature range.

FEATURES

- **Wide 4.5V to 18V Input Voltage Range**
- **0.765V to 5.5V Programmable Output Voltage**
- **700kHz Pseudo-Fixed Switching Frequency**
- **Fast Transient Response with Adaptive Off-Time Turbo™ Mode**
- **Low Output Ripple with Low ESR Output Capacitors**
- **Low R_{DSON} Integrated MOSFETs (36mΩ/28mΩ)**
- **Optimized for High Efficiency at Low Duty Cycles**
- **Shutdown Current: 15μA (TYP)**
- **High Light Load Efficiency with Auto-Skip PSM**
- **Cycle-by-Cycle Current Limit**
- **Under-Voltage Lockout Protection**
- **Thermal Shutdown Protection**
- **Pre-biased Soft-Start**
- **1ms Fixed Soft-Start Time**
- **Power Good Output and Enable Input**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Low-Voltage Systems
Digital-TV Power Supplies
High-Definition Blu-Ray Disc Players
Home Networking Terminals
Digital Set-Top Boxes (STBs)

TYPICAL APPLICATION

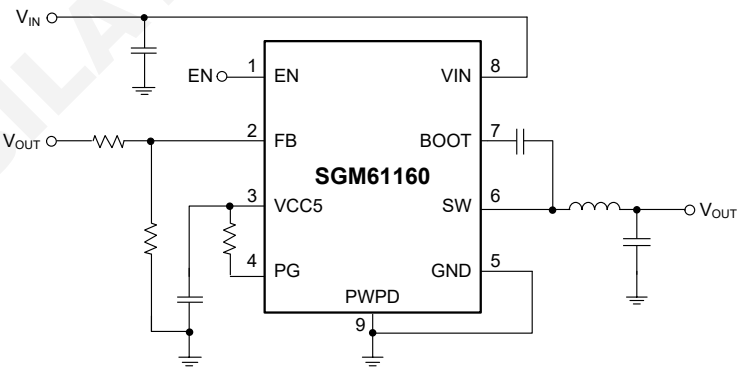

Figure 1. Typical Application Circuit

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PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61160	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61160XPS8G/TR	SGM 61160XPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX
- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to the GND Pin)

Input Voltage Ranges
- VIN, EN .... -0.3V to 20V
- BOOT .... -0.3V to 26V
- BOOT (10ns Transient) .... -0.3V to 28V
- BOOT-SW, FB, PG .... -0.3V to 6.5V
- SW .... -2V to 20V
- SW (10ns Transient) .... -3V to 22V

Output Voltage Ranges
- VCC5 .... -0.3V to 6.5V
- GND .... -0.3V to 0.3V

Voltage from GND to Thermal Pad, V_{DIFF} .... -0.2V to 0.2V
Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

RECOMMENDED OPERATING CONDITIONS

(All Voltages Referenced to the GND Pin)

Supply Input Voltage Range .... 4.5V to 18V

Input Voltage Ranges
- BOOT .... -0.1V to 24V
- BOOT (10ns Transient) .... -0.1V to 27V
- BOOT-SW .... -0.1V to 6V
- PG .... -0.1V to 5.7V
- EN .... -0.1V to 18V
- FB .... -0.1V to 5.5V
- SW .... -1.8V to 18V
- SW (10ns Transient) .... -3V to 22V
- Voltage from GND to Thermal Pad, V_{DIFF} .... -0.1V to 0.1V

VCC5 Output Voltage Range (V_{VCC5}) .... -0.1V to 5.7V
VCC5 Output Current Range (I_{VCC5}) .... 0mA to 5mA
Operating Ambient Temperature Range .... -40℃ to +125℃
Operating Junction Temperature Range .... -40℃ to +125℃

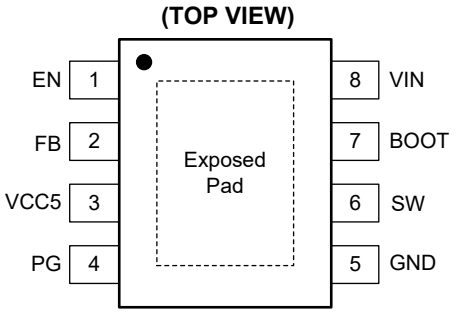
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	EN	Enable Input. The EN pin is active high and must be pulled up to enable the device.
2	FB	Feedback Input. Connect to the center point of the resistor divider to program the output voltage.
3	VCC5	5.1V Output. Connect a 1μF ceramic capacitor between VCC5 and GND pins as close to the device as possible. The VCC5 pin is not active when EN pin is low.
4	PG	Power Good Output. It is an open-drain output and needs an external pull-up resistor. It can be pulled up to VCC5 pin. Do not pull up to voltage rails above 5.7V.
5	GND	Ground Pin. Ground reference and power return for switching circuit. Connect the input and output capacitor returns to GND at a single point near the GND pin.
6	SW	Switching Node Output. Connect this pin to the power inductor and one terminal of the bootstrap capacitor. Keep the copper area connected to this pin small and on the same layer to minimize EMI noise. Keep sensitive signals such as FB traces away from this node.
7	BOOT	Bootstrap Input. Connect this pin to the other terminal of the bootstrap capacitor. A 0.1μF ceramic capacitor (C_{BOOT}) is recommended. This capacitor along with an internal diode between VCC5 and BOOT nodes is used to supply the high-side switch gate voltage. The high-side gate voltage needs to be higher than V_{IN} and is provided by bootstrapping the SW voltage with C_{BOOT} and internal diode.
8	VIN	Power Supply Input. Connect a low ESR ceramic capacitor between VIN and GND pins as close to the device as possible to supply pulsating currents of the power converter and minimize the voltage ringing and noise on the SW node.
Exposed Pad	GND	Exposed Pad of the Package. It is provided to conduct heat away from the device and must be soldered to GND copper planes. Filled vias under this pad can enhance thermal conduction to other layers, improve reliability by operating at lower junction temperatures and maximize achievable output current (less derating).

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ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Operating Non-Switching Supply Current	I_{VIN}	VIN current, V_{EN} = 5V, V_{FB} = 0.8V		500		μA
Shutdown Supply Current	I_{SHDN}	VIN current, V_{EN} = 0V		15		μA
Logic Threshold						
EN High Level Input Voltage	V_{ENH}	V_{EN} rising	1.6			V
EN Low Level Input Voltage	V_{ENL}	V_{EN} falling			0.6	V
FB Voltage						
FB Threshold Voltage	V_{FBTH}	V_{OUT} = 1.05V, CCM operation		765		mV
FB Bias Current	I_{FB}	V_{FB} = 0.8V		±0.15		μA
VCC5 Output						
VCC5 Output Voltage	V_{VCC5}	V_{IN} = 6V to 18V, I_{VCC5} = 0mA to 5mA		5.1		V
VCC5 Output Current	I_{VCC5}	V_{IN} = 6V, V_{VCC5} = 4V	20			mA
Power MOSFETs						
High-side Switch On-Resistance	R_{DSON}	V_{BOOT} - V_{SW} = 5.5V		36		mΩ
Low-side Switch On-Resistance				28		mΩ
Over-Current Limit						
High-side Peak Current Limit	I_{OCL_HS}	L = 1.5μH (1)		9		A
Low-side Valley Current Limit	I_{OCL_LS}	L = 1.5μH (1)		6.7		A
On-Time Timer Control						
Switching Pulse On-Time	t_{ON}	V_{IN} = 12V, V_{OUT} = 1.05V		150		ns
Minimum Off-Time between On Pulses	t_{OFF_MIN}	V_{FB} = 0.7V		260		ns
Soft-Start						
Internal Soft-Start Time	t_{SS}			1.0		ms
Power Good						
Power Good Threshold	V_{THPG}	V_{FB} rising (good)		90%× V_{REF}		V
		V_{FB} falling (fault)		85%× V_{REF}		
Power Good Sink Current	I_{PG}	V_{PG} = 5V		4		mA
UVLO						
UVLO Threshold (on VCC5)	UVLO	Wakeup VCC5 voltage (rising)		3.75		V
		Hysteresis VCC5 voltage		0.32		
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SHDN}	Temperature rising		150		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}			25		℃

NOTE:

1. Not tested in production.

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FUNCTIONAL BLOCK DIAGRAM

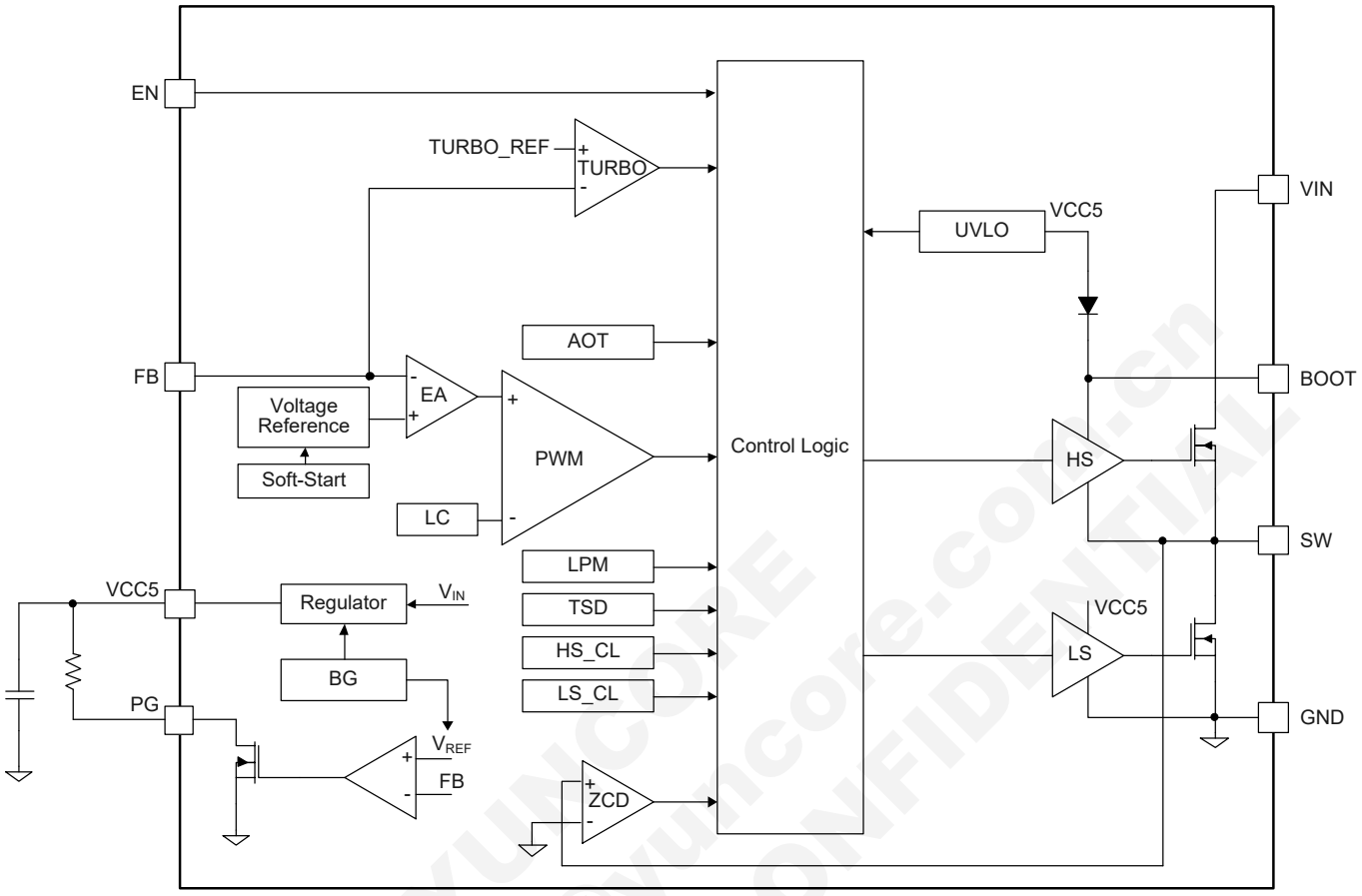

Figure 2. SGM61160 Block Diagram

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DETAILED DESCRIPTION

Overview

The SGM61160 is a 6A synchronous step-down (buck) converter with integrated N-channel power MOSFETs and power-save mode (PSM). Using adaptive off-time Turbo™ control, it can provide a fast transient response with reduced output capacitance. Moreover, low ESR ceramic or polymer capacitors can be used on the output due to a proprietary internal ripple simulation circuit. The PG output can also be used for power supply sequencing.

PWM Operation

An adaptive off-time PWM controller that supports a proprietary Turbo™ mode control is a main control loop of the SGM61160. The Turbo™ mode control combines adaptive off-time control with an internal compensation circuit for pseudo-fixed frequency operation with minimum external components. This controller supports low ESR ceramic or special polymer output capacitors and is stable even with virtually no output ripple.

The high-side MOSFET (HS) is turned on at the beginning of each cycle and on-time is decided by the error amplifier (EA) which is proportional to the HS power MOSFET current. The off-time is decided by the one-shot timer. The one-shot time is set by V_{IN} and V_{OUT} such that the operating frequency is almost constant (pseudo-fixed) over the V_{IN} range, and the off-time is adapted accordingly (that's why it is called adaptive off-time control). After the one-shot is reset, the high-side switch is turned on again when V_{FB} falls below V_{REF}. To simulate the output ripple and eliminate the need for the actual ripple caused by ESR, a ramp signal is added to V_{REF} before comparison.

During the load transient condition, when the output voltage is lower than 97.5% × V_{REF}, the Turbo^{TM} mode will be triggered to improve the load transient performance.

The SGM61160 does not have a dedicated oscillator and runs at 700kHz pseudo-fixed frequency. In continuous conduction mode (CCM), the off-time is set proportional to the V_{OUT}/V_{IN} and because $D = t_{ON}/T = f(1 - t_{OFF})$, the frequency is almost constant.

Auto-Skip PSM Control

To improve light load efficiency, the auto-skip PSM feature is included in the SGM61160. By reducing the load, the inductor current is also reduced and at the boundary point the valley current reaches zero. With further reduction of the load, the continuous conduction mode (CCM) changes to discontinuous conduction mode (DCM). The low-side switch (synchronous rectifier) is turned off when zero inductor current is detected. In DCM, the on-time is kept almost the same as CCM, so it takes a longer off-time to discharge the output capacitor to the reference voltage level. The transition point at which the CCM to DCM change occurs (light load operation, LL), can be calculated by Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

Soft-Start with Pre-biased

A fixed 1.0ms internal soft-start circuit is included in the SGM61160. When VIN voltage is in the operating range and EN is pulled high, the reference voltage to the PWM comparator begins ramping up by the soft-start and the output will follow with the same ramp slope.

If a pre-bias voltage is present on the output at start-up, sink current from the output must be avoided and controller should be prepared for a smooth and monotonic output ramp. In SGM61160 a special circuit blocks the synchronous rectification of the low-side switch and prevents backward boosting when the demanded output ramp is still lower than the output pre-biased level. Then the synchronous rectification is gradually started with narrow gate pulses on the low-side switch and the on-time is increased cycle-by-cycle until it reaches the time dictated by the controller (1-D). This process assures smooth ramp up into regulation and the controller has enough time to adjust itself for smooth transition from pre-biased output to normal output regulation.

Power Good Function (PG)

The PG open-drain output is functional after the soft-start is completed. When power good function is activated, the PG output is released to go high when V_{FB} exceeds 90% × 0.765V of the regulation target. If V_{FB} falls below 15% × 0.765V of the target value, PG is pulled low. Use a 25kΩ to 150kΩ resistor (R_{PG}) for pulling the PG pin up to the VCC5.

When V_{FB} exceeds 10% × 0.765V, the PG is still high. And the chip stops switching.

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DETAILED DESCRIPTION (continued)

Over-Current Protection (OCP)

Both high-side and low-side switches are protected against over-current event. Cycle-by-cycle valley and peak current detection determines the load over-current limit. The low-side switch current is monitored by measuring its drain-to-source voltage (SW-GND voltage) during the off-time as a signal proportional low-side switch current. The sensed voltage is temperature compensated for improve accuracy. If this voltage is above the low-side limit value, the low-side switch will remain on and the off-time is extended until inductor current falls below this limit. Then a new cycle starts by turning the high-side switch on. Note that the actual load current limit (or the inductor average current) is higher than low-side switch limit by half of the inductor peak-to-peak ripple that must be considered in the design.

Under-Voltage Lockout Protection (UVLO)

The internal device circuitry may malfunction if the VCC5 voltage that powers the internal circuitry is not high enough. VCC5 is powered from VIN. For UVLO protection, VCC5 is monitored and if it falls below UVLO threshold the device will shut down. Normal operation will resume when VCC5 rises above the UVLO threshold with a small hysteresis window.

Thermal Shutdown (OTP)

The junction temperature (T_J) is constantly monitored for over-temperature protection. If it exceeds +150℃ (TYP), the device will shut down. Normal operation is automatically resumed when the junction temperature cools down and T_J decreases by approximately 25℃.

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APPLICATION INFORMATION

The SGM61160 can deliver up to 6A output current from a 4.5V to 18V input supply and its output voltage is programmable from 0.765V to 5.5V with a resistor divider network. A 1.05V output power supply is shown in Figure 3 as an example to explain the simplified design procedure.

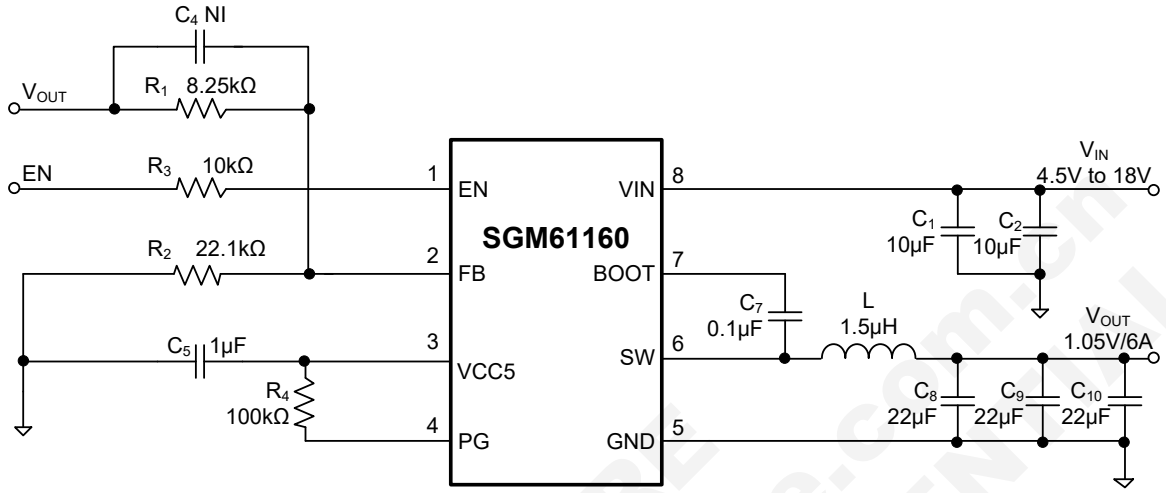

Figure 3. 1.05V/6A Power Supply Design Example with SGM61160

Table 1. Bill of Materials for Typical Application Circuit at 1.05V/6A

Designator	Qty	Description	Package	Manufacturer	P/N
C_1, C_2	2	Capacitor, Ceramic, 10μF, 25V, ±10%, X7R	1206	Murata	
C_5	1	Capacitor, Ceramic, 1.0μF, 25V, ±10%, X7R	0603	Murata	
C_8, C_9, C_{10}	3	Capacitor, Ceramic, 22μF, 16V, ±10%, X7R	0805	Murata	
C_7	1	Capacitor, Ceramic, 0.1μF, 25V, ±10%, X7R	0603	Murata	
R_1	1	Resistor, 8.25kΩ, ±1%, 0.1W	0603	UniOhm	
R_2	1	Resistor, 22.1kΩ, ±1%, 0.1W	0603	UniOhm	
R_3	1	Resistor, 10kΩ, ±1%, 0.1W	0603	UniOhm	
R_4	1	Resistor, 100kΩ, ±1%, 0.1W	0603	UniOhm	
L	1	Inductor, Metallic Magnetic Core, 1.5μH ± 20%, I_{TEMP} = 11A, I_{SAT} = 11.5A, DCR = 9.7mΩ	7.1mm × 6.5mm × 3.5mm SMD	TDK	SPM6530T-1R5M100

Step-by-Step Design

The following application parameters should be known to start the design:

- Input Voltage Range
- Desired Output Voltage
- Desired Maximum Output Current
- Maximum Acceptable Output Voltage Ripple
- Maximum Acceptable Input Voltage Ripple

Resistor Divider Design

Design R_1 and R_2 resistors to set V_{OUT} using Equation 2. Use ±1% or better resistors for more accurate output:

$$V_{OUT} = 0.765 \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

For higher light load efficiency, larger resistors are preferred. However, high resistances make the sensitive FB input more susceptible to noise and voltage errors due to FB input bias current, so a tradeoff is needed.

Output Filter (L and C_{OUT} Design)

The output LC low-pass filter has a double pole at the f_P frequency as given in Equation 3:

$$f_P = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} \quad (3)$$

APPLICATION INFORMATION (continued)

At lower frequencies, the loop gain is set by the resistor divider network and the SGM61160 internal gain. The operation amplifier phase is 180° at these frequencies. At the double pole frequency, the gain rolls off with -40dB/dec rate and the phase drops rapidly. The adaptive off-time controller adds an equivalent high frequency zero and reduces the gain roll off rate to -20dB/dec and increases the phase for 90° at one decade above the zero frequency. The L and C_{OUT} must be chosen such that f_P is less than the high frequency zero, but close enough to get adequate phase boost for a good phase margin and stability. Use the recommended values in Table 2 to meet these requirements.

For higher V_{OUT} values, R_1 is typically large and transients on V_{OUT} are weakened before being sensed by FB. A feedforward capacitor (C_4) in parallel with R_1 can be used to compensate that and provide proper feedback of transients for additional phase boost.

The inductor peak-to-peak ripple current (ΔI_L), peak current (I_{PEAK}) and RMS current ($I_{L(RMS)}$) can be calculated from Equation 4, 5, and 6 respectively.

$$\Delta I_L = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12}\Delta I_L^2} \quad (6)$$

Table 2. Recommended Component Values for Different Output Voltages

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	C_4 (pF) (Optional)			L (μH)			$C_{OUT} = C_8 + C_9 + C_{10}$ (μF)	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX
1	6.81	22.1	5	150	220	1.0	1.5	4.7	66	
1.05	8.25	22.1	5	150	220	1.0	1.5	4.7	66	
1.2	12.7	22.1	5		100	1.0	1.5	4.7	44	
1.5	21.5	22.1	5		68	1.0	1.5	4.7	44	
1.8	30.1	22.1	5		22	1.2	1.5	4.7	44	
2.5	49.9	22.1	5		22	1.5	2.2	4.7	44	
3.3	73.2	22.1	2		22	1.8	2.2	4.7	44	
5	124	22.1	2		22	2.2	3.3	4.7	44	

The inductor rated saturation current must be higher than the calculated peak current. Also, the rated RMS current (heating) must be greater than the calculated RMS current. Choosing an inductor with lower DCR resistance (typically smaller than low-side switch R_{DSON}) improves the efficiency significantly. Consider f_{SW} = 700kHz in the equations for CCM operation.

For this example, the calculations result in I_{PEAK} = 6.51A and $I_{L(RMS)}$ = 6.01A. A TDK SPM6530-1R5M100 shielded inductor (L = 1.5μH) with peak current rating of 11.6A, RMS current rating of 11A and maximum DCR of 10.7mΩ is chosen.

The C_{OUT} capacitance and ESR determine the magnitude of the output voltage ripple. The SGM61160 is designed for ceramic or other low ESR capacitors. Recommended C_{OUT} values are between 22μF to 68μF. Equation 7 gives the C_{OUT} RMS current.

$$I_{C_{OUT}(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L \times f_{SW}} \quad (7)$$

For this example two TDK C3216X5R0J226M 22μF, 6.3V, X5R capacitors with typical ESR of 2mΩ (each) are used (C_{OUT} = 44μF). The calculated RMS current is 0.286A while each output capacitor can handle 4A.

Input Capacitor Design (C_{IN})

A ceramic input decoupling capacitor is necessary for the SGM61160. The recommended value is at least 10μF along with an additional small package size 0.1μF capacitor for high frequency filtering. A bulk capacitor may be required depending on the application. Consider ceramic capacitor voltage derating and choose large voltage margin for C_{IN}.

Bootstrap Capacitor (C_{BOOT})

Connect a 0.1μF capacitor between BOOT and SW pins. Ceramic capacitor is recommended.

VCC5 Decoupling Capacitor (C_5)

Connect a 1μF ceramic capacitor between VCC5 and GND pins as close to the device as possible.

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APPLICATION INFORMATION (continued)

Thermal Design Considerations

This SGM61160 is encapsulated in an SOIC-8 (Exposed Pad) package for heat sinking. Solder the thermal pad directly to the PCB ground planes as heat sink. Use filled thermal vias to conduct the heat to other GND copper planes or a designed heat sink copper area.

Layout Guides

A list of important PCB layout considerations are provided below:

1. Heat dissipation is an important consideration due to large 6A load current. Fill the top-side area near the SGM61160 with ground plane as much as possible.

2. Dedicate the bottom-side of the PCB that is directly under the IC for ground planes and connect it directly to the thermal pad of the device with vias. Consider the ground areas as large as it is practical including additional internal layers.

3. Keep the input switching current loop as small as possible with input capacitor placed as close as possible to VIN and GND pins.

4. Keep the SW node short and small to minimize parasitic capacitance and radiated emissions.

5. Consider Kelvin connections for connecting the output terminals (load point) to the feedback pin.

6. Keep analog and non-switching elements away from switching components and traces.

7. Consider separate AGND and PGND ground planes for sensitive and high current returns respectively and make a single point connection between them and device GND pin.

8. Do not allow switching current to flow under the device.

9. Solder the exposed pad to PGND.

10. Place VCC5 capacitor near the device and connect it to PGND.

11. Connect input and output capacitor grounds to the broad PGND planes on the same layer.

12. Voltage feedback loop should be as short as possible and preferably surrounded by ground shields.

13. Tie the voltage divider lower resistor (R_2) to AGND.

14. Use enough vias to stitch VIN and PGND planes on different layers.

15. FB node connected copper must be as short as possible.

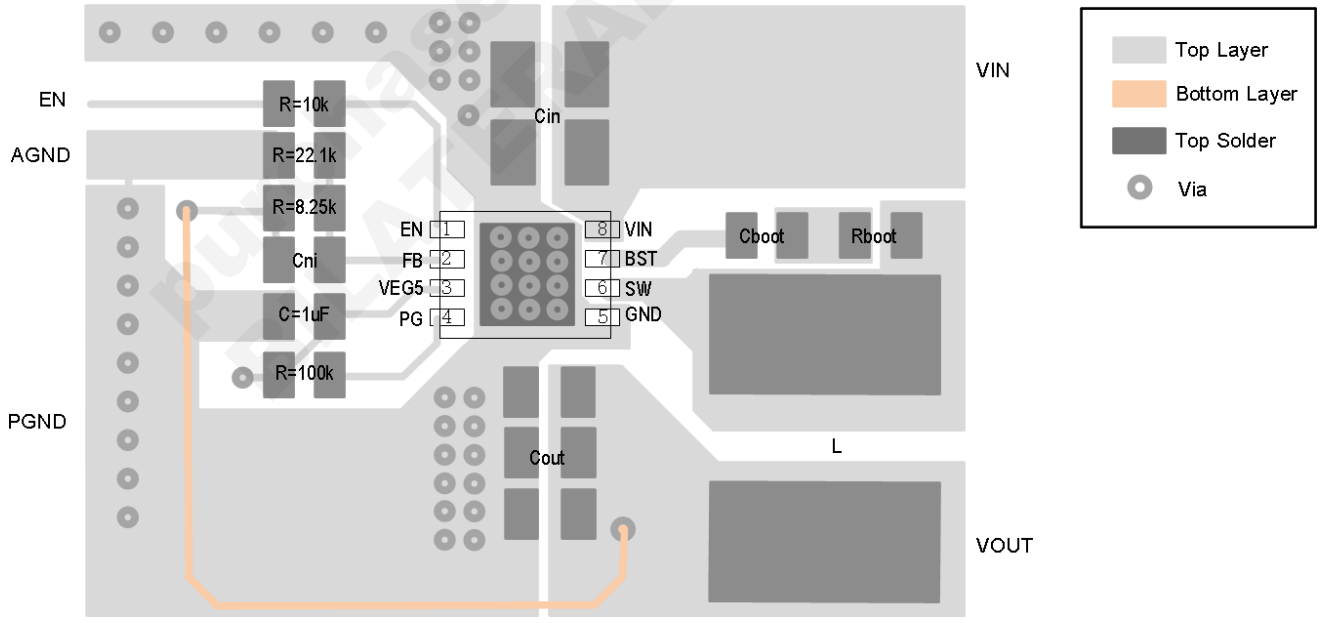
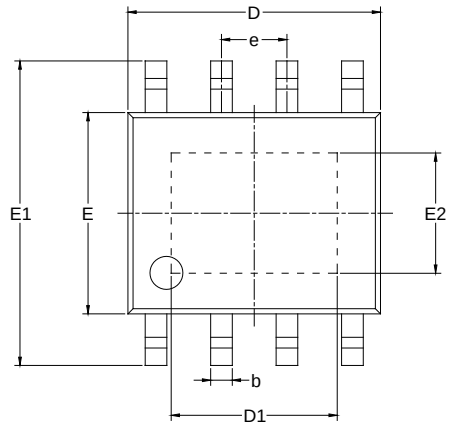
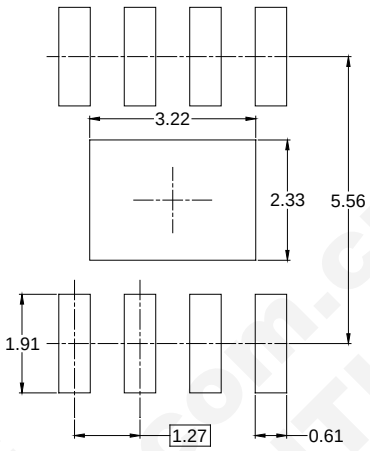


Figure 4. PCB Layout

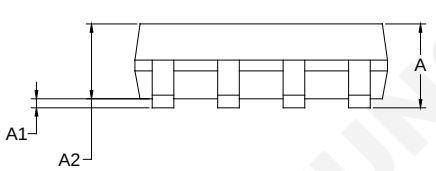
PACKAGE OUTLINE DIMENSIONS

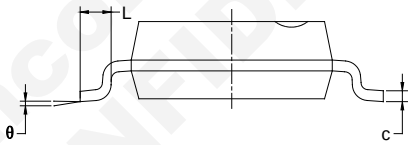
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°

NOTES:

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

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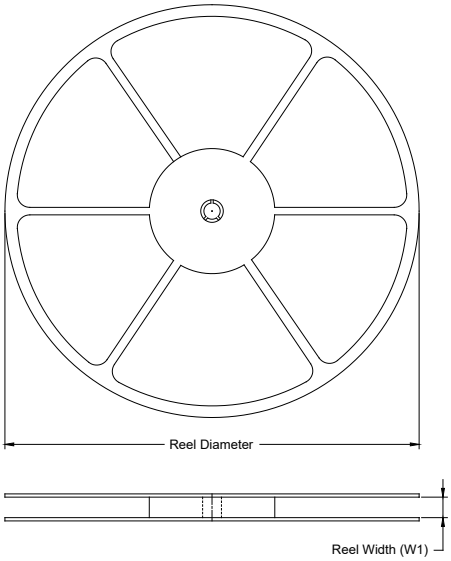
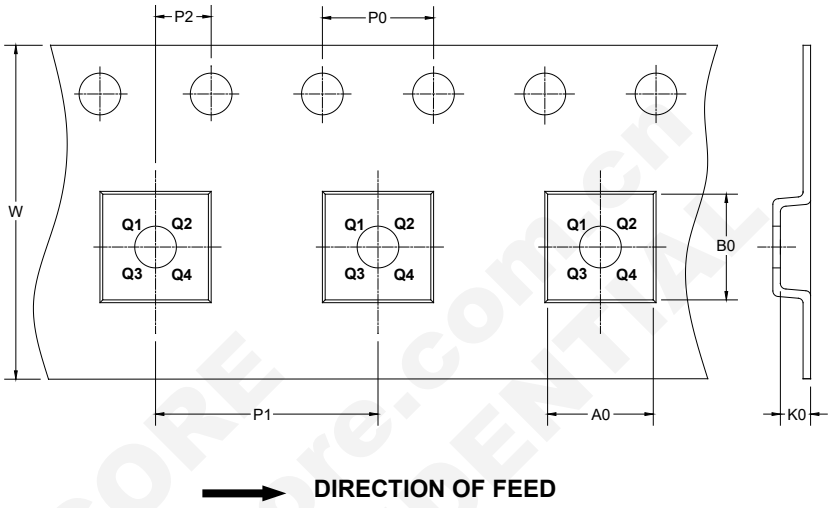
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

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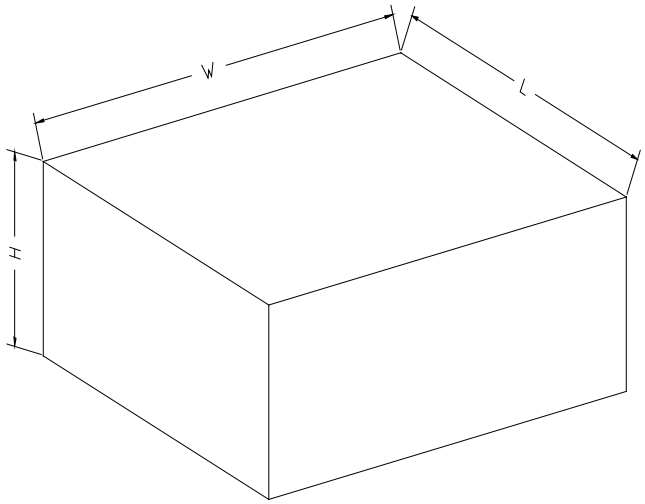
CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002

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