SGM41281/SGM41281C
70V/35V 2.5mA Precise Protection APD Bias Dual-Gains Current Mirror w/ Output Enable

GENERAL DESCRIPTION

The SGM41281 or the SGM41281C integrates a boost for generating up to 70V regulated output, a dual-gains current mirror with a controlled output buffer, which is unique to simplify the multi-channel receiving monitoring sharing design with a MCU with regular resolution ADC. Its precise over current protection and mirror voltage drop compensation further make design tradeoff comfortable between more sensitivity and more robust.

The SGM41281 is available in Green TQFN-3×3-16L package and the SGM41281C is available in Green 12-Bump, 1.2mm × 1.6mm, 0.4mm Pitch WLCSP package. Both operate over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Up to 70V Output 1.3MHz Boost Regulator**
- **1:30 Output Voltage Programming**
- **Programmable Precise Over Current Limit Protection**
- **Compensated Mirror Voltage Drop**
- **Internal X1/X16 Dual Gain Current Mirror**
- **2.5V Full Scale Current to Voltage Buffer**
- **Full Chain Circuit: Bias-Mirror-Track/Hold**
- **Controlled Monitoring Outputs for Sharing**
- **SGM41281 Available in Green TQFN-3×3-16L Package**
- **SGM41281C Available in Green 12-Bump, 1.2mm × 1.6mm, 0.4mm Pitch WLCSP Package**
- **-40℃ to +85℃ Operating Temperature Range**

APPLICATIONS

CWDM/DWDM Fiber Modules
CFP Modules

TYPICAL APPLICATION

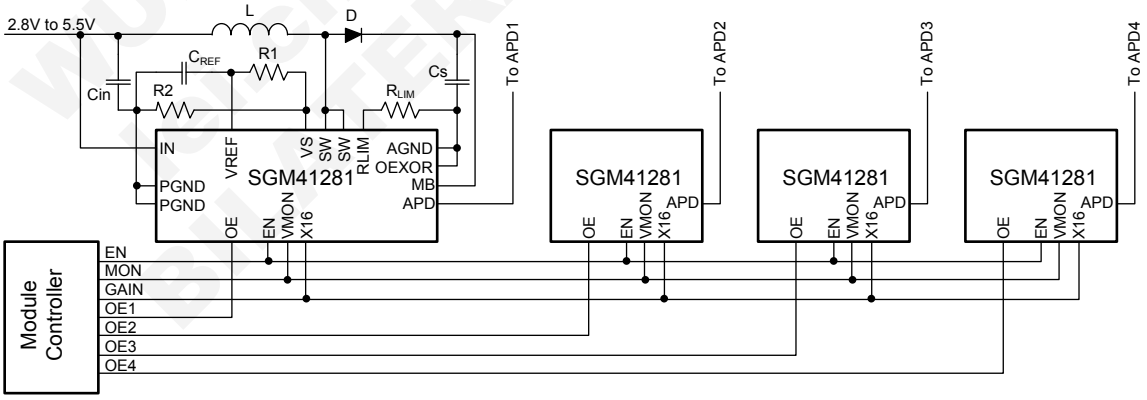


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41281	TQFN-3×3-16L	-40℃ to +85℃	SGM41281YTQ16G/TR	41281TQ XXXXX	Tape and Reel, 4000
SGM41281C	WLCSP	-40℃ to +85℃			

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, EN, VS, OE, VMON, RLIM, VREF, X16, OEXOR ..... -0.3V to 6V
SW, MB..... -0.3V to 76V
APD .....-0.3V to (MB + 0.3V)
Storage Temperature Range.....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .....2.8V to 5.5V
V_{APD} Range, SGM41281.....20V to 70V
V_{APD} Range, SGM41281C .....15V to 35V
I_{APD}.....<2mA
Junction Temperature Range.....-40℃ to +125℃
Environmental Temperature Range .....-40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

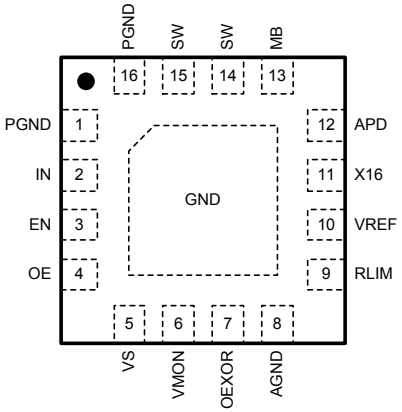
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

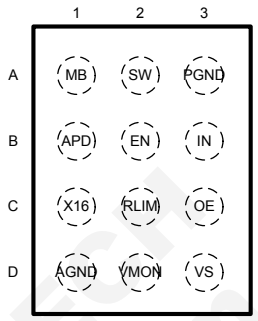
PIN CONFIGURATIONS

SGM41281 (TOP VIEW)



TQFN-3×3-16L

SGM41281C (TOP VIEW)



WLCSP

PIN DESCRIPTION

PIN		NAME	TYPE (1)	FUNCTION
TQFN-3×3-16L	WLCSP			
1, 16	A3	PGND	G	Ground, current return path of the boost switch.
2	B3	IN	P	Power Input to all Internal Circuit. A 4.7μF or over high frequency type capacitor placed close to IN and PGND is recommended.
3	B2	EN	I	Enable Input. Input high to enable this chip, low to shut down.
4	C3	OE	I	Output Enable. Its effective logic level is decided by the logic level seen at the OEXOR input. If the (OE xor OEXOR) is true, enables the VMON and X16 to output, or both are put into high-Z state otherwise.
5	D3	VS	I	Proportional input for programming the MB voltage with an increment gain of 1:30.
6	D2	VMON	O	Current Monitoring Output, which is a voltage proportional to the current out of the APD pin.
7	–	OEXOR	I	Logic input; for selecting effective logic level of output enabling at the OE input. The complementary logic level to the logic level of the OEXOR at the OE is put for tracking.
8	D1	AGND	G	Ground; current return path of the current sensing circuit.
9	C2	RLIM		Current-Limit Programming. Connect a resistor from RLIM to GND to program the APD current-limit threshold.
10	–	VREF	O	2.5V Voltage Reference Output.
11	C1	X16	O	Gain Selection Output. The current monitoring circuit selects internal X1 or X16 stage adaptively against the current level for extending the monitoring scale by 16 times over a given an ADC type. Output high for reporting that the X16 gain stage is selected.
12	B1	APD	O	Output for Biasing the APD Device. The current out of this pin is sampled with a mirror circuit for current monitoring and over current protection. The voltage drop over the mirror stage is compensated against the current change, which maintains the drop varying less.
13	A1	MB	I	Mirror Bias Input. Connected to the boost stage output.
14, 15	A2	SW	O	Low End Boost Switch Output. Connect to the anode of the rectifier diode and the boost end of a power inductor.
Exposed Pad	–	GND	G	Ground; internally tie to substrate of the circuit.

NOTE : I: input, O: output, G: ground, P: power for the circuit.

ELECTRICAL CHARACTERISTICS

(Test at T_A = +25℃, V_{IN} = 3.3V, EN = V_{IN}, V_{FS} = 70V for the SGM41281, V_{FS} = 35V for the SGM41281C, unless otherwise specified in test conditions. Limits in boldface type apply over the entire junction temperature range for operation. Limits are production tested, and highly appreciate values on characterization and statistics.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}		2.8		5.5	V
Efficiency	η	70V 1mA loading				
Quiescent Current	I_Q			1.3		mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising		2.5		V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}			200		mV
Shutdown Current	I_{SHDN}	V_{SHDN} = 0V		0.02		μA
Output Short Circuit Operation Current	I_{SHRT}					
BOOST AND APD BIASING						
Switch Frequency	f_{SW}			1.3		MHz
Maximum Duty Cycle	D_{MAX}			90		%
V_{VS} to V_{MB} Programming Ratio	VPR			30		
Boost Start-Up Time	t_{UP}	From EN to 90% 70V output voltage, 1mA load		1		ms
Power Switch on Resistance	R_{ON}			0.6		Ω
Peak Switch Current Limit	I_{LIM_SW}			1.1		A
Switch Leakage Current		V_{SW} = 76V, T_A = +25℃		0.1		μA
Mirror Voltage Drop	V_{MD01}	100μA loading, 70V		2.4		v
Mirror Voltage Drop	V_{MD1}	1mA loading, 70V		2.5		v
V_{IN} to V_{APD} Suppression	SR_{APD}	Test by applying 0.1V 1kHz square wave at V_{IN}				%
V_{IN} to V_{MB} Suppression	SR_{MB}	Test by applying 0.1V 1kHz square wave at V_{IN}				%
CURRENT MONITORING						
1X Transfer Resistance	TR_{1X}	APD current to VMON transferring ratio, X1		1.25		kΩ
16X Transfer Resistance	TR_{16X}	APD current to VMON transferring ratio, X16		20		kΩ
Gain Difference Error	G_{DE}	X1 to X16 gain ratio variation				
Low Gain Change Point	LG_{CP}	X1 to X16 gain change, VMON after rising				
High Gain Change Point	HG_{CP}	X16 to X1 gain change, VMON after falling				
X1 In-Scale Error	$1X_{ERROR}$	From change point to 90% X1 FS				
X16 In-Scale Error	$16X_{ERROR}$	From 10% X16 FS to change point				
Full Range Error	FR_{ERROR}	Full range error, from 10% X16 FS to 90% X1 FS				
Monitoring Settle Time	t_{ST}	APD to VMON settle time, to 90%		250		ns
Holding Droop	V_{DROOP}					
VMON Ripple at Tracking	VR_{TRK}	Tracking, C_S 0.1μF, 1mA 70V load		50		mv
VMON Ripple at Holding	VR_{HLD}	Holding, C_S 0.1μF, 1mA 70V load				
VMON PSSR at Tracking	$PSSR_{TRK}$	Tracking, applying 0.1V 1kHz at V_{IN}				
VMON PSSR at Holding	$PSSR_{HLD}$	Holding, applying 0.1V 1kHz at V_{IN}				
I_{LIM} Programming Error	I_{LIMERR}	Test with R_{LIM} = 28kΩ for I_{LIM} = 2.5mA				

ELECTRICAL CHARACTERISTICS (continued)

(Test at T_A = +25℃, V_{IN} = 3.3V, EN = V_{IN}, V_{FS} = 70V for the SGM41281, V_{FS} = 35V for the SGM41281C, unless otherwise specified in test conditions. Limits in boldface type apply over the entire junction temperature range for operation. Limits are production tested, and highly appreciate values on characterization and statistics.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC IO						
Input Low Threshold	V_{IL}				0.4	V
Input High Threshold	V_{IH}		1.6			V
Input Low Souring	I_{LS}	Bias to V_{IL}		1		nA
THERMAL PROTECTION						
Thermal Shutdown Temperature		Temperature rising		160		℃
Thermal Shutdown Hysteresis				15		℃

FUNCTIONAL BLOCK DIAGRAM

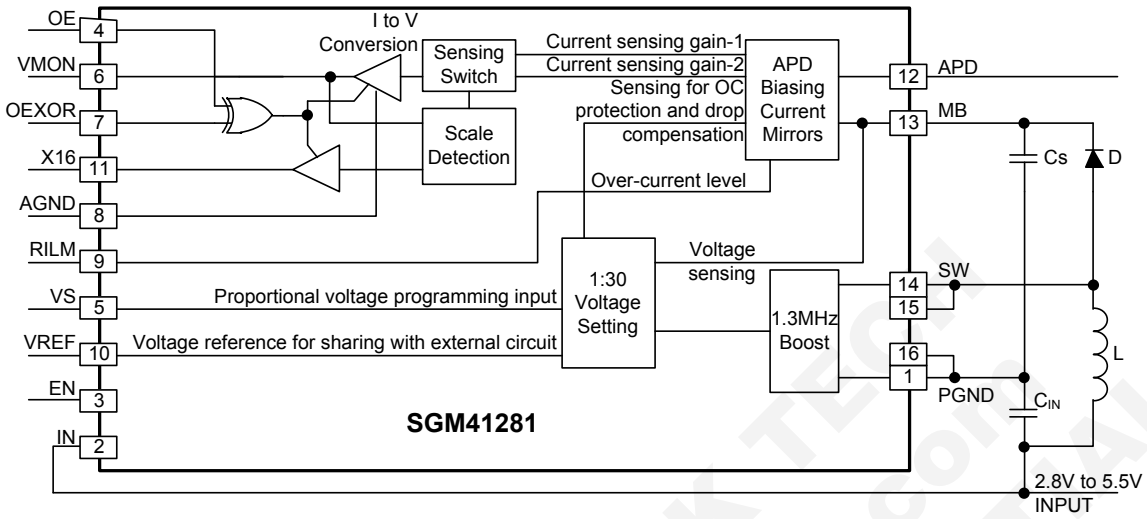


Figure 2. Circuit Block Diagram

OUTPUT SETTLING

插入实测波形替换

调整电流使 VMON 输出 500mV 左右，X16=1；在 VMON 和 X16 均挂 1k 负载。

Figure 3. ON to VMON and X16 Settlings (OEXOR = L)

FUNCTION, OPERATION AND APPLICATION

Ref to the Figure 2 for more details, the SGM41281 has 4 elementary circuits. One is for programming the output voltage and compensating the voltage drop on the mirror circuit; one is for generating a higher voltage from low voltage power source; one is a current mirror that samples the current out of APD pin into internal circuit for monitoring and protection; and the last one is a current to voltage converter and a dual-gains adaptive buffer circuit that selects a proper gain for outputting against APD current level.

Extending the Appreciated Monitoring Range

The VMON buffer circuit could select a proper gain for outputting a suitable signal for external circuit and a flag signal to report which gain selected adaptively by check if the APD current is too low or too high to a given range. This design extends the appreciated monitoring range by 16 times. As the fiber receiver monitors signal in very high dynamic range but less resolution, this circuit is a unique tradeoff between the resolution and dynamic range.

Programming the APD Voltage

The voltage seen at the APD pin is the sum of a component proportional to the setting voltage at the VS pin and a headroom drop designed for the current mirror operation. The voltage at APD pin and the voltage at the MB pin are calculated with following equations, where the V_{APD} is the voltage seen at the APD pin, the VMB is the voltage at the BM pin, the V_{VS} is the voltage put at the VS pin and the I_{APD} is the current out of the APD pin; also reference to the typical VI plots in the Figure 4:

$$V_{PAD} = XX(V_{VS}), YY(I_{APD})$$

$$V_{BM} = ?????$$

此处插入图 4，在 V_{APD} 和 V_{VS} 为轴的坐标中绘制几个不同电流时 V_{VS} 与 V_{MB} 和 V_{APD} 的关系

Figure 4. The V_{VS} to V_{APD} and V_{MB} plots

Programming the Current Limit Level

The RLIM for setting the current limit level is calculated with following equation, and the typical I_{LIM} to R_{LIM} plot is in the Figure 5.

$$R_{\_RLIM}(k\Omega) = \frac{70}{I_{APD,MAX}}(mA)$$

此处插入 I_{LIM} 与 R_{LIM} 的关系曲线

Figure 5. The I_{LIM} to R_{LIM} plot

Ripple Filtering

A simple RC filtering circuit could help in suppression of ripple applied at MB input, which then improving the modulation effect to the signal picked-up in the optical channel, which helps in getting better eye diagram opening. Reference to the Figure 6, the resistance of the R inserts drop that is not compensated.

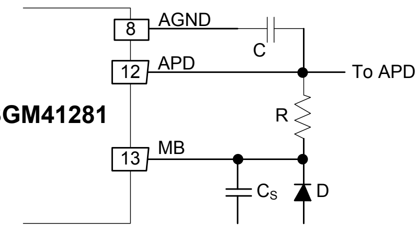


Figure 6. A RC Filtering for Ripple Suppression

FUNCTION, OPERATION AND APPLICATION (continued)

Burst Pulse Response

The Figure 7 shows the capture of waveform at the VMON pin in tracking mode, where a train of current pulses with two different peak values is applied to the APD output, representing the case of burst pulse receiving. The Figure 8 shows the test setup for making the measurement.

用获取的变幅度脉冲串输入时的输入、输出波形取代下图

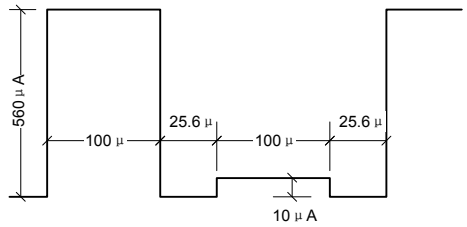


Figure 7. Burst Pulse Receiving Waveform

此处插入测试电路和设备连接图

Figure 8. The Burst Pulse Test Setup

External Components Selection

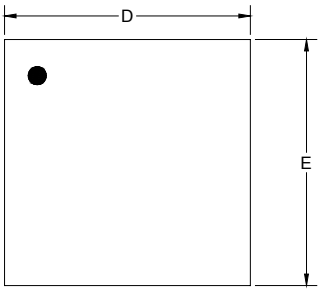
Components Recommended:

C_{IN}	填入电容容量范围和规格。
C_S	填入电容容量范围和规格。
L	填入电感量范围和规格。如果跟最大电流有一定关系，在这说明下。
D	填入我们使用的二极管型号。
R	填入电阻范围。
C	填入电容容量范围和规格。

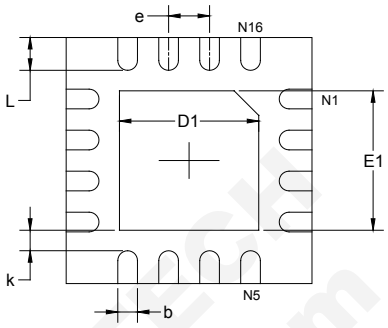
As the boost circuit works at about 1.3MHz, capacitors with good high frequency performance are needed for the application circuit. As the storage capacitor (the C_S in the Figure 1 or the Figure 2) works with high bias voltage, refer to the capacitor's datasheet to assure its effective capacitance is more than 0.1μF at the output voltage.

PACKAGE OUTLINE DIMENSIONS

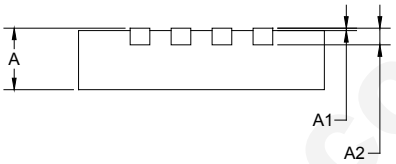
TQFN-3×3-16L



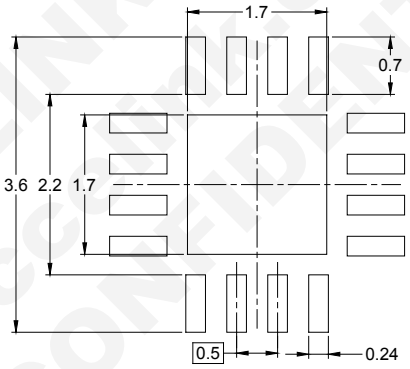
TOP VIEW



BOTTOM VIEW



SIDE VIEW

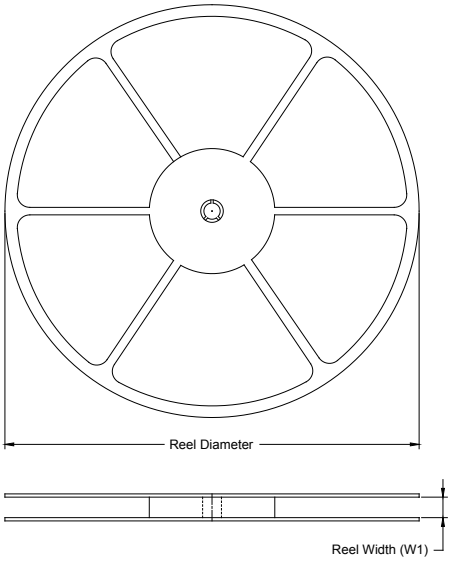


RECOMMENDED LAND PATTERN (Unit: mm)

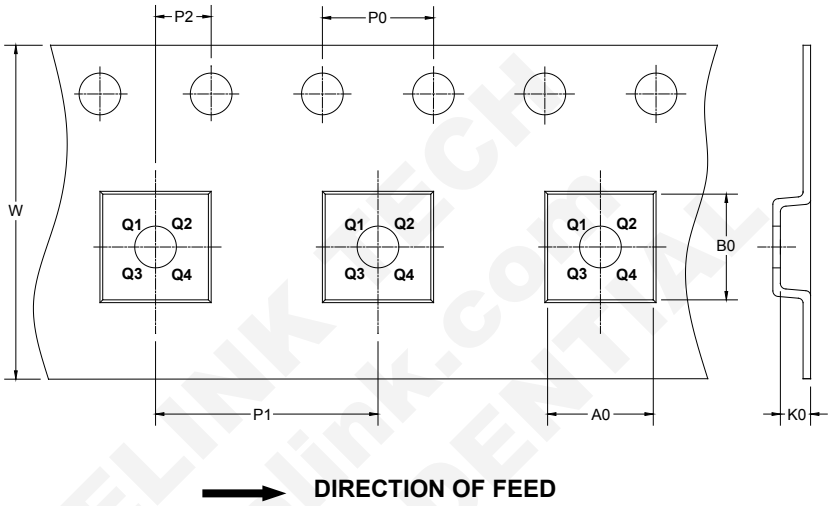
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



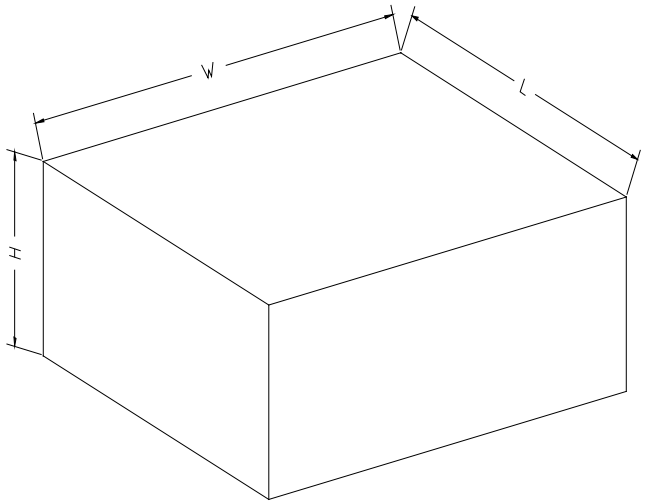
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002