LITE-ON SEMICONDUCTOR

L35ESDL5V0CB2

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE – **5.0** Volts
POWER DISSIPATION – **350** WATTS

GENERAL DESCRIPTION

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diodes in small Surface-Mounted Device (SMD) plastic packages designed to protect one data line from the damage caused by ESD.

FEATURES

- Protects one power or I/O line
- Max. peak pulse power : Ppp = 350W at tp = 8/20 us.
- Ultra Low Capacitance : 1.6pF Typical
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), > ±15KV (air) ; > ±8KV (contact)

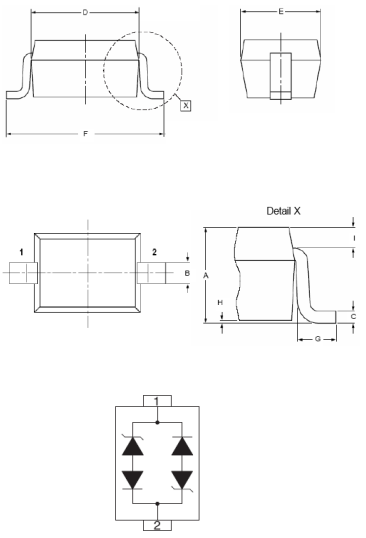
APPLICATION

- Ethernet - 10/100/1000 Base T
- Cellular Phones
- Handheld - Wireless Systems
- Personal Digital Assistant (PDA)
- USB Interface

MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish), solderable per J-STD-002 and JESD22-B/02.
- Moisture Sensitivity: Leve 1 per J-STD-020C
- Component in accordance to RoHs 2002/95/E

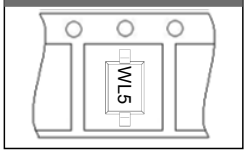
SOD-323



SOD-323		
DIM.	MIN.	MAX.
A	0.80	1.10
B	0.25	0.40
C	0.10	0.25
D	1.60	1.80
E	1.15	1.35
F	2.30	2.70
G	0.15	0.45
H	----	0.05
I	0.15	0.25
All Dimensions in millimeter		

PIN ASSIGNMENT	
1	Cathode
2	Cathode

Marking & Orientation



MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	P_{pk}	350	W
Peak Pulse Current (tp = 8/20us)	Ipp	17	A
Operating Junction Temperature Range	T_J	-55 to + 150	℃
Storage Temperature Range	Tstg	-55 to + 150	℃
Soldering Temperature, t max = 10s	T_L	260	℃

ELECTRICAL CHARACTERISTICS (Tj= 25℃ unless otherwise noticed)

Parameter	Symbol	Conditions	Mln	Typ	Max	Unit
Reverse standoff voltage	V_{RWM}		---	---	5.0	V
Breakdown voltage	V_{BR}	I_R = 1 mA	6.0	---	8.0	V
Reverse leakage current	I_{RM}	V_{DRM} = 5V	---	---	5	uA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs	---	---	9.8	V
Clamping Voltage	V_C	I_{PP} = 17A, tp = 8/20μs	---	---	21	V
Junction capacitance	C_J	V_R = 0V, f = 1MHz	---	1.6	3.5	pF

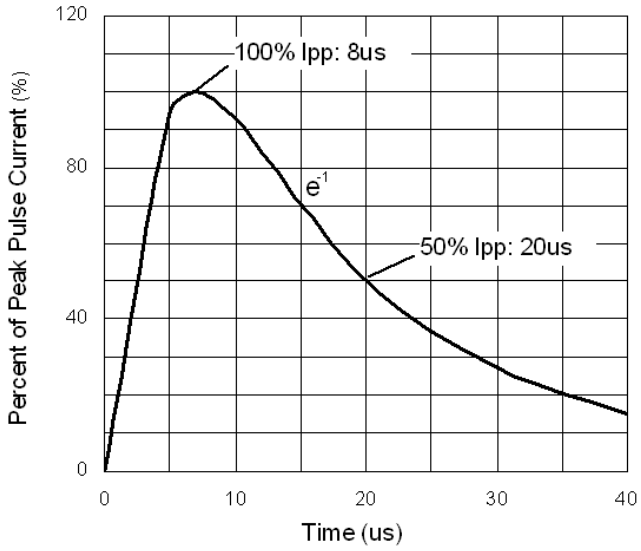


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

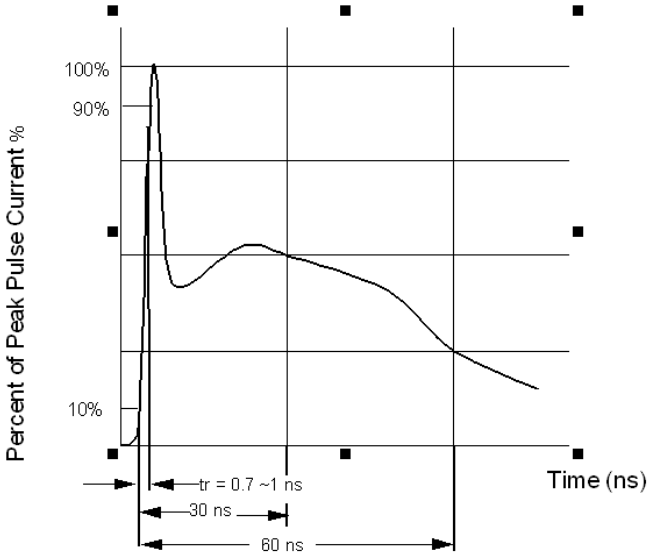


Figure 2. ESD pulse waveform according to IEC 61000-4-2

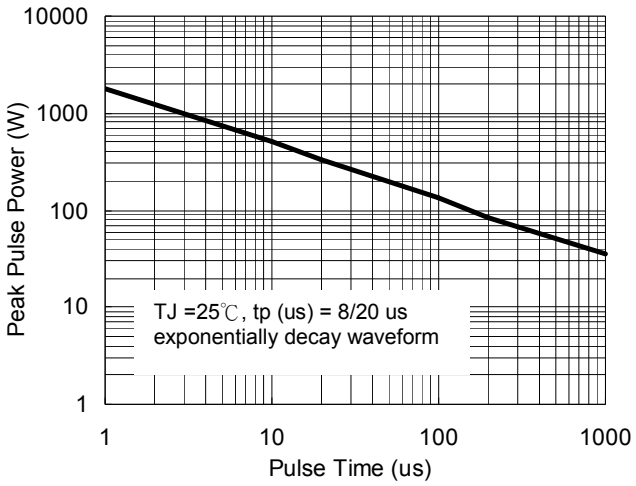


Figure 3. Power Dissipation versus Pulse Time

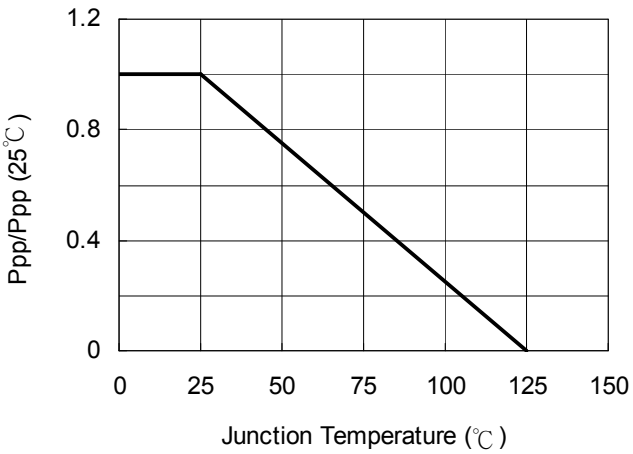


Figure 4. Peak pulse power versus TJ

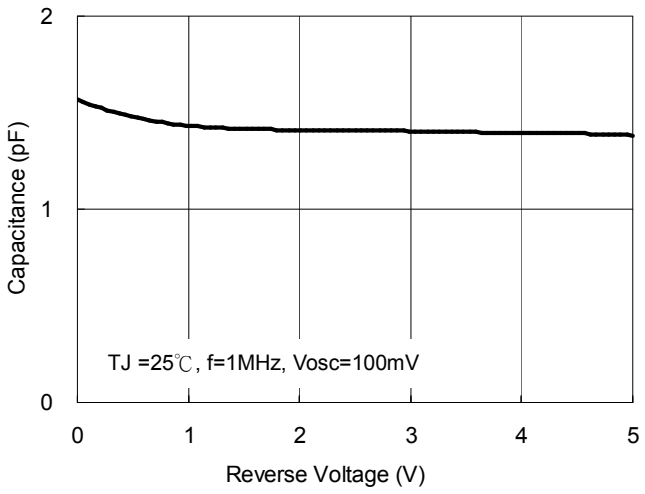


Figure 5. Typical Junction Capactiance

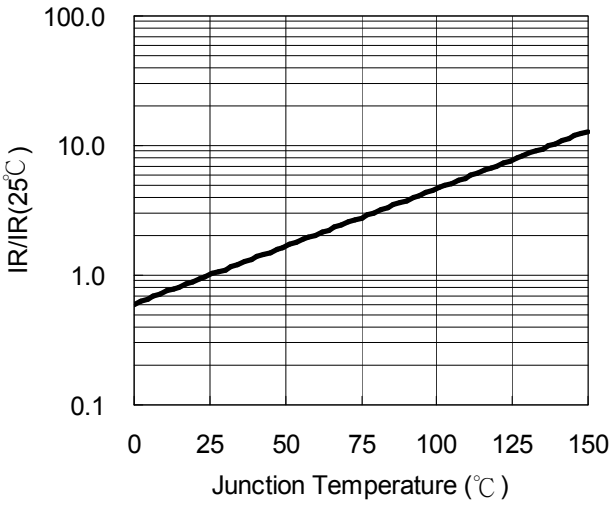


Figure 6. Reverse Leakage Current versus TJ

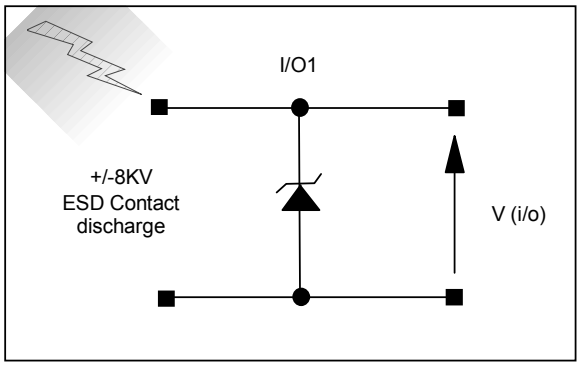


Figure 7. ESD Test Configuration

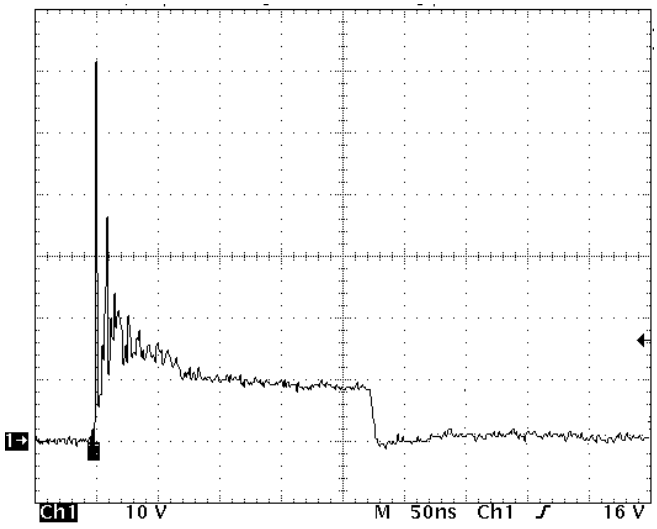


Figure 8. Clamped +8 kV ESD voltage waveform

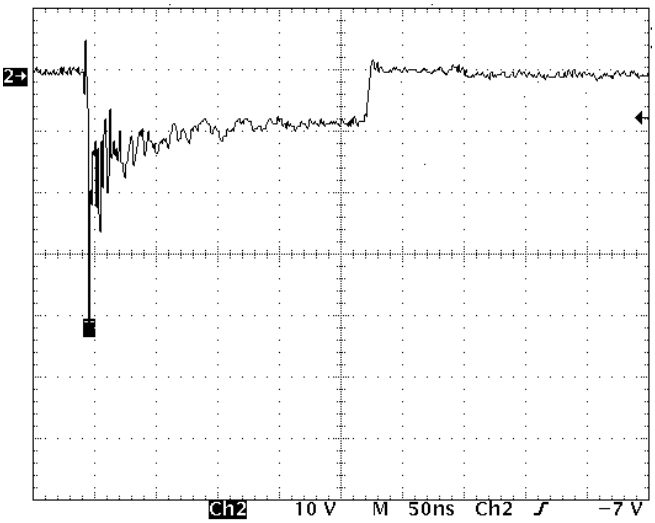


Figure 9. Clamped -8 kV ESD voltage waveform

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